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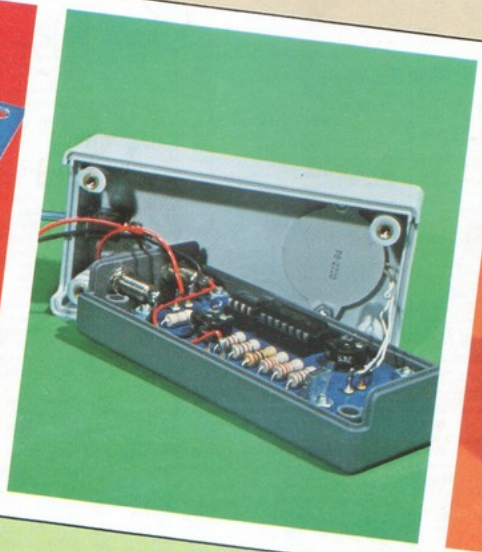
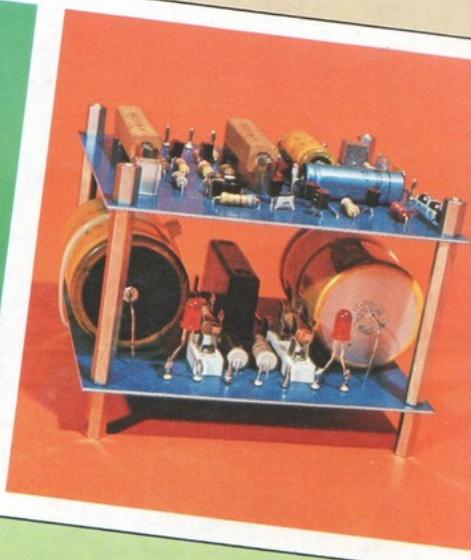
Surinder Singh





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contents

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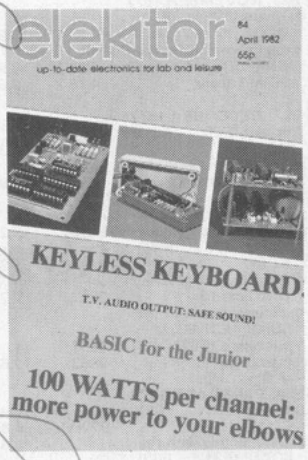


Holographics and crime

Civil and government authorities in the United States are getting seriously concerned with the criminally abusive use of the very latest technological advance in opto electronics. A recently published report states that the realisation of holographic projections (HP) is creating havoc in law enforcement agencies throughout the USA. It would appear that the legal aspect regarding a holographically projected image has yet to be defined. This state of affairs has been brought to light by the felonous activities in the use of HP with regard to fraud.

Several large companies involved in the sale of second-hand cars initially used HP for the purpose of defrauding the Inland Revenue Service. In order to qualify incorrect sales figures on tax returns the companies used HP to project the images of a far larger stock of vehicles than actually existed in their showrooms. However, one car distributor extended the use of HP a little too far with the result that its entire stock consisted of vehicles that did not in fact actually exist. This action went undetected until an unfortunate buyer purchased a vehicle that was an HP. The driver took the car home and found in the morning to his horror that the car had disappeared. Unknown to the car sales company, the current state-of-the-art in holographic projection can only maintain an image for about 20 hours.

It is known that prominent figures in criminal organisations are using HP in order to confirm their appearance in public when they are likely to be suspected of felonous activities elsewhere. Certain unscrupulous politicians have also been known to maintain an HP image of themselves at social and public functions. When questioned they maintained that this directly effected a gain in popularity. The authorities fear that this use of HP may spread into vice, armed robbery and bodily assault.

One personnel officer in a multinational corporation has expressed concern at the high rate of possible absenteeism at senior executive level. The legal position of a holographically projected image of an employee is rather uncertain with regard to pay and working conditions. This has far-reaching effect when accident insurance claims are submitted for an injury sustained to an HP image on employers' premises.

The disappearance of large amounts of cash from a number of clearing banks in the Mid West is now being attributed to the use of HP. In view of this the FBI have been assigned the task of verifying the existence of the Federal gold reserve at Fort Knox. Fears are increasing for the long-term stability of the American economy.

Real estate has not been overlooked in the illegal use of HP. In a recent court case in Redwood City L.A., a fraudulent financier was indicted for selling a chain of hotels that did not exist. Apparently the buyer discovered the plot when the particular hotel in which he was staying disappeared during a local power failure. The missing persons branch of the FBI discovered another fraudulent use of HP when attempting to trace a number of families who apparently disappeared while on holiday. The common factor in a large proportion of the cases was a travel agency, Moonlight Travel, which, following investigations, was found not to exist. It is thought that the company used holographic projections of offices, aircraft, staff and holiday resorts to fly unsuspecting holidaymakers to Jackson Heights, a suburb of New York.

The worry expressed by the authorities cannot be understated since it has been suggested in some quarters that the Statue of Liberty in New York harbour is an HP. The original was reputedly sold to a wealthy Arab at some time during 1968 in order to aid the failing economy of the City of New York.

However, HP also has its positive side since sources suggest that the US government have been experimenting with HP power stations for the past two years. It is hoped that this may be an answer to the energy crisis.

So far the abusive uses of HP have not reached the UK to any great degree. A spokesman for Scotland Yard speaking from the Metropolitan Police Headquarters in Hyde Park stated that, 'Reports that certain members of the conservative party are engaged in H.P. have not been substantiated by our staff'.

APR Inc. USA

(S 758)

An example of specialised equipment modified for use in H.P. This photograph was obtained by the good offices of a prominent U.K. manufacturer.

Flawless micro-machining by beams of ions

Ions, several thousand times as heavy as free electrons, cause a great deal of damage on an atomic scale when they are accelerated by high electric potential into a beam striking the surface of a workpiece. In this way they can be used to knock off fragments, atom by atom, in a highly precise machining or etching process. Machining tools based on the ion-beam technique are now being used by the micro-electronics manufacturing industry, where it has great potential for the production of chips with very high packing densities. Ion beams are capable of cutting a neat groove as little as one micrometre deep, with a repeatable precision of the order called for when, as will almost certainly happen in the not-too-distant future, a million 'bits' may be incorporated on a single minute slice of semiconductor material.

Dr. Roy Clampitt, of Oxford Applied Research at Witney, near Oxford, believes that industry could find a large number of diverse applications for the technique. His company, formed three years ago, provides an independent centre for research and is able to call upon the vast knowledge and expertise to be found in the Oxford area. Established applications of the ion-beam technology already include cutting fine lines on optical flass for use in spectrophotometers, and in smoothing titanium steel for joints in replacement-part surgery. The picture shows an engineer making final adjustments to ion-beam equipment prior to its despatch from Witney.

Spectrum No. 175

(757 S)

The silent noise of a gas turbine

The low-pitched rumble from gas turbines can be felt as much as heard over a radius of one kilometre or more from aircraft engine test beds and similar installations. It is a background noise which many people find objectionable and even distressing when continuous, and hitherto it has proved almost impossible to suppress. Now, in what is believed to be the first successful application of electronic 'active sound control' to this kind of problem, noise from one such machine has been cut to one-twentieth of its original level. Such vibration-cancelling devices promise to become a common feature of machines and vehicles of the future.

All who have examined high-fidelity music systems know that it is the low-frequency, bass sounds that are most difficult and expensive to control. To reproduce them faithfully calls for large loudspeakers, which give out a sound that penetrates the walls and ceilings of houses and is heard far away as a booming or rumbling noise; the treble elements lack such persistence and are easily absorbed.

So it is, too, with the noise of powerful machinery. Though the high-frequency elements are easily muffled, suppressing the bass rumble is extremely difficult and costly, for it means investing in massive acoustic enclosures. The gas turbine, our most compact source of power, is also man's noisiest machine. Little wonder that it is on the gas turbine that most noise-control development is concentrated and that the first full-scale demonstration of anti-noise techniques is now reported.

Anti-sound

Noise is a vibration of the air, the pattern of aerial vibrations travelling in waves from source to receiver and beyond. And different noises can be superposed without distortion or loss. Incoherent sounds do not interfere with the background chatter at a cocktail party and in no way deform any particular conversation; only raised voices are heard — but the tonal quality and information in the successive undulations of the sound wave are not in the least distorted by the different level. Nor would two sounds, one with peaks and troughs corresponding exactly to the other's troughs and peaks, interfere. But the combination of the two would be silence, for one would be the negative of the other. That is the principle of anti-sound, a principle that has progressed from its science-fiction base,

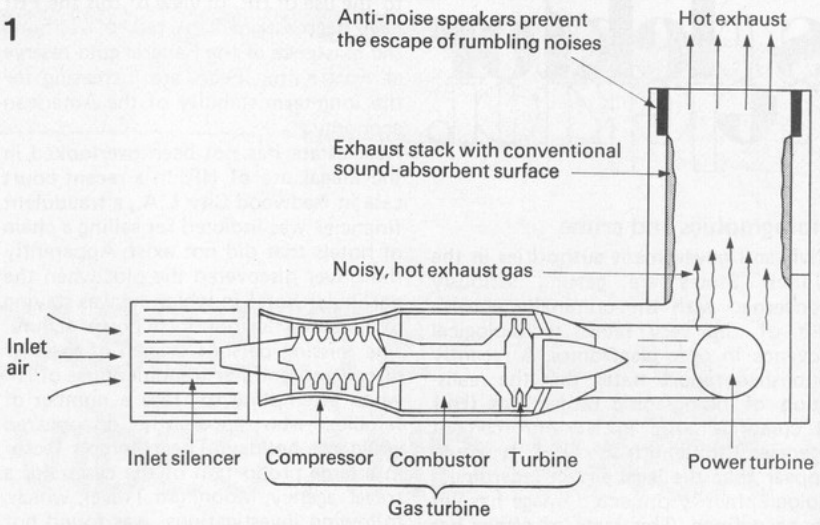


Figure 1. Blockdiagram of the gas-turbine compressor plant that has been silenced by anti-sound.

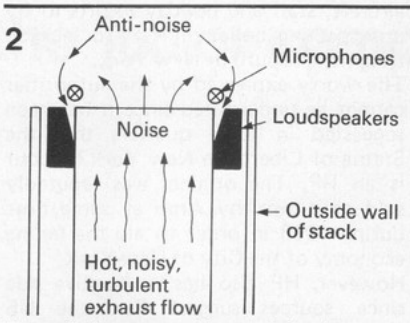


Figure 2. Arrangement for obviating low-frequency noise by anti-sound from actively-controlled loudspeakers.

through numerous small-scale and laboratory experiments to this full-scale application on an 11-MW gas turbine.

The UK National Research Development Corporation (NRDC) has stimulated the growth of this novel method of noise control for more than ten years. It has sponsored projects to perfect the technique and bring it out of the laboratory to a practical application. The technique calls for fast electronic signal processing and precise superposition of the noise and anti-noise fields, so it is most easily applied to the low-frequency, long-wavelength elements of noise, the sort that cause the window-rattling rumble of large engines. Because it is this very rumble that has always been most difficult to suppress, the new technique is a welcome complement to existing mufflers, which work best at high frequencies.

Two years ago, laboratory demonstrations had reached the stage where the time was ripe for field trials. A worth-while trial to suppress loud rumble would mean running powerful machines, for they alone are capable of generating rumble at a really annoying level. The British Gas Corporation agreed to cooperate by allowing one of their compressors powered by a Rolls-Royce Avon engine to be fitted with 'anti-sound', and the job was taken on by Topexpress, a small, high-technology research company based close to Cambridge University. Within six months it was demonstrated that control was feasible, and the anti-noise suppressor was built, fitted and switched on within two years. It instantly silenced a rumble that would otherwise be heard more than a mile away — and annihilated it everywhere. NRDC's £ 300 000 investment in the principle had brought a new hush to the landbased gas turbine; it would take more than ten silenced units to make as much noise as the standard, unsilenced one. Moreover, the silencing carries no performance penalty and is attained at less than half the cost of conventional muffling.

Airflows

Gas turbines operate by compressing air which is then heated at high pressure by burning gas in it. The hot products of combustion flow through the turbine, which extracts most of the energy. The engine uses that energy to drive its own compressor, leaving a balance over for useful work. With the Avon, the balance is 11 MW. After flowing through the turbine the hot, spent gases are exhausted through a stack, which they enter in a highly turbulent and noise state. The airflows are large and the exhaust is eventually vented to the atmosphere at a speed of some 50 m/sec and a temperature of 200°C from a duct with a diameter of three metres. The inlet to the engine is carefully treated to prevent noise escaping from the site, and so is the exhaust, but that poses a much more challenging problem. It is not easy to absorb and prevent the escape of noise when one end of the pipe is a gaping three-metre hole! In practice the noise control is extremely good, but inevitably the low-frequency rumble escapes. That rumble is a broadband sound in the frequency range 20 to 50 Hz, with the peak of the spectrum

at just over 20 Hz. Of course, this noise too can be controlled by conventional means, but only by constructing massive extensions to the exhaust stack, an expensive operation that makes the installation more visually obtrusive. The suppression of the rumble without any modification to the stack was the task set to the Topexpress team.

Information

The first step was to monitor the sound with advanced, highly accurate equipment to find out its level and waveform, how it varied from time to time and point to point and to discover in particular whether a control signal could be obtained to drive the active control gear. The entire technique depends on obtaining enough information about the precise characteristics of the noise and activating the anti-noise sources in time to prevent the sound escaping from the chimney. The Topexpress team had to be sure both that the control technology existed and that the acoustical equipment was good enough for the job before deciding to embark on manufacture. It was – but there was little room for manoeuvre. Amplifiers would have to handle 12 kW of peak power, enough to drive 72 of the loudest bass loudspeakers known to discos.

The diameter of the exhaust stack is about half the wavelength of the highest-frequency elements to be controlled and is just small enough for the noise field to have a relatively simple geometry. A good control signal was obtained by using four microphones.

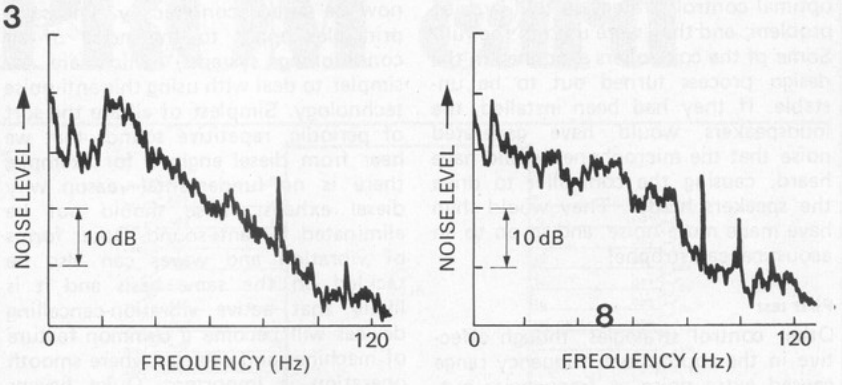


Figure 3. Noise spectrum (left) without active silencer and (right) with active silencer in operation.

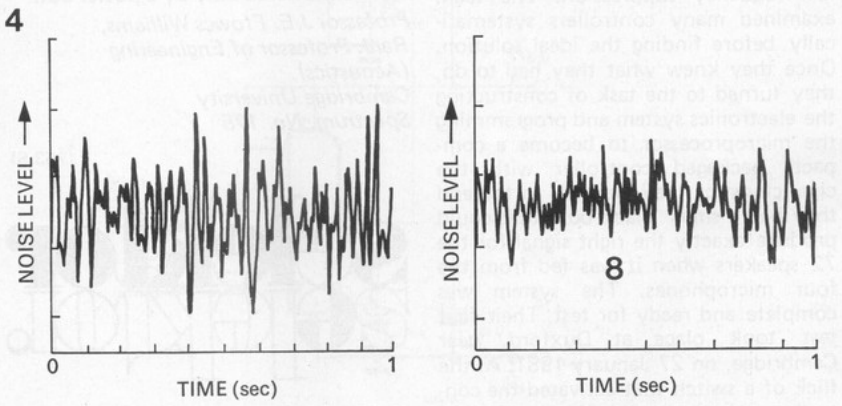
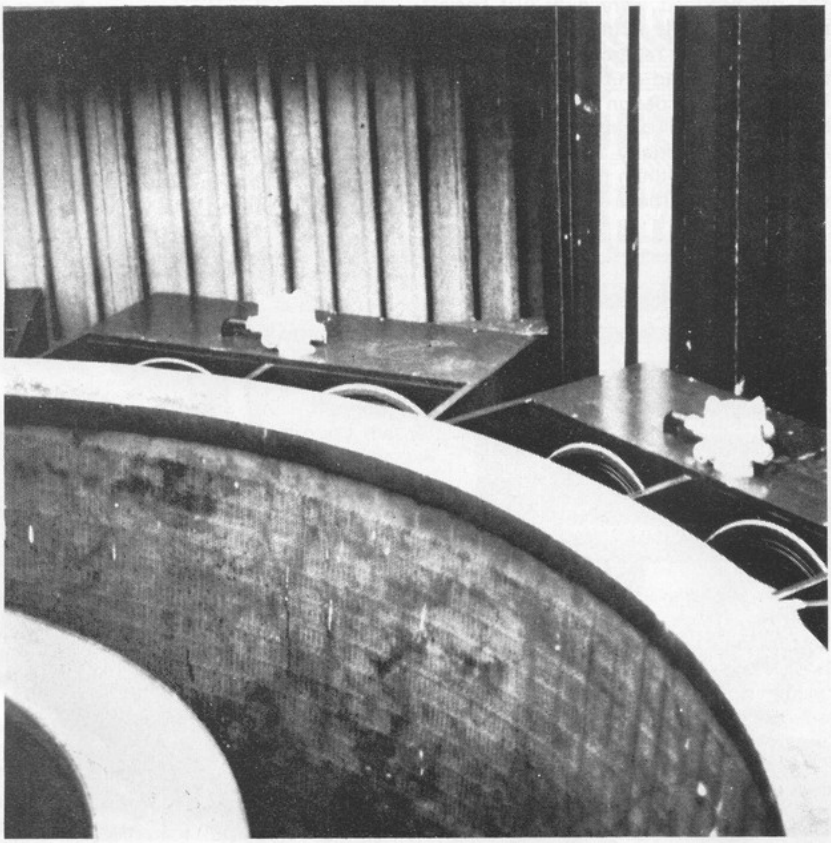


Figure 4. Time record of noise (left) without active silencer and (right) with active silencer in operation.



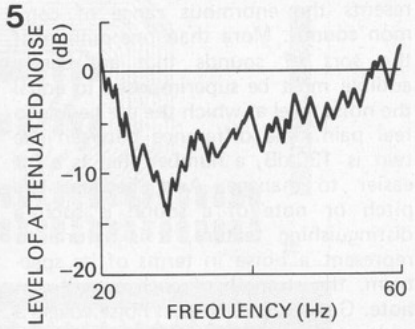


Figure 5. Spectrum of attenuation achieved by the active silencer.

The loudspeakers were tightly packed around the stack exit and early tests which recorded signals showed that the audio system could accurately mimic the noise. Conditions were expected to change when the gas turbine was started up and the exhaust duct filled with moving, turbulent, hot gas, but the change was anticipated satisfactorily. So, the team has reached the critical stage in producing a control system.

It would be necessary to accept the signals from the four microphones and generate an electrical input to the loudspeakers that would induce them to cancel exactly the exhaust noise. There are powerful mathematical and compu-

tational techniques for establishing the optimal control strategy in that type of problem, and they were used to the full. Some of the controllers examined in the design process turned out to be unstable. If they had been installed, the loudspeakers would have generated noise that the microphones would have heard, causing the controller to drive the speakers harder. They would then have made more noise, and so on to an acoustical catastrophe!

First test

Other control strategies, though effective in the appropriate frequency range caused extra noise at frequencies outside the control band; they would have produced an unacceptable emphasis of high-frequency noise as the price for low-frequency suppression. The team examined many controllers systematically before finding the ideal solution. Once they knew what they had to do, they turned to the task of constructing the electronics system and programming the microprocessor to become a compact, packaged controller with the characteristics they wanted. In the end they had a small 'black box' that could produce exactly the right signal for the 72 speakers when it was fed from the four microphones. The system was complete and ready for test. Their first test took place at Duxford, near Cambridge, on 27 January 1981. At the flick of a switch that activated the controller, the gas turbine's rumble disappeared.

Noise levels are measured in decibels, a logarithmic scale that compactly represents the enormous range of common sounds. More than one million of the sort of sounds that are barely audible must be superimposed to equal the noise level at which the ear begins to feel pain. The difference between the two is 130 dB, a number that is a lot easier to manage. And, because the pitch or note of a sound is such a distinguishing feature, it is natural to represent a noise in terms of its spectrum, the strength of each constituent note. Gas turbine exhaust noise covers a wide and continuous spectrum and the active silencer attained a reduction of about 10 dB across the lowest octave, with a peak attenuation of 13 dB, which represents a factor of 20. In other words it would have taken 20 silenced compressors, all working simultaneously, to make as much noise as the unsilenced one.

Work is going on to develop the system to even better standards. Meanwhile, it will be possible to duplicate this anti-noise system at less than half the cost of silencing a gas turbine's rumble by conventional means. Moreover, the new silencer is not visible from the outside and has no detrimental effect on the engine's performance, which cannot be said of the conventional techniques that call for massive enclosures and partial throttling of the engine's exhaust.

This means that gas turbine rumble can now be cured economically. The same principles apply to the noise of air conditioning systems, which are far simpler to deal with using this anti-noise technology. Simplest of all are the sort of periodic, repetitive sounds that we hear from diesel engines, for example; there is no fundamental reason why diesel exhaust noise should not be eliminated by anti-sound. Other forms of vibration and waves can also be tackled on the same basis and it is likely that active vibration-cancelling devices will become a common feature of machines and vehicles where smooth operation is important. Quiet havens could be built — there is no obvious end to the development that is possible. We can look forward to a future quiet that will be shattered only by a power cut!

Professor J.E. Ffowcs Williams,
Rank Professor of Engineering
(Acoustics),
Cambridge University
Spectrum, No. 175

(753 S)

New reading aid

As 1981, the Year of the Disabled, drew to a close, ideas to make life easier for the handicapped were only just beginning to dawn. It is interesting to note the favourable repercussions that the campaign has had on the manufacturing industry, the design described here being just one of many devoted to helping the partially sighted read and thus providing them with better communication facilities.

The electronic reading aid incorporating the latest in optical technology has been developed by engineers at Wormald International, a New Zealand company specialising in aids for the disabled.

The aid, called Viewscan, is portable and can be used by the partially sighted at work, school or home. It is designed to produce a bright, magnified image of reading material when the material is scanned by a hand-held camera.

A 0.5 W micro-miniature bulb illuminates the page via a high resolution fibre optic ribbon in the solid state camera. The image is transmitted to a photo diode array and the signal from this is fed directly to two high speed microprocessors in the display unit. A buffer memory then reassembles the information into moving lines of print.

The display screen, developed specially for Viewscan, is a flat neon matrix panel. Special attention was paid to colour. The orange shade for the display has been selected for reasons of maximum visibility and clarity and can be switched easily from a positive to a negative image. Other display colours were extensively researched but orange was finally chosen because it can also provide higher levels of brightness than any other alternatives. Magnification is achieved electronically and the eight settings from X4 to X64 are easily selected by means of a switch on the front panel.

Viewscan is efficient and economical in power consumption so that a portable version can be powered using rechargeable NiCad batteries.

Wormald International

(743 S)

mini EPROM card

a miniature memory extension for the Junior Computer

This is an elegant, low-cost solution for Junior Computer owners seeking a suitable RAM extension (to accommodate the Junior BASIC or a large assembler, for instance). At the same time, the board takes up a minimum of space.

Book 3 in the series on the Junior Computer explained how to fetch the three NMI, RES and IRQ vectors from EPROM connected to the bus board (and page FF). Appendix 3 gave an example of this using a 82S23 PROM. A 2716 EPROM, however, provides a better solution, as it is much more straightforward to program (see the 'EPROM programmer' in the January issue, E-81). The miniature board described here is designed to cater for 2k of EPROM.

The circuit diagram for the miniature EPROM card is shown in figure 1. The EPROM stored in IC2 is addressed by way of IC1. The memory range comprises addresses $F8ØØ . . . $FFFF. Two wire links enable the range to be accessed either by way of pin $\overline{OE}$ (Output Enable) or by way of pin $\overline{CE}$ (Chip Enable). On the one hand the Output Enable method speeds up EPROM operation, but consumes a fair amount of stand-by current. On the other hand, Chip Enable addressing saves up to 300% current and is slightly slower. Readers may choose either method, provided they remember to ground the enable pin and connect the other to the output of IC1. This is carried out with the aid of the links shown in the circuit diagram.

Finally, the following data must be programmed into the final six locations in the $F8ØØ . . . $FFFF memory range:
address $FFFA should store 2F;
address $FFFB should store 1F;
address $FFFC should store 1D;
address $FFFD should store 1C;
address $FFFE should store 32;
address $FFFF should store 1F.
The remaining 2018 memory locations are entirely at the disposal of the operator.

1

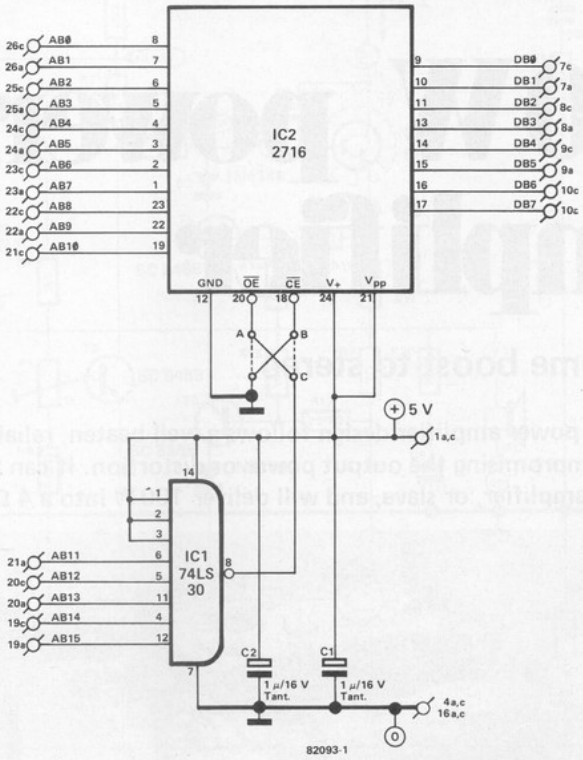


Figure 1. The 'mini' EPROM circuit diagram.

2

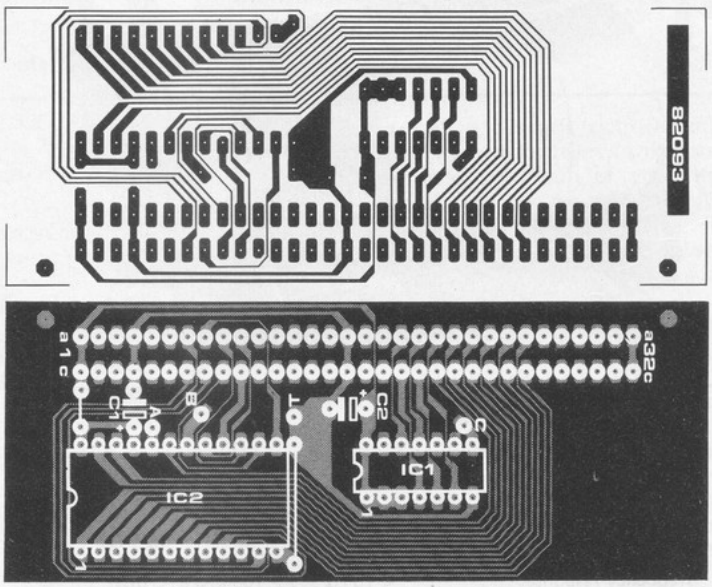


Figure 2. The component overlay and the copper track pattern for the mini EPROM printed circuit board.

Parts List

Capacitors:
C1,C2 = 1 µ/16 V tantalum

Semiconductors:
IC1 = 74LS30
IC2 = 2716

Miscellaneous:
1 64-pin male connector ('a' and 'c') 41612

100 W power amplifier

a welcome boost to stereo

This 100 W power amplifier design follows a well-beaten, reliable track, without compromising the output power or distortion. It can be used as a power amplifier, or slave, and will deliver 100 W into a 4 Ω load.

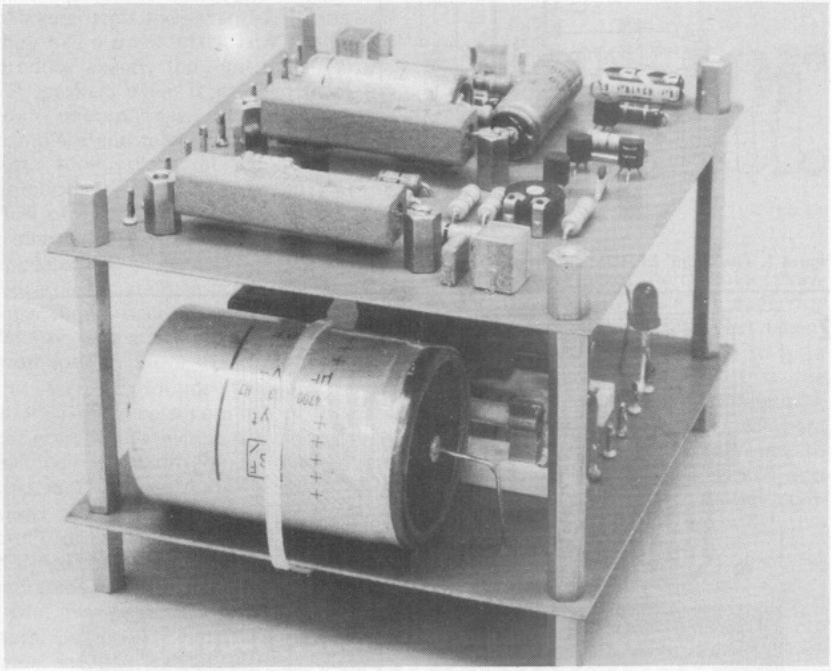


Table 1

Technical specifications:	
output power:	
(continuous sinewave signal)	100 W (R_L = 4 Ω, k = 0.1%) 70 W (R_L = 8 Ω, k = 0.1%)
power range:	< 10 Hz . . . > 20 kHz at 100 W,
frequency response:	< 10 Hz . . . > 100 kHz (−3 dB)
distortion:	< 0.1% at 20 Hz . . . 20 kHz and 100 W
intermodulation distortion:	0.28% measured at 40 Hz and at 10 kHz; amplitude ratio 4 : 1, P_a = 100 W
S/N ratio:	70 dB
input sensitivity:	0.775 V at full modulation
input impedance:	100 kΩ
output impedance:	0.052 Ω (at 1 kHz)
minimum load:	4 Ω
supply voltage:	80 V symmetrical (+40 V, 0, −40 V)
current consumption:	2.25 A max. where R_L = 4 Ω
transistor quiescent current:	50 mA

Output power amplifiers (or slaves as they are known in the music world) are not only fun to build, but can be adapted to suit anyone's personal requirements. With the aid of numerous interesting suggestions made by readers, a set of parameters for the 'ideal' power amplifier were drawn up:

- It must deliver 100 W (into 4 Ω load).
- The distortion must not exceed 0.1% at 100 W (even at 20 kHz!).
- The power bandwidth should be extensive.
- It must be 'short' proof, for the protection of the output transistors.
- The power supply must be symmetrical, so that no electrolytic capacitors are needed in the output stage.
- Only standard, easily available components should be used.
- Construction and calibration must be straightforward.
- The amplifier should be economically viable, and reliable.

Some readers are bound to think that to build an amplifier that complies with most (if not all) of the above parameters is practically impossible. However, they should reserve judgement until they have taken a closer look at this compact circuit, designed around modern darlington transistors.

How does this particular circuit compare to other Elektor amplifiers published in the past? Well, the highly popular EQUA and EQUIN amplifiers were not intended to deliver anything like as much power. The Elektornado can only manage 100 W when it is constructed in the form of a bridge circuit. At the other extreme we have the 'disco power amplifier' which was described in the January 1981 issue. This does provide 200 W (into 4 Ω), but suffers from a restricted (low) frequency response and has the disadvantage that electrolytic capacitors need to be used in the output stage. Taking everything into consideration the need arose for an inexpensive, good quality, medium rated power amplifier design.

The circuit

Figure 1 shows the complete amplifier circuit diagram. The input consists of a discrete differential amplifier, built up around transistors T1 and T2. This is followed by the driver stage T4, the collector of which is connected to transistor T3. This acts as an 'adjustable zener diode' and sets the quiescent current level. A fully complementary output stage (using darlington transistors T7 and T8) is connected to the driver. One advantage of using a symmetrical power supply is that the midpoint between T7 and T8 has a zero voltage potential, avoiding the need for an electrolytic capacitor at the output.

The amplifier has a fairly high input impedance of 100 kΩ, since C4 is 'bootstrapped' by R2; the input impedance of T1 is also quite high, of course.

1

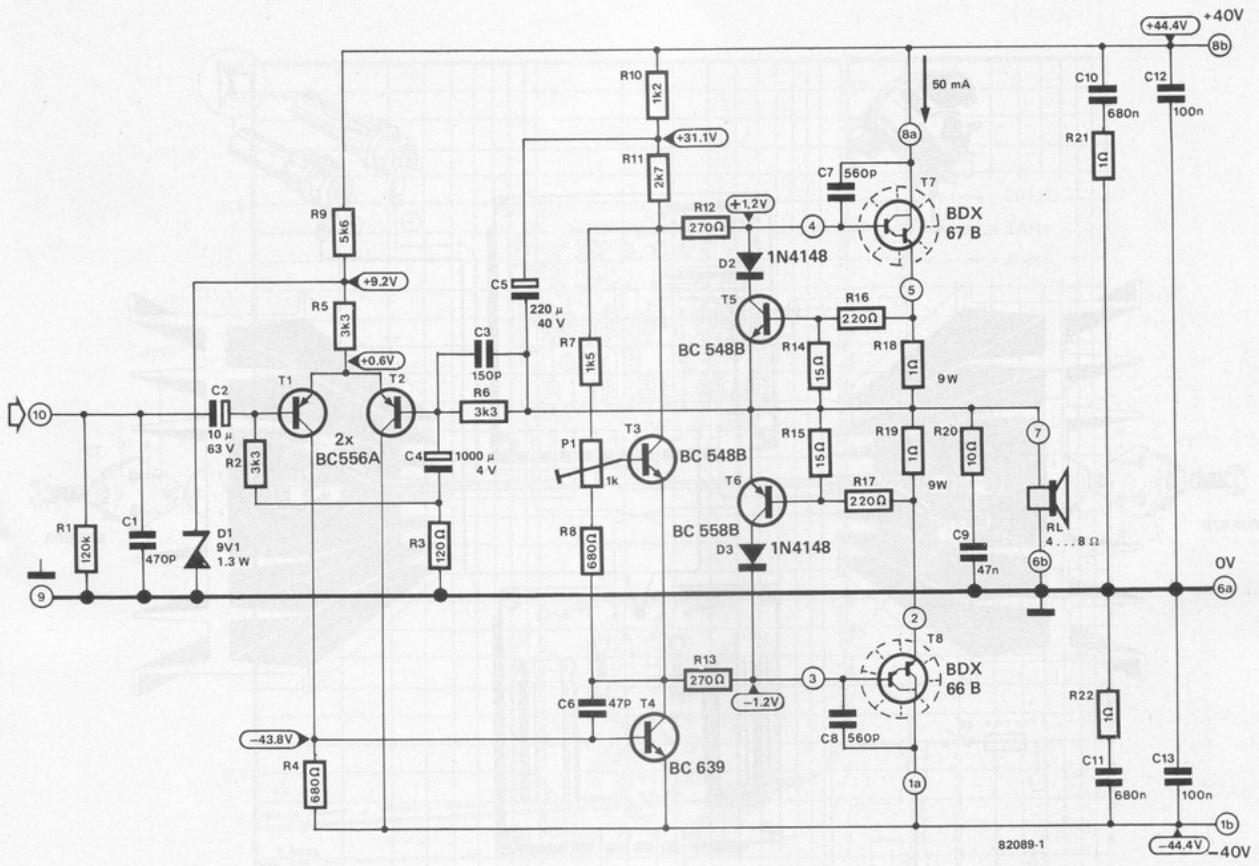


Figure 1. The 100 W power amplifier circuit diagram. Distortion is low, even at high output levels.

2

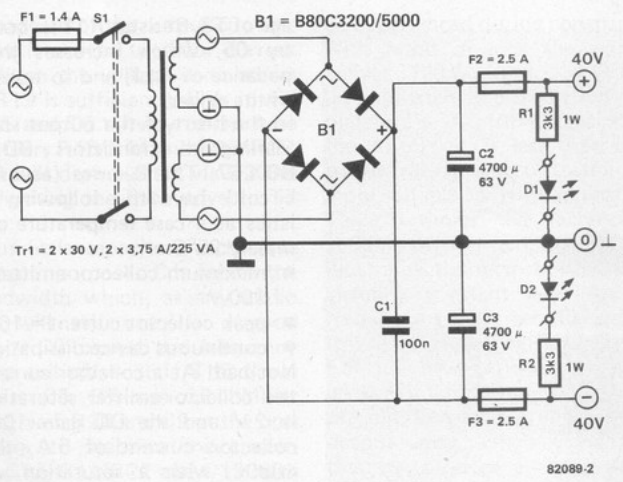


Figure 2. This straightforward power supply meets every requirement thanks to the quality of its mains transformer. With ± 40 V, 2.5 A can be supplied.

Negative feedback (both DC and AC) is fed from the output to the base of T2 (the other input of the differential amplifier) by way of R6. The DC component of the negative feedback keeps the output at a zero voltage potential. The AC feedback determines the gain as set by R6, (C4) and R3. Using the values in the circuit (figure 1) the gain can be seen to be:

$$\frac{U_o}{U_i} = \frac{R3 + R6}{R3} = \frac{3420}{120} = 28.5x$$

The driver T4 is coupled to the collector of T1. T4 boosts the signal; it must be capable of supplying the output transistors (T7 and T8) with sufficient base current. Fortunately, the darlington transistors (T7 and T8) require very little base current, since they have a high current gain. As a result T4 dissipates a negligible amount of heat, and therefore does not need to be 'cooled'.

Transistor T3 determines, and resistors R18 and R19 stabilise the quiescent current passing through the elements of the output stage. The voltage drop across the emitter resistors R18 and R19 is determined by the setting of P1, since this sets the collector-emitter volt-

3,4

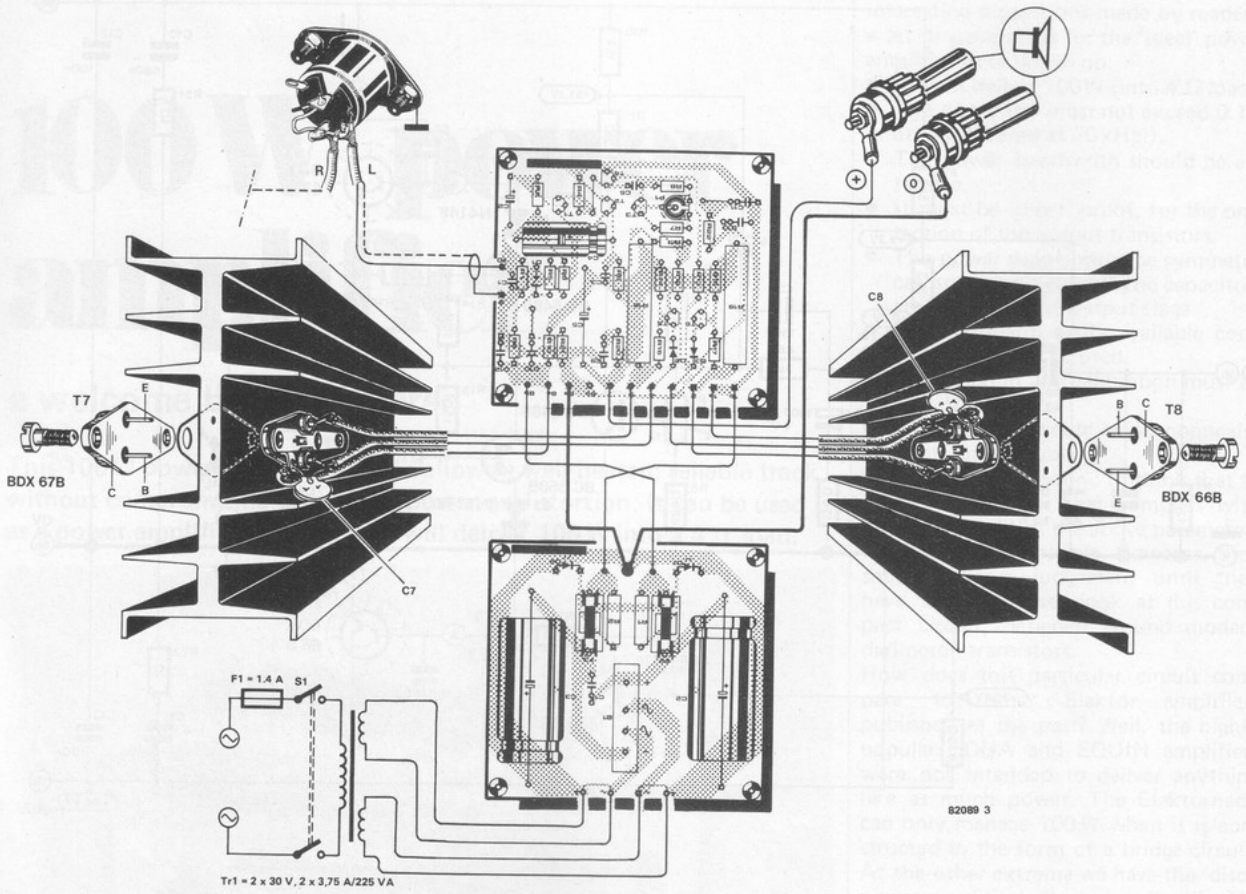
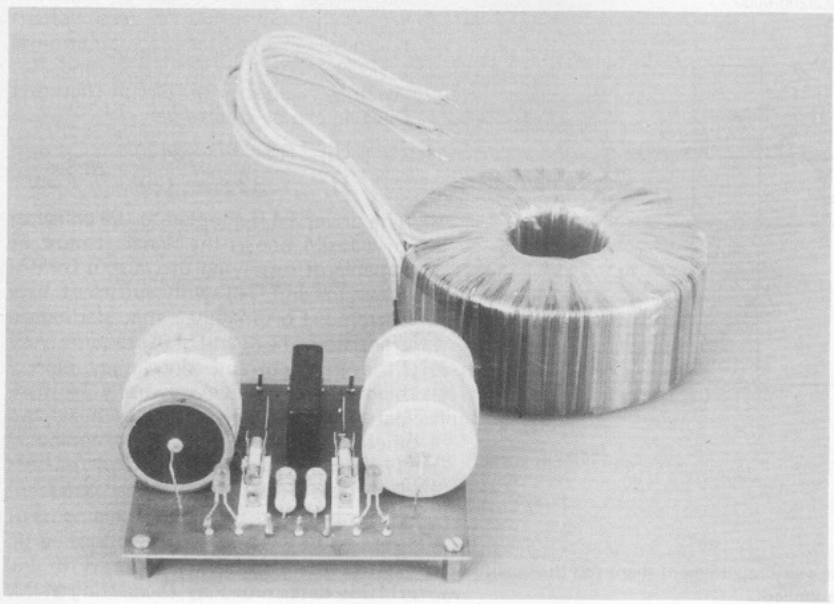


Figure 3. Exploded view of the darlington power transistors on the heat sink, see text.

Figure 4. The power amplifier connections.



age of T3. Resistor R11 is 'bootstrapped' by C5, which increases the AC impedance of R11, and so boosts the gain of the driver.

In the heart of the output stage are the 'darlington' transistors BDX 66 and BDX 67. The B-series (as used in this circuit) have the following characteristics at a case temperature of approximately 25°C:

- maximum collector-emitter voltage = 100 V
- peak collector current = 16 A
- continuous device dissipation = 150 W

Not bad! At a collector current of 10 A the collector-emitter saturation voltage is 2 V and the DC gain 1000x. At a collector current of 5 A, the gain is 4000x, with a saturation voltage of between 0.4 and 0.5 V. These characteristics make the BDX 66 and BDX 67 ideal for this type of circuit!

No matter how 'sturdy' the output transistors are, they still need protection against overload. The voltage drop across the emitter resistors R18 and

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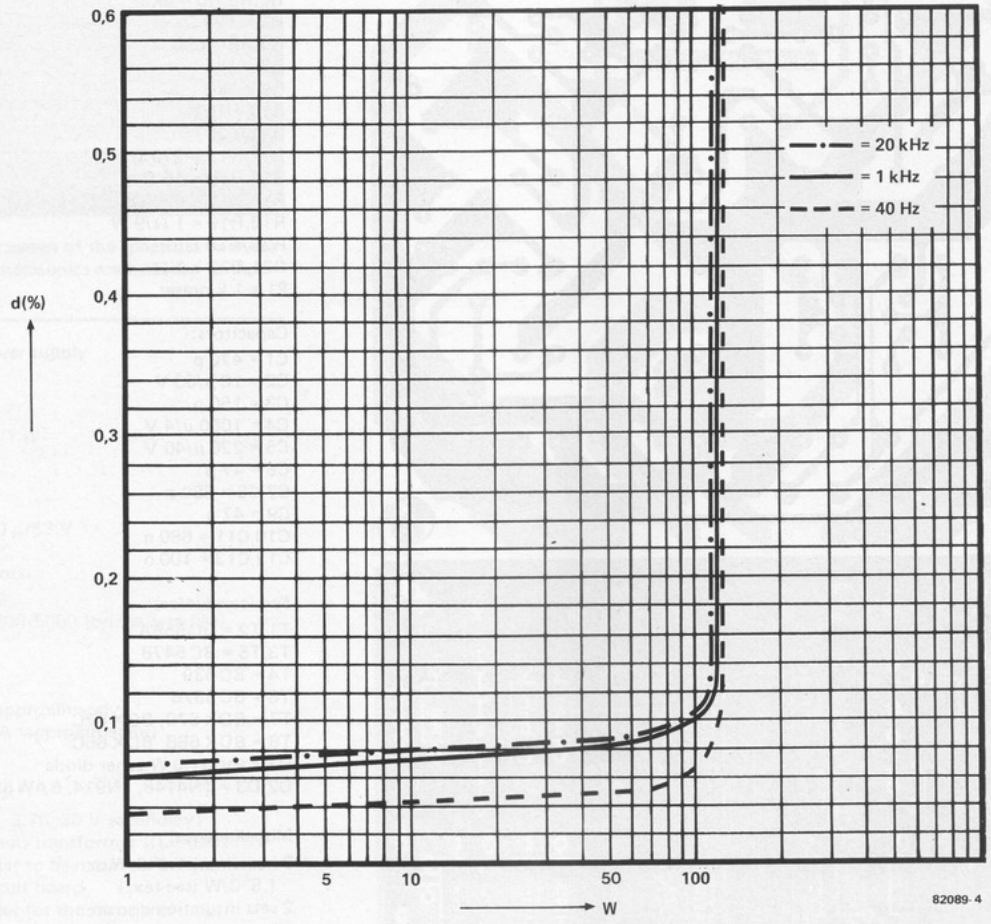

Figure 5. The graphs illustrate the high performance of the amplifier.

R19 is a measure of the output current. This means it can be used for current limiting. When the voltage drop across R18 and R19 is sufficiently high it will turn on T5 and T6 by way of the base voltage dividers R16/R14 and R17/R15. T5 and T6 will draw current via D2 and D3, thus limiting the base drive to T7 and T8.

The various little capacitors each serve an important purpose. C1 limits the input bandwidth which, as any audio enthusiast will tell you, is a good idea . . . . C3 causes the frequency response to roll off – it is 3 dB down at 100 kHz. C6, C7 and C8 ('Miller Capacitors') and R20 and C9 at the output all help to stabilise the circuit. C10/R21, C12, C11/R22 and C13 serve to suppress spikes and RF from the power supply.

Technical specification

The circuit is a straightforward, reliable design, and very few difficulties should be experienced during construction.

With a bit of luck the amplifier will deliver 120 W into a 4 Ω load, but unfortunately the distortion is approximately 1%. At 100 W (again into 4 Ω), the distortion is less than 0.1%. This power rating and distortion factor is more suitable for HiFi applications . . . . Table 1 shows the technical specifications of the amplifier. As figure 5 illustrates, the distortion factor remains virtually constant over the complete frequency range from 40 Hz to 20 kHz. It is less than 0.1% all the way!

For full modulation a minimum input of 0.775 V is required. Most modern preamplifiers supply approximately this output level. When using equipment that can produce a higher output, it is advisable to add a 10 k preset potentiometer at the input of the power amplifier.

The power supply

It is only a slight exaggeration to say that a power amplifier is only as good as its power supply. For this amplifier, a nominal supply voltage of ± 40 V is required. At full drive, 2.25 A is needed (100 W into 4 Ω) – or 1.1 A for 70 W into 8 Ω. For reasons of cost and simplicity, an unstabilised supply is normally used. By its very nature, if this delivers ± 40 V at full load, it will run up to a higher voltage as the current demand is reduced. However, the output devices are only 'safe' up to 100 V – corresponding to ± 50 V. To allow a safety margin, an off-load supply voltage of ± 46 V is preferred. This leaves only 6 V lee-way between off-load and full drive (over 2 A), so that a very low-impedance power supply is a must. A good way to achieve this is by using a good quality transformer . . .

Given a good mains transformer, a bridge rectifier and a few electrolytics are all that is needed to complete the power supply circuit. Fuses in both supply lines are a good idea, since the current limiting circuits in the output

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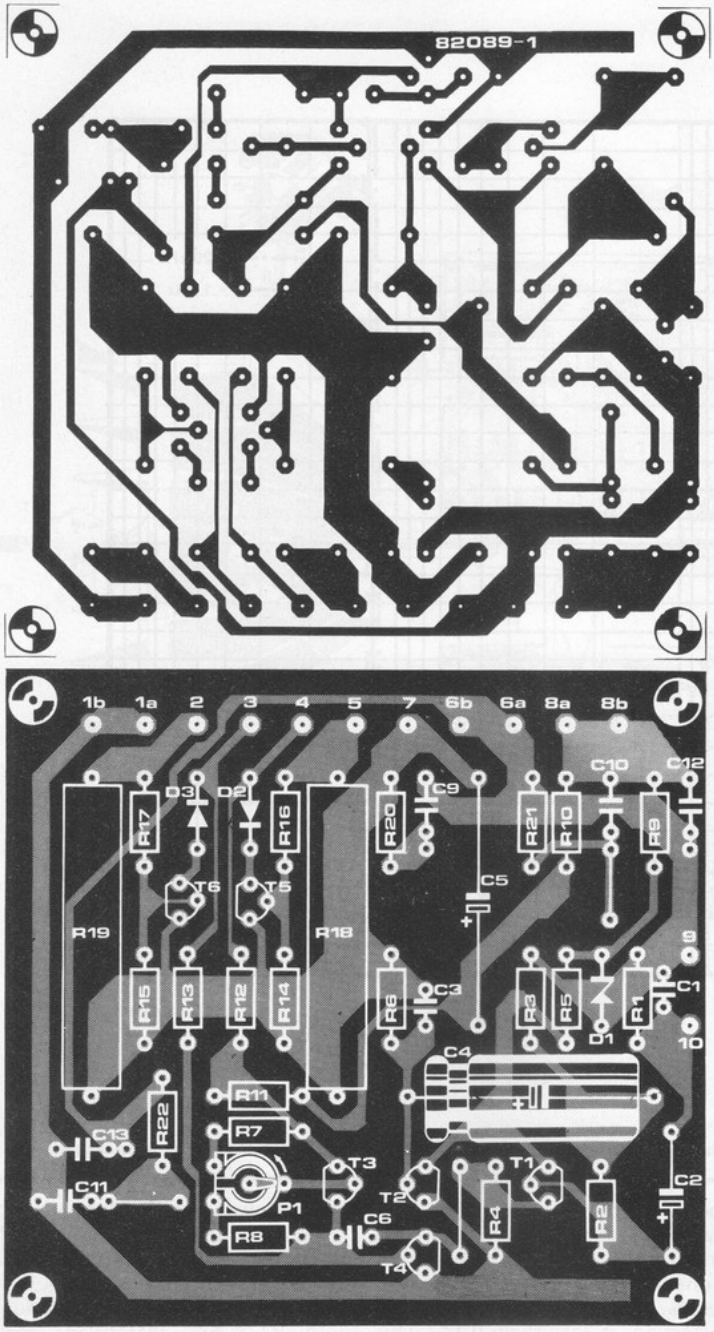

Figure 6. The copper track pattern and the component overlay of the amplifier printed circuit board.

Parts list, power amplifier

Resistors:
R1 = 120 k
R2,R5,R6 = 3k3
R3 = 120 Ω
R4,R8 = 680 Ω
R7 = 1k5
R9 = 5k6
R10 = 1k2
R11 = 2k7
R12,R13 = 270 Ω
R14,R15 = 15 Ω
R16,R17 = 220 Ω
R18,R19 = 1 Ω/9 W
R20 = 10 Ω
R21,R22 = 1 Ω
P1 = 1 k preset

Capacitors:
C1 = 470 p
C2 = 10 µ/63 V
C3 = 150 p
C4 = 1000 µ/4 V
C5 = 220 µ/40 V
C6 = 47 p
C7,C8 = 560 p
C9 = 47 n
C10,C11 = 680 n
C12,C13 = 100 n

Semiconductors:
T1,T2 = BC 556A
T3,T5 = BC 547B
T4 = BC 639
T6 = BC 557B
T7 = BDX 67B, BDX 67C
T8 = BDX 66B, BDX 66C
D1 = 9V1/1.3 W zener diode
D2,D3 = 1N4148, 1N914, BAW 62

Miscellaneous:
2 heatsinks, 1.2°C/W or 1.8°C/W (see text)
2 sets insulating disc etc. for power transistors

stage cannot guarantee 'permanent short circuit' protection. They only increase the chances of survival until the fuses 'blow'!
Two units are necessary for stereo, because the power supply will only cater for one power amplifier.

Construction

The printed circuit board is shown in figure 6. The emitter resistors R18 and R19, should be mounted at least 5 mm 'off' the board. This will allow good ventilation, so that heat can be dissipated freely.
The output transistors (T7 and T8) and the capacitors C7 and C8 are mounted 'off-board'. As shown in figures 3 and 4, each transistor (T7 and T8) and its capacitor (C7 and C8) should be mounted on a separate 1.2°C/W heat sink, such as a black SK 84 (see photo). Alternatively, if heat conductive paste is applied to both sides of the mica washer, then a 1.8°C/W, black SK 03 (100 mm) type should be sufficient. It is worthwhile noting that, when several transistors are mounted on a single heatsink, the thermal resistance must be divided by the total number of transistors. Therefore if T7 and T8 (with or without heat conductive paste) are on one heatsink, it must be either a 0.6°C/W (SK 84) or a 0.9°C/W (SK 03) type.
Under no circumstances should the case or the connections of the power transistors come into contact with the heat sinks, as this would cause a 'short'. Be reminded that the case of the transistor is the collector. As a matter of interest, insulating caps for power transistors are available.
When connecting C7 and C8 as shown in figure 4, ensure that their leads are insulated. The connections to the printed circuit board are made with thin copper wire and should be kept as short as possible. It is common knowledge that DIN sockets are unreliable, so the use of good Japanese HiFi spring terminal blocks is advised for the output.
Use screened AF cable to connect the input socket to the printed circuit board (see figure 4). The most convenient point to connect the ground of the amplifier and earth of the case, is the ground connection of the input socket. The cable and the input socket should be mounted as far away as possible from the other components and wiring. This is necessary, in order to reduce the

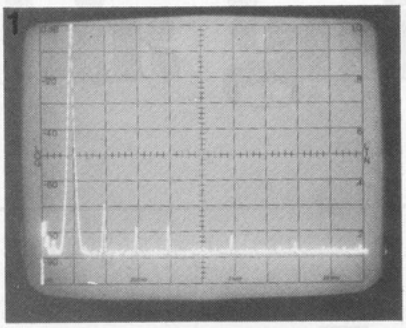

Photo 1. The screen of the spectrum analyser shows which harmonics are included in the distortion.

Parts list, power supply

Resistors:
R1,R2 = 3k3/1 W

Capacitors:
C1 = 100 n
C2,C3 = 4700 µ/63 V

Semiconductors:
D1,D2 = LED
B1 = B80C3200/5000 (bridge rectifier)

Fuses:
F1 = 1.4 A (approximately)
F2,F3 = 2.5 A (approximately)

Miscellaneous:
2 x (225 VA, 3.75, 30 V secondary) toroidal mains transformer (ILP 62017)
2 x fuse holder to be mounted on the printed circuit board
1 x fuse holder for the rear panel
S1 = double pole mains switch

possibility of feedback and hum.
The two secondary windings of the transformer are totally separate. This leaves four unmarked connection wires to play with. In order to find out which is which, simply join up any two of the four and measure the voltage across the other two. If this is found to be 60 V AC, the joined wires must be connected to the ground of the power supply, and the other two to the remaining connections. Should 0 V be registered, then the wires should be swapped over.
The electrolytic capacitors C2 and C3 should be securely attached to the board by means of plastic cable fasteners. This will prevent the terminal leads from snapping off (see photo).
The connection wires between the printed circuit board and the loudspeaker socket or terminal are laid along the sides of the case and away from everything else, to reduce the chance of feedback.

Setting up the amplifier

Make sure there is nothing connected to the output, 'short' the input and remove

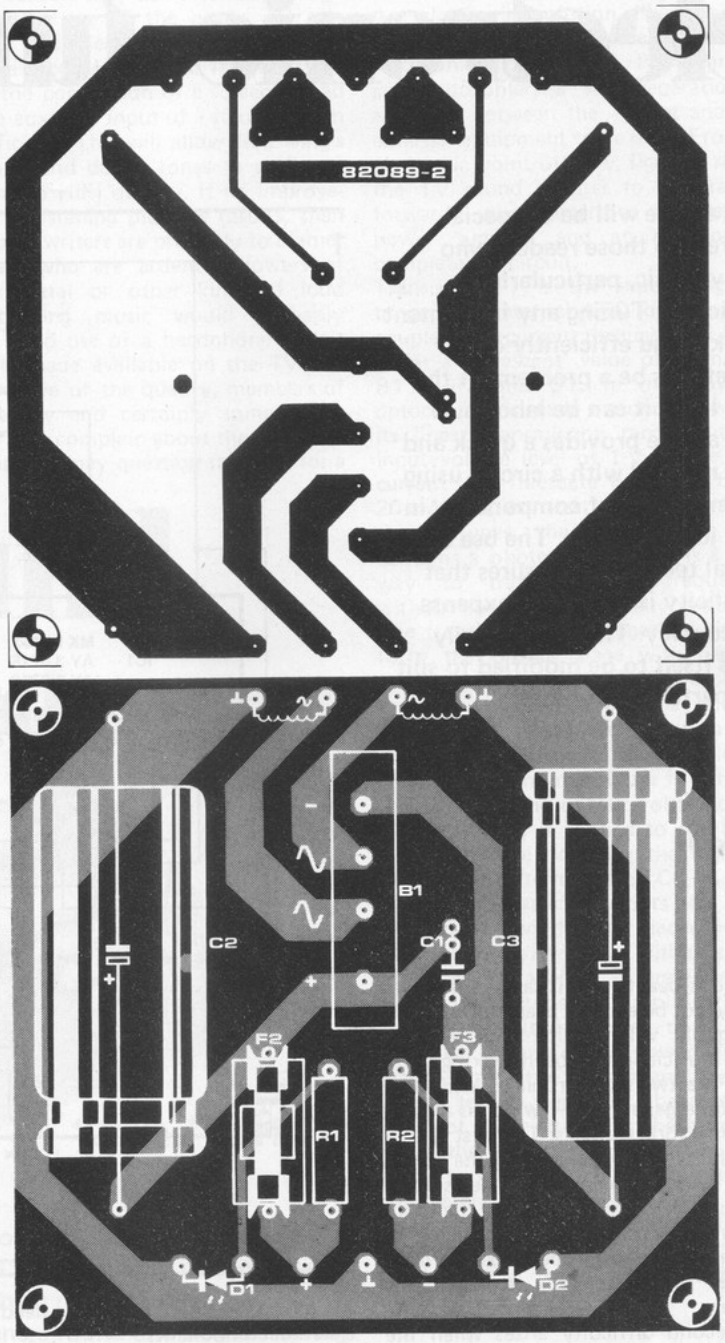

Figure 7. The copper track pattern and component layout of the power supply board.

the fuse F2 from the power supply circuit. Then set a multimeter to the 1A DC current measurement range and connect it to the terminals of the fuse holder (+ terminal of the meter, to C2/ fuse junction).
Turn P1 fully anti-clockwise. Check all the connections and switch on the mains supply. The multimeter needle should hover around 0 A. If a higher current is indicated switch off immediately, as there must be something wrong! Provided only a few milliamps are flowing through the circuit, the meter may be reset to the 100 mA range and P1 adjusted to give 80 mA. About 50 mA quiescent current should then be flowing through the output transistors.
This completes the setting-up procedure. Replace the fuse F2 (switch off the supply voltage first!). If there are any problems, readers will be able to track down the error quickly by comparing their voltage readings to the DC voltage values indicated in the circuit diagram. In the prototype all the voltages were measured with the input shorted out and the circuit connected to a loudspeaker.

electronic tuning aid

This article will be of special interest to those readers who enjoy music, particularly musicians. Tuning any instrument quickly and efficiently can sometimes be a problem, at the very least, it can be laborious. This article provides a quick and easy method with a circuit using the minimum of components, in fact, just three ICs. The use of digital technology ensures that simplicity is not at the expense of accuracy. The circuit easily lends itself to be modified to suit any particular purpose.

S. Akkal

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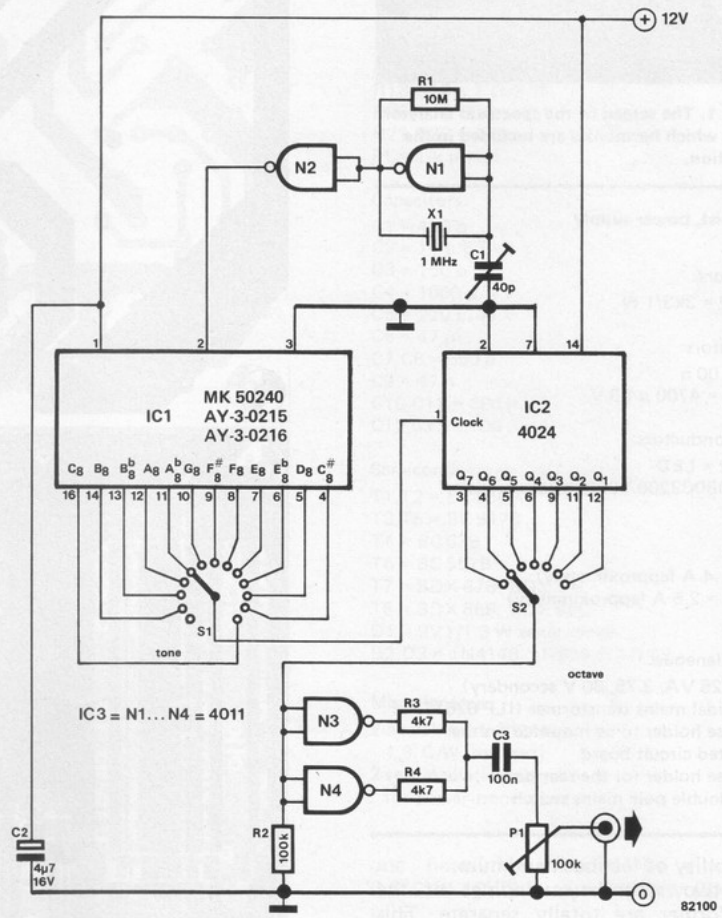

Simple is beautiful it is said. In this case it may not be exactly beautiful, but this tuning aid will provide what a great many musicians have been looking for.

There are two main problems associated with tone generators — which is all that a tuning fork really is. The first is that of stability. It is obvious that the instrument being tuned can only be as accurate as the tuning source and therefore the circuit must produce the same F# in a month's time as it does today. A large number of components increases this problem.

The second difficulty arises when the tuning source provides a number of notes. The relationship between them must of course be fixed and they must also remain stable. A look at the circuit diagram in figure 1 will show that the number of components could hardly be any less. All the available tones are derived from a 'master' oscillator (or frequency generator). This is formed by two gates, N1 and N2, and is crystal controlled for greater accuracy. This effectively takes care of the stability and long term accuracy problems. The use of a crystal keeps drift to an absolute minimum. The oscillator frequency can be trimmed by means of the variable capacitor C1.

The oscillator frequency is fed to pin 1 of the master tone generator IC1. This will provide the complete set of 13 notes of an octave without any need for external components.

A 1 MHz crystal will provide a frequency at pin 16 of 2092.0502 Hz for C_8. It is worth considering the complexity of a circuit required to do this little job before the appearance of LSI ICs.

It is a simple matter to select any one of the outputs with the aid of a switch, S1 in this case. However, we still finish up with just any one note of one octave. This may satisfy many requirements, but it would be very useful to be able to select any one of the number of octaves as well.

Fortunately this can be accomplished quite simply. The wiper of switch S1 is fed directly to the clock input of a 7 stage counter, IC2. The 7 outputs of this IC provide us with any one of seven outputs — seven octaves in fact.

All that remains of the circuit are the gates N3 and N4 and the surrounding components. The two gates are connected in parallel and act as buffers for the output. Potentiometer P1 is used to adjust the output level.

For precise calibration a frequency counter is needed. This is connected to the output of N2 and C1 is adjusted for a reading of 1.00012 MHz. However, in reality the difference between this figure and 1 MHz is so small that it can be ignored. Although originally intended as a tuning aid, the circuit can have many other uses. For specific purposes one or even both switches may be dispensed with, and one or a few specific tones can be 'hard wired'. For instance guitarists will require E, A, D, G, B and E. A six way switch with 'tappings' at the right outputs will provide this very easily.

TV sound interface

'Dallas' in HiFi?

In certain countries TV sets capable of producing 'stereo' sound are fast becoming available. The majority of TV sets already in home use (there are exceptions) produce a sound which may require improvement. With this in mind our designers found one way of solving the problem. They have produced a simple, relatively low cost device which helps to enhance the original sound. By doing so, it is hoped that even the most critical of viewers will be pleased.

Some readers may be fortunate enough to possess one of the newer TV sets already equipped with headphone and/or tape recorder sockets. If that is the case, the connection of a screened lead to the auxiliary input of a stereo system is sufficient. This will allow JR Ewing's intrigues and dulcet tones to achieve a reasonable HiFi quality. If no improvement in listening pleasure results, then the script writers are probably to blame. Readers who are ardent followers of heavy metal or other kinds of loud head-bashing music would probably make good use of a headphone socket if it is made available on the TV set. Irrespective of the quality, members of the family and certainly some neighbours may complain about the quantity. TV viewers may question the need for a circuit. To many of them a straightforward method is to connect a socket in parallel with the speaker. At first sight this may seem plausible. But unfortunately, as the chassis of a TV set is normally connected to the mains supply, the application of such a solution would be hazardous to the health of tape recorders or HiFi equipment.

The fitting of an isolation transformer can prove to be rather costly (especially if fitted by an expert). Another disadvantage is that the use of a transformer would add noise and distortion to the output signal.

An electronic solution like the one described here would seem to be a worthwhile compromise: By means of an optocoupler, a safe separation is achieved, between the TV set and any external equipment to be used. From an electronic point of view, figure 1 shows the TV sound adapter to be straightforward, two separate symmetrical power supplies and an optocoupler complete the circuit.

Transistor T1 is the input stage to trigger the internal LED of the optocoupler. The current through the LED is set at a 'quiescent' value of 18 mA via R1 . . . R3 and D1. In this way the optocoupler is made to function within its linear transmission range. With an input voltage level of 1 V_{pp}, the LED current will fluctuate between 16 and 20 mA. In contrast to the cheaper, slower types, the optocoupler used, contains a photo diode: This is a good way to transmit high frequencies without incurring too many problems. The transistor in IC3 together with T2 form the output stage with negative feedback via R6 and R7. The base bias for T2 is set with R4. The value of resistor R5 is selected so that the output stage can be driven to near maximum, thereby ensuring the circuit is not overloaded when the output voltage of the TV final stage is applied to the input. The amplitude drop for the high frequencies is determined by C6, in other words, this capacitor limits the transmission bandwidth. Any reader wishing to do so may experiment with this value in order to achieve a preferred frequency characteristics. Amplification of the TV sound is set at a gain of 1.

Although the use of two power supplies may seem a little extravagant, they are found to be necessary, because the input of the circuit must be separated from the output. Two mains transformers or one transformer with two completely separated secondary windings are therefore required. Finally, to achieve the object of the exercise, a good quality transformer should be used.

Construction and application

The layout for the printed circuit board of the TV sound interface is shown in figure 2. With the exception of the transformer, the mains switch and fuse, all components will fit on the board. Before mounting the circuit into the TV set, a few checks to ensure correct construction should be made. Prior to mounting the optocoupler measure the operating voltage. Mount the optocoupler. Connect an audio signal to the input, and check that the output signal is of the same value: The circuit is now ready and can be inserted into the TV set.

The circuit as described has an input impedance of 1 kΩ and was specifically designed for connection in parallel to a

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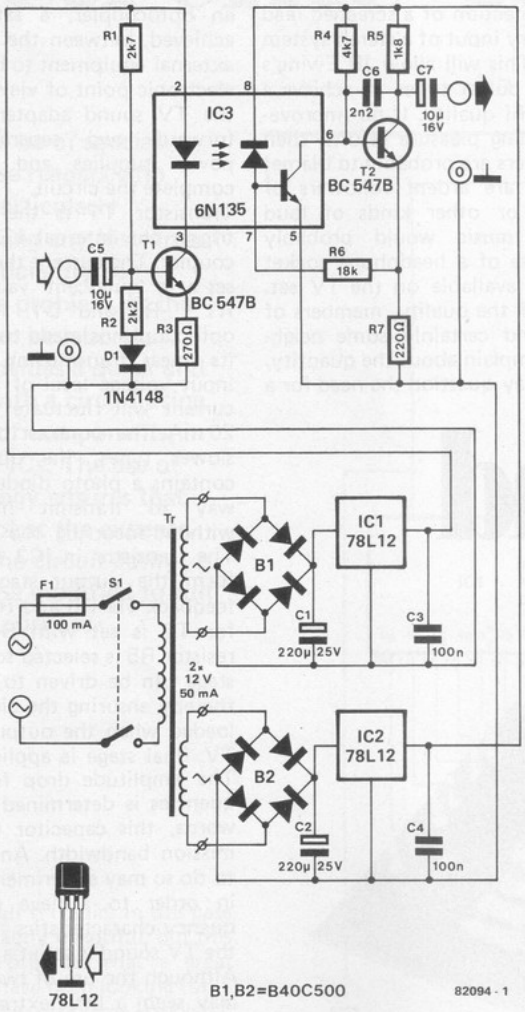

Figure 1. The circuit diagram consists mainly, of a fast opto coupler and two separate power supplies. This ensures that the audio signal can be taken from the set 'safely'.

Table 1

Technical data of the prototype
Distortion and signal to noise ratio at various input levels (f = 1 kHz and 10 kHz)

U_{in} (V_{pp})	d (%)	S/N (dB)
0.06	< 0.1	60
0.3	0.06	72
1.5	0.25	> 85
5	0.85	> 85

amplification: 1x (0 dB)
input resistance: 1.3 kΩ or 100 kΩ (see text)
frequency bandwidth:
< 10 Hz . . . 23 kHz (−3 dB)
maximum output level: 6 V_{pp}

Parts list

Resistors:
R1 = 2k7
R2 = 2k2
R3 = 270 Ω
R4 = 4k7
R5 = 1k8
R6 = 18 k
R7 = 220 Ω

Capacitors:
C1, C2 = 220 µ/25 V
C3,C4 = 100 n MKT
C5,C7 = 10 µ/16 V
C6 = 2n2 MKT

Semiconductors:
B1,B2 = B40C500
D1 = 1N4148
T1,T2 = BC 547B
IC1,IC2 = 78L12
IC3 = 6N135 (Hewlett-Packard)

Miscellaneous:
S1 = dp mains switch
F1 = 100 mA slow miniature fuse
Tr = 2 x 12 V/50 mA mains transformer

TV loudspeaker. If 220 k resistors are substituted for R1 and R2 and a BC 517 transistor for T1, an input impedance of 100 kΩ is achieved. Together with the further addition of a potentiometer (50 k log) to the output (to vary the output level), the circuit becomes quite versatile.

With a few minor modifications (if necessary), it can be applied to any situation where isolation from the mains is required. It can be applied easily and successfully to AF circuits to control strobes and optical/lighting effects.

In practice there are two ways of connecting the circuit to the TV. The first is shown in figure 3a, in parallel to the speaker (R_L). When switched off (by means of S2) the connection is made across R ($R = R_L$).

Most loudspeakers have their resistance values indicated on the chassis. Should no markings be found, then a TV circuit diagram would be useful. Fortunately most loudspeakers fitted fall into the 4 to 16 Ω region, but occasionally a high impedance of 25 Ω or more may be found. Should this be the case, then the TV volume control will have to be set low to counteract the rather high output level. The problem of the control setting, although not a major one, could prove to be inconvenient. A simple remedy is to connect a voltage divider or preset before the input of the circuit.

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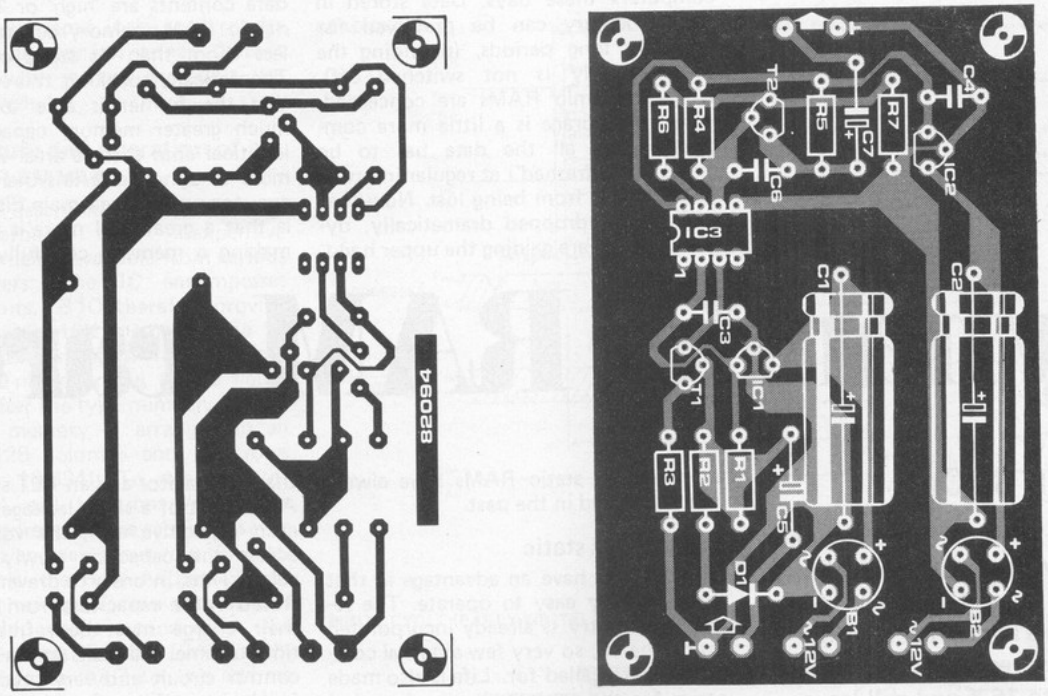

Figure 2. The track pattern and component overlay of the printed circuit board. This circuit forms the interface between the TV set and HiFi equipment, a headphone-amplifier or a tape recorder.

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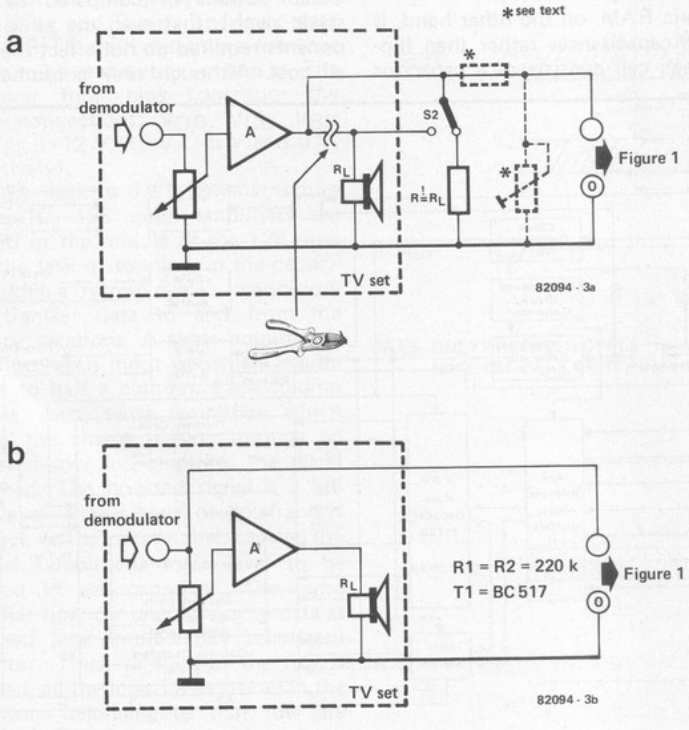

Figure 3. The internal loudspeaker can be switched on and off via switch S2. Resistor R_L then becomes the load for the TV audio stage A. Figure 3a provides details of the connections via a voltage divider or preset. Figure 3b illustrates the connection to the output of the demodulator and in this case, some form of external volume control is required.

The second possibility (figure 3b) is to eliminate the audio power amplification stage of the TV altogether, by connecting the circuit directly to the demodulator output. In other words the 'live' and earthed terminals of the TV volume potentiometer are connected to the input and ground of the circuit. Normally, setting the volume control to zero will silence the TV loudspeaker, but obviously if it continues to emit any unwanted sound then it can be switched off by using S2 (see figure 3b). One side effect of connecting the circuit to the demodulator output is that the TV volume potentiometer will now not be able to control the level of the external speaker. As there are many variations in TV circuit design, a brief study of the TV circuit diagram (if possible) would be advisable, certainly before contemplating any further modifications.

With the use of a multimeter it will not be possible to ascertain accurately whether the earth (ground) of a TV set is connected to the mains, because irrespective of how unsophisticated the TV power supply may be, it will always contain a few diodes and rectifiers. The only sure way to find out is to take a close look at the circuit diagram. But as a generale rule; if the TV set has no headphone/tape-recorder or auxiliary speaker socket then it should be assumed that the ground is connected to the mains supply.

Static and dynamic RAMs are playing an increasingly important role in home computers these days. Data stored in static memory can be preserved for relatively long periods, (providing the power supply is not switched off). Where dynamic RAMs are concerned, long-term storage is a little more complicated, as all the data has to be renewed ('refreshed') at regular intervals to prevent it from being lost. Now that prices have dropped dramatically, dynamic RAMs are gaining the upper hand, even though static RAMs have always been preferred in the past.

dynamic RAM card

16 K in 8 ICs

Dynamic RAMs are so economical these days that it is worthwhile to use them instead of static RAMs, despite the additional control electronics required. Eight ICs can store up to 16 K and still leave plenty of room on the Eurocard for the control logic. Further advantages include low current consumption and high-speed access times. Computer owners who are running out of memory and space will welcome this opportunity to extend their RAM facilities.

Dynamic vs static

Static RAMs have an advantage in that they are very easy to operate. The required circuitry is already incorporated inside the IC, so very few external components are called for. Life is also made easier for the operator by the fact that no timing problems are involved as long as IC types are selected for the right speed to cope with the application in hand.

A static RAM memory cell consists of a sort of set/reset flipflop, which contains at least 5 or 6 transistors. As readers can imagine, a complete RAM IC has an immensely complex structure.

A dynamic RAM, on the other hand, is based on capacitances rather than flipflops. Each cell consists of a capacitor and an FET switch. The voltage across the capacitor determines whether the data contents are 'high' or 'low'. A dynamic RAM memory cell takes up far less room than its static counterpart. Theoretically speaking, this would mean that the former is able to provide a much greater memory capacity on an identical chip surface area. But there is more to dynamic RAMs than meets the eye, for one of their main disadvantages is that a great deal more is involved in making a memory cell fully operative than a capacitor and an FET switch.

As a result of a slight leakage current in each capacitive unit, the voltage level across the capacitor slowly drops in value. Thus, in order to prevent the data stored in the capacitors from being lost, their charge must be refreshed from time to time. This calls for an additional control circuit and very precise timing for the operation to pass off smoothly.

That is not the only problem. An awful lot of memory cells can be integrated on a single chip and so addressing is rather complicated. Dynamic RAM manufacturers have tried to solve this by using a multiplexed address bus, (yet another addition to the circuitry).

Nevertheless, dynamic RAMs are so cheap nowadays, (compared to their static rivals), that even the extra components required do not affect the overall cost. Although they consume very

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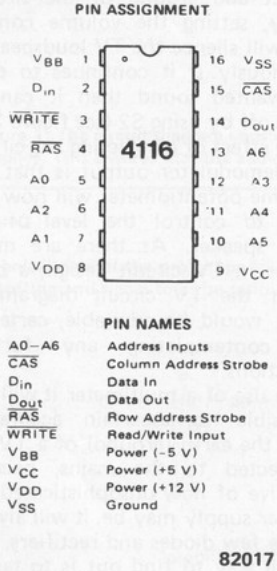

Figure 1. The pin assignment of the dynamic RAM IC 4116. Note that it requires three supply voltages, and that its current consumption is fairly low.

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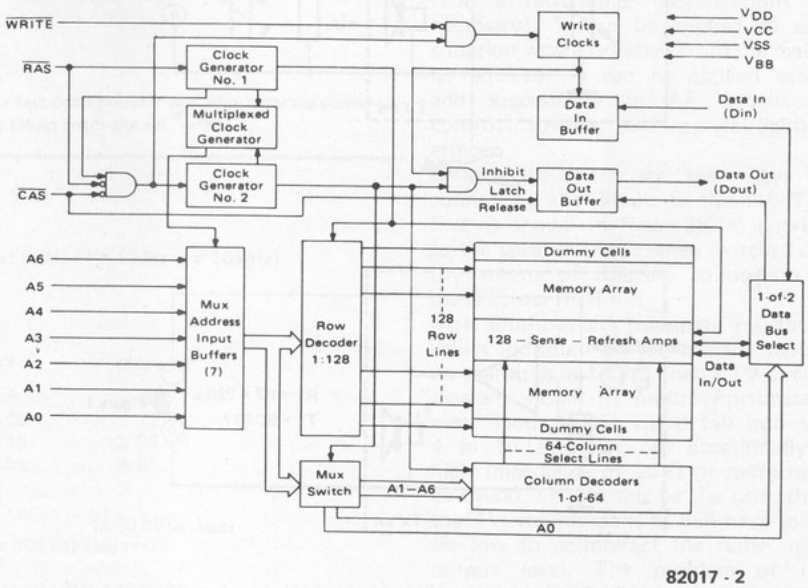


Figure 2. Block diagram of the 4116. Its memory capacity is distributed among 128 columns. Sense amplifiers are located between the rows.

little current, the dynamic RAMs used here do need three separate supply voltages.
All things considered, if the same results can be obtained for less money, there is no reason why readers shouldn't use dynamic RAMs.

The structure and operation of a dynamic RAM chip

The design described in this article is centred around the inexpensive 4116 IC, which is available from various manufacturers. The IC encompasses 16384 x 1 bits. 8 ICs therefore provide an 8 bit wide 16K memory. The IC series has access times, ranging from 150 . . . 300 ns according to the figure indicated after the type number.
The 4116 memory is arranged in an array of 128 columns and 128 rows (128 x 128 = 16,384). To decode 1 of the 16,384 cell locations within the 4116, 14 address bits are required, seven per column and seven per row. An integrated clock, the Row Address Strobe ($\overline{RAS}$) latches the 7 row address bits into the chip and a second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. In other words, the 7 address inputs are multiplexed. The pin assignment for the 4116 is shown in figure 7. A negative pulse at the $\overline{RAS}$ input 'reads in' data in the form of a row address into the address inputs and a negative pulse at the $\overline{CAS}$ input reads in the data as a column address. As the memory is only one bit wide, only one data input and one data output are required (D_{in} and D_{out}). The logic state of the $\overline{WRITE}$ input determines whether a bit is to be read out or written in. The remaining four pins constitute the supply connections: V_{DD}, V_{CC}, V_{BB} and V_{SS} (+12 V, +5 V, −5 V and 0 V, respectively).
To come back to the internal structure of the IC, 128 sense amplifiers are situated in the middle of the 128 rows with the task of topping up the capacitors during a 'refresh cycle'. In addition, they transfer data to and from the memory locations. A sense amplifier is a flipflop, each input of which is connected to half a column. Each column has its own sense amplifier which detects the charge passing through an addressed row and amplifies the signal produced. The boosted signal is a full logic level, either 'high' or 'low' and is fed back to the column line, causing the original (amplified) logic level to be restored in the capacitor. The sense amplifier now contains the same data as the read (and immediately rewritten) capacitor. Thus, as soon as the row is accessed, all the logic levels stored in the capacitors belonging to that row are refreshed. To give you an idea of the capacitance level involved: a 4116 storage capacitor has a value of about 0.04 pF!
The order in which the different signals have to be applied is as follows:

3

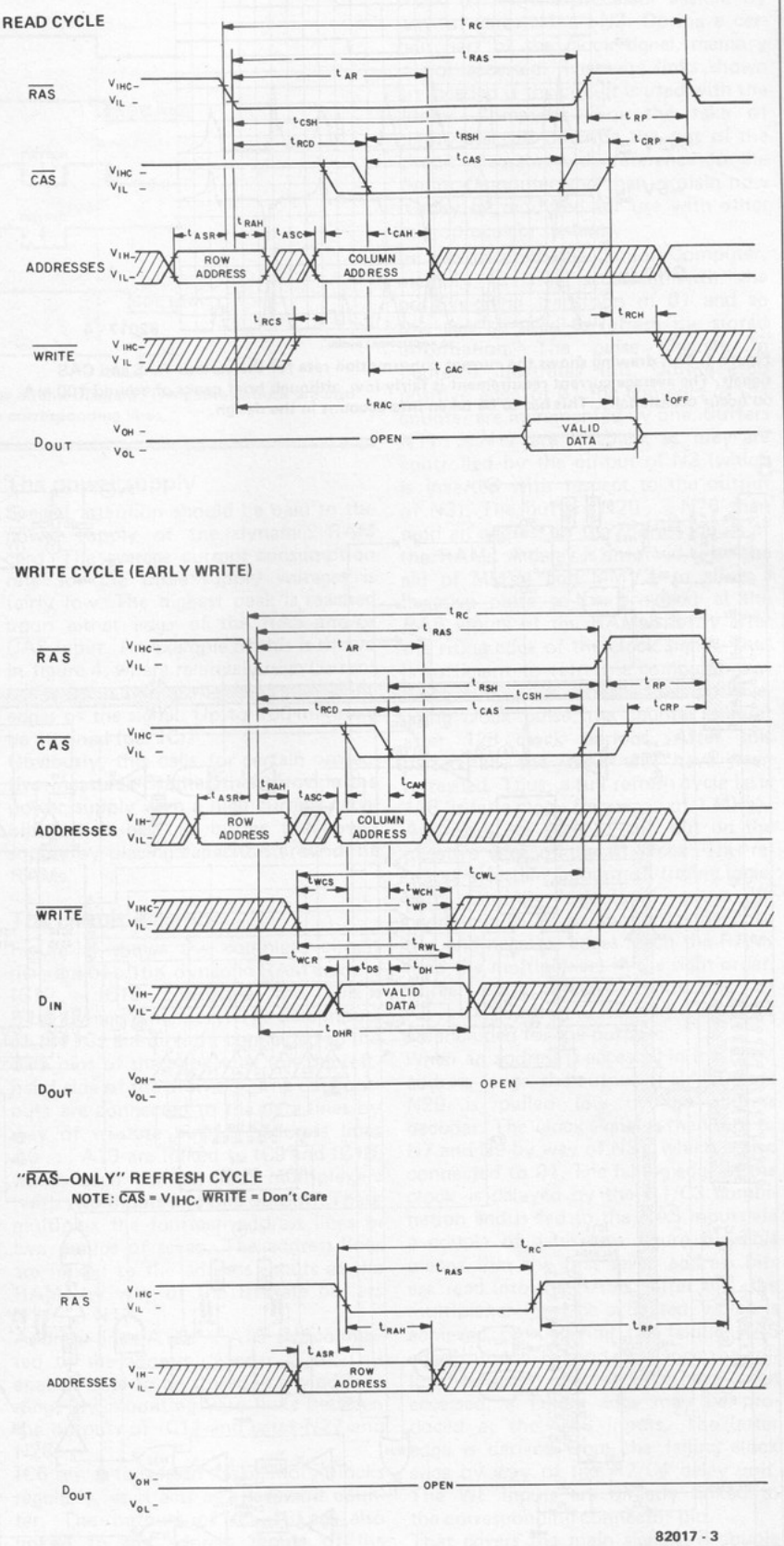


Figure 3. Time sequence charts for reading, writing and refreshing the 4116. No specific times are given here, because they depend on the speed of the host processor. All times are in the nanosecond range.

4

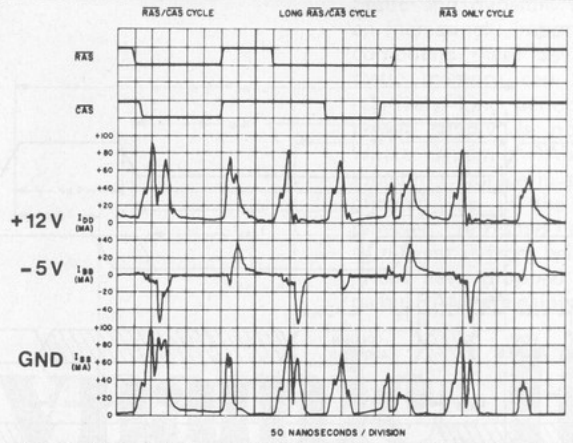


Figure 4. This drawing shows the current consumption rate for the various RAS and CAS signals. The average current requirement is fairly low, although brief peaks of around 100 mA do occur occasionally. This has to be taken into account in the design.

Data is read out of a memory location, a seven bit address being stored at the address inputs beforehand. Then a pulse is generated at the $\overline{RAS}$ input. The row address must be available for a certain amount of time, after which the seven bit column address can be produced. This is followed by a pulse at the $\overline{CAS}$ input. The column address must also be present for a certain minimum period. An internal output buffer then sends the logic level of the selected address bit to the data output. During this procedure the $\overline{WRITE}$ input must be high.

Virtually the same principle applies to write operations, only now the data input is initially provided with a logic level and the $\overline{WRITE}$ input goes low. The time sequence chart in figure 3 illustrates these events in the form of a graph.

5

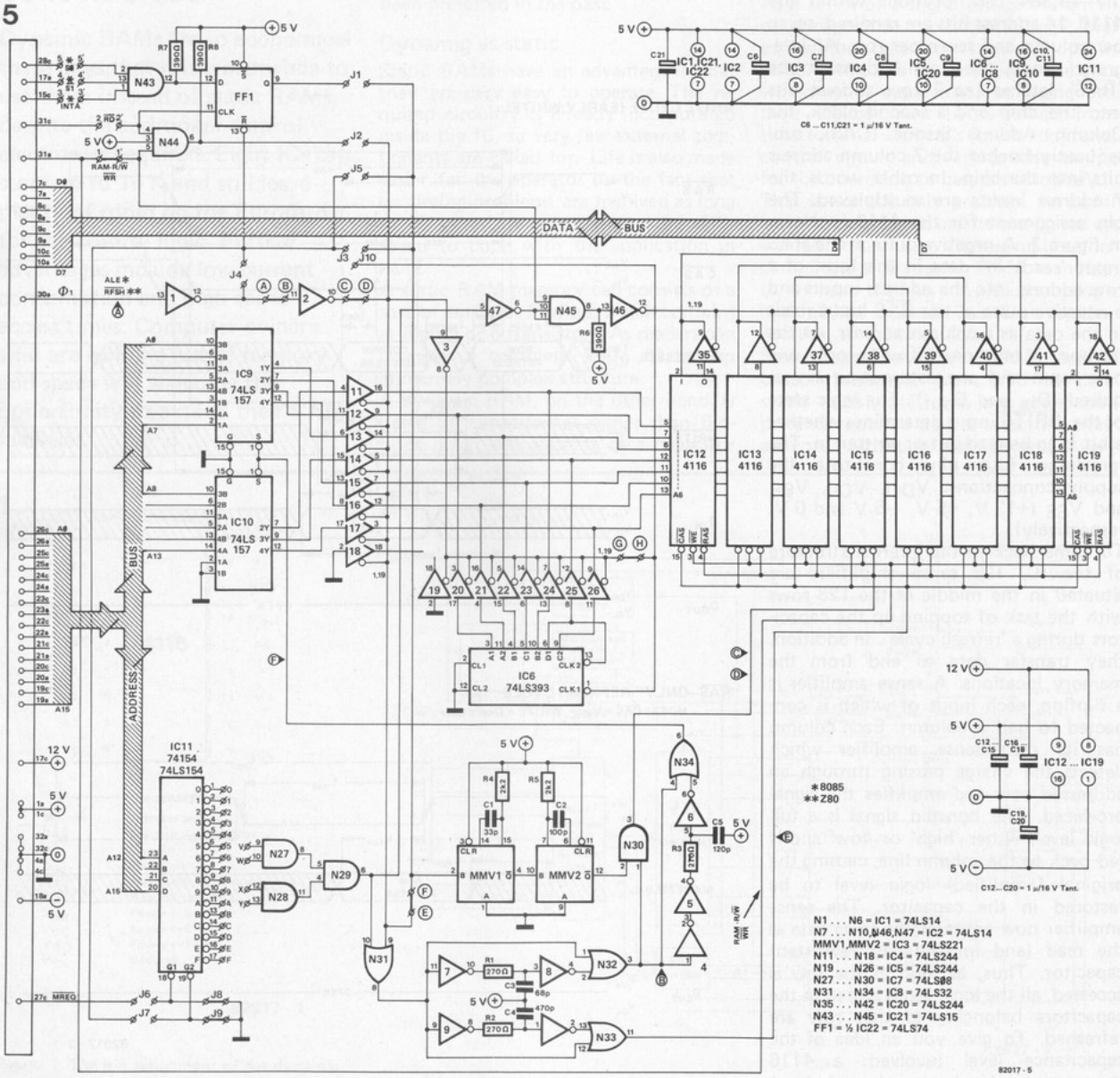


Figure 5. The dynamic RAM circuit diagram. Using wire links the card may be adapted to different microprocessor systems.

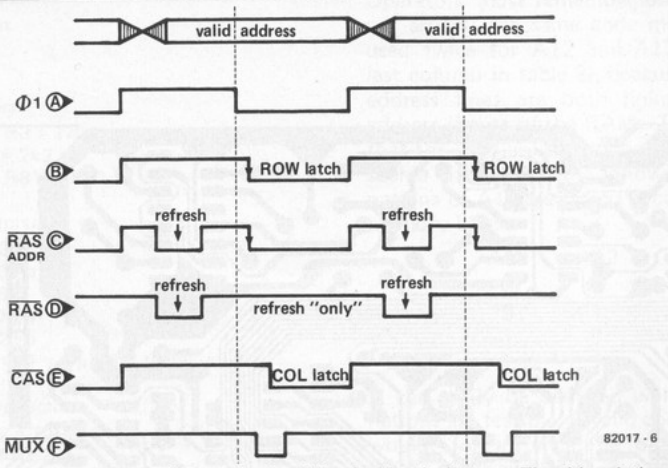


Figure 6. The waveforms of the main signals in the circuit diagram. The abbreviations are also indicated in the circuit diagram together with the corresponding lines.

The refresh cycle

As mentioned earlier, using capacitors to store digital information has a number of advantages, but there is also another side to the coin. Slowly but surely, this type of capacitor loses its charge *and* the stored logic level. This is why it is necessary to refresh the level from time to time. In the case of the 4116 this must be done every two milliseconds, which is quite reasonable, considering its low cell capacitance.

Fortunately, the refresh operation is relatively straightforward, thanks to the structure of the IC, in which the 'sense' amplifiers are situated in the direct vicinity of the cells. The sense amplifiers, as has already been seen, boost the logic levels in the memory cells. When a row address is read in after the computer has generated a $\overline{RAS}$ pulse the entire row of 128 bits is read into the sense amplifiers. At the same time, the logic levels are amplified and written back into the 128 row capacitances. In other words, once a row address and an $\overline{RAS}$ pulse have been produced, the 128 bits are refreshed. As long as this method ensures that the whole operation is executed within 2 milliseconds, data stored inside the IC will remain intact.

Of course, the refresh cycle may be shorter than 2 milliseconds, if necessary. This particular RAM card was designed to be used with the Junior Computer, or a similar microprocessor, with a clock frequency of 1 MHz. This means the refresh cycle for 128 rows takes 128 μs.

The timing

Figure 3 contains the time sequence charts for the read, write and refresh cycles, respectively. The diagrams clearly show the order in which the various signals must be provided. Different times are involved and this will have to be taken into account. No specific values are indicated, as they vary somewhat per IC type and manufacturer.

The power supply

Special attention should be paid to the power supply of the dynamic RAM card. The average current consumption rate for the three supply voltages is fairly low. The highest peak is reached upon either edge of the $\overline{RAS}$ and/or $\overline{CAS}$ input. An example of this is shown in figure 4, where relatively high current peaks occur during the rising and falling edges of the signal. Up to 100 mA may be attained (per IC)!

Obviously, this calls for certain protective measures. Rather than provide the power supply with a high current capability it is best to buffer the power supply by placing capacitors around the RAMs.

The circuit diagram

Figure 5 shows the complete circuit diagram of a 16K dynamic RAM card.

IC12 . . . IC19 constitute the 16K x 8 bit dynamic memory. The data inputs of the ICs are directly connected to the data pins of the connector (on the left-hand side of the drawing). The data outputs are connected to the data lines by way of tri-state buffers. Address lines AØ . . . A13 are linked to IC9 and IC10, which each contain four multiplexers (with two inputs and one output). These multiplex the fourteen address lines in two groups of seven. The address lines are linked to the address inputs of the RAMs by way of the tri-state buffers N11 . . . N17.

Address lines A12 . . . A15 are connected to the address decoder IC11. This enables data to be stored in any address range by mounting wire links between the outputs of IC11 and gates N27 and N28.

IC6 serves to refresh the memory blocks regularly, as it acts as a seven-bit counter. The outputs of the IC are also linked to the address inputs of the RAMs by way of tri-state buffers (N20 . . . N26). The refresh cycle takes place during the period that the processor is not using the address bus. The clock input of the counter IC6 and the control inputs of the tri-state buffers, N20 . . . N26, are connected to the clock Ø1 of the processor system by way of gates N1 . . . N3. During a certain part of the clock signal, memory is not accessed. The wire links shown are needed if the circuit is used with the Junior Computer. For the sake of clarity we will describe the rest of the circuit diagram with reference to the Junior Computer and then explain how it may be modified for use with other microprocessor systems.

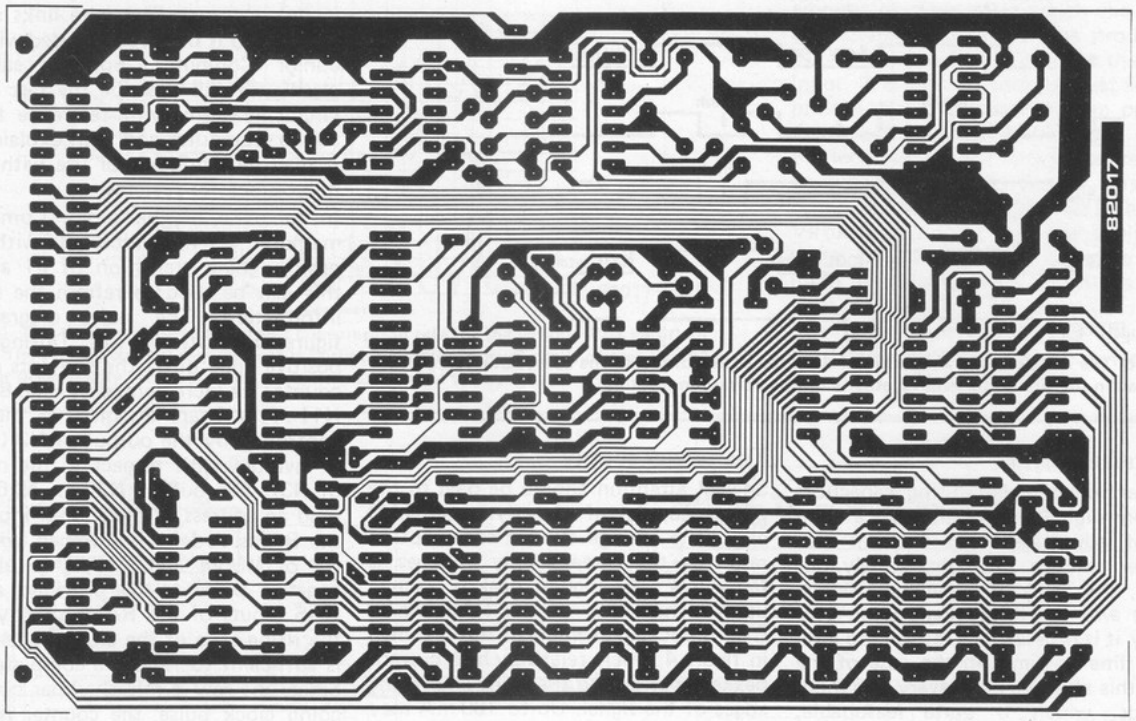
In the case of the Junior Computer, memory is not accessed with the positive-going transition of Ø1 and so this can be used to refresh the stored information. The pulse diagram in figure 6 illustrates this. During each positive edge of Ø1 the contents of the counter are incremented by one. Buffers N11 . . . N17 are disabled, as they are controlled by the output of N2 (which is inverted with respect to the output of N3). The buffers N20 . . . N26 then send an address to the address inputs of the RAMs. A delay is enforced, with the aid of MMV1 and MMV2, to allow a negative pulse to be provided at the $\overline{RAS}$ inputs of the RAMs shortly after the rising edge of the clock signal. That is sufficient to refresh a complete row. Since one row is refreshed per positive-going clock pulse, the counter is reset after 128 clock periods. After this period all the rows will have been refreshed. Thus, a full refresh cycle lasts 128 μs (at a clock frequency of 1 MHz).

Addresses are read in and out on the negative edge of the Ø1 clock. This requires a certain amount of 'timing logic' with carefully calculated values (in nanoseconds) to be sure that the positive and negative edges reach the RAMs (and the multiplexer) in the right order. Three pulse 'delays' consisting of N4 . . . N10, R1 . . . R3 and C3 . . . C5 are included for the purpose.

When an address is accessed in the RAM address range, the output of NAND gate N29 is pulled low by the address decoder. The clock signal is then sent to N7 and N9 by way of N31, which is also connected to Ø1. The falling edge of the clock is delayed by the R1/C3 combination and is fed to the $\overline{RAS}$ inputs via a couple of gates (see figure 6). This means that the first seven address bits are read into the RAMs. After this, the multiplexer must be activated, which is achieved by delaying the falling RAS edge through R3 and C5. Once the following seven address bits have been accessed, a falling edge may be produced at the $\overline{CAS}$ inputs. The latter edge is derived from the falling clock edge by way of the R2/C4 delay unit. The $\overline{WE}$ inputs are directly linked to the corresponding connector pin.

That covers the main signals. A couple of gates and a flipflop are shown in the top left-hand corner of the circuit diagram. These simply serve to adapt the various signals to make them 'digestible' for processors other than the 6502.

7



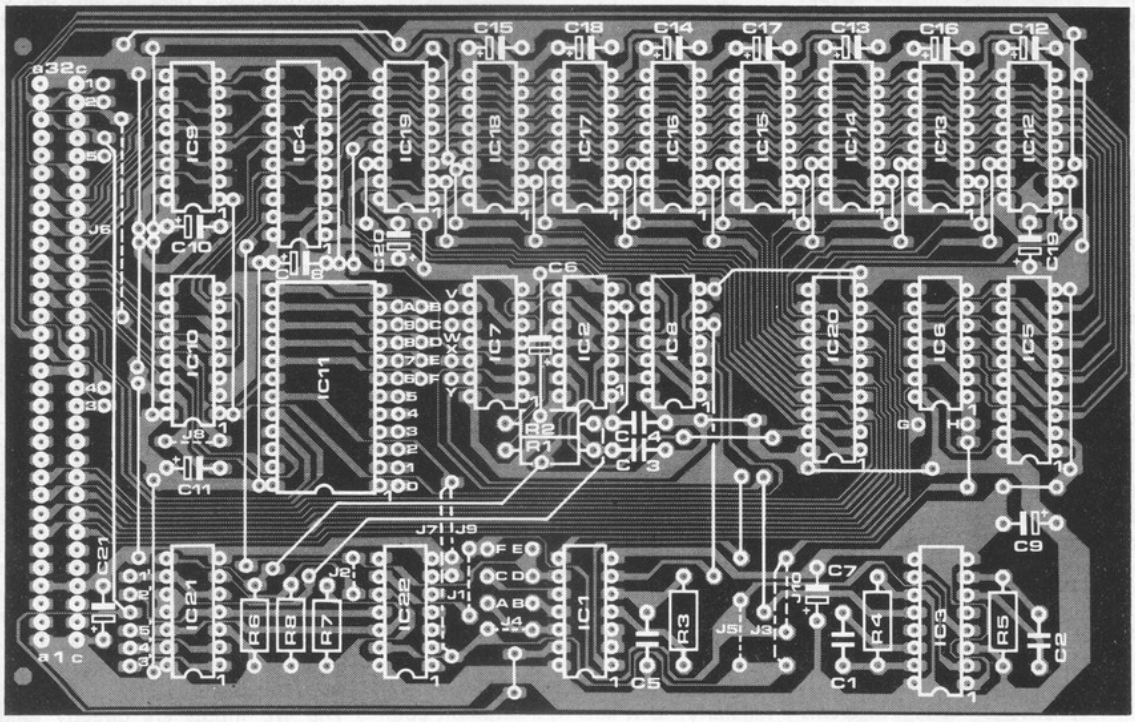


Figure 7. The component overlay and the copper tracking pattern of the dynamic RAM printed circuit board. The wire links should be mounted according to the different μP specifications in table 1.

Parts list

Resistors:
R1 . . . R3 = 270 Ω
R4,R5 = 2k2
R6 . . . R8 = 390 Ω

Capacitors:
C1 = 33 p
C2 = 100 p
C3 = 68 p
C4 = 470 p
C5 = 120 p
C6 . . . C21 = 1 μ/16 V tantalum

Semiconductors:
IC1,IC2 = 74LS14
IC3 = 74LS221
IC4,IC5,IC20 = 74LS244
IC6 = 74LS393
IC7 = 74LS08
IC8 = 74LS32
IC9,IC10 = 74LS157
IC11 = 74LS154
IC12 . . . IC19 = 4116 (250 ns)
IC21 = 74LS15
IC22 = 74LS74 (see text)

Miscellaneous:
1 x 64-pin DIN 41612, male connector

Construction

The printed circuit board for the dynamic RAM card is shown in figure 7. Since timing is very important, care must be taken when mounting the components. Readers are advised to abide by the indicated component values, especially with regard to the resistors and capacitors. The easiest method is to use the Elektor printed circuit board.

How the wire links are positioned depends on which processor is in use. Table 1 shows the requirements for the Junior Computer, the Z80 and the 8085. IC22 can be omitted for the 6502 and the Z80, as flipflop FF1 has also been left out. As far as the 8085 is concerned, things are different again. Unlike the Z80, the 8085 does not produce a refresh signal. Instead, this is generated by SØ, $\overline{S1}$ and INTA (which indicate the opcode fetch status). During the period that the processor needs to detect the code, the RAM is not being used and so a refresh cycle may take place. In the 8085 (multiplexed) addresses are accessed by way of a data bus. Since the dynamic RAM card is only suitable for a non-multiplexed bus, however, the data bus will have to be demultiplexed elsewhere in the 8085 system.

The connections between points V, W, X and Y and the outputs of IC11 define the address range. Each output of the IC represents an address range of 4K. The memory array is shown in table 2. A total of 16K therefore requires four outputs of IC11 to be linked to points V . . . Y. This enables data to be stored in blocks of 4K practically anywhere within the memory range.

Operators must remember one important aspect: the same code may not be used twice for A12 and A13 (see the last column in table 2), because the two address lines are both linked to the address inputs of the RAMs. This means that the wire links must be mounted in such a manner that the following combinations of A13 are stored in consecutive memory blocks:

A13	A12
Ø	Ø
Ø	1
1	Ø
1	1

It can easily be deduced which combinations are feasible. A valid combination would, for instance, be blocks 8ØØØ, 9ØØØ, AØØØ and BØØØ. But ØØØØ, 4ØØØ, 8ØØØ and CØØØ are totally out of the question, because A13 and A12 would be ØØ for all blocks.

If the card is used in combination with the Junior Computer, the required supply voltages will already be available. The other processor systems will have to produce the required voltages using integrated voltage regulators. Plenty of power supplies meeting the requirements can be found in previous Elektor issues.

Testing the circuit

Before connecting up the supply voltages, it is a good idea to check all the solder joints thoroughly. Then the card may be plugged into the bus of the μP system.

It doesn't really matter in which order the supply voltages are connected, although the manufacturer recommends constructors to start with the –5 V line. This provides an extra safety margin in the event of an overload (which is unlikely to happen if a good power supply is used).

If all is well the memory should function normally as soon as the power supply is switched on. As the memory locations are invisible to the naked eye, the best way to test the system is to read data in and out and compare the results. A special test program has been written for the purpose and is shown in table 3. This can also be used to test other types of RAM. Once the program has been entered, the start address and the end address of the memory range being tested must be stored at locations ØØØØ (= ADL) and ØØØ1 (= ADH) and at locations ØØØ2 (= ADL) and ØØØ3 (= ADH), respectively. The program is then initialised at address ØØØ4 and ØØ is written into the memory range. The program checks whether ØØ is in fact stored at the first address of the range-under-test. If so, Ø1, Ø2, Ø4, Ø8, 1Ø, 2Ø, 4Ø and 8Ø are written into the address in succession and read out again at once. As a result, every bit in the address will have been *high* once. Subsequently, FF is stored at this address to track down any addressing errors. For if there is an found in a different address. The mistake is detected when FF is read out somewhere along the line.

The above procedure is applied to every single address until the program reaches the end of the test range. Then the entire test program is repeated (it also tests the operator's patience!) starting with the storage of ØØs. This time the range is examined back to front. Again, this is necessary to be able to trace any addressing errors that might have cropped up.

If everything passed off without a hitch, address ØØØØ will appear on the display at the end of the program, followed by the low order address byte of the entered start address. If on the other hand an error was detected, the address at which it was found is shown on the display together with its (erroneous) contents. Restart the program at address ØØØA in order to carry on with the test.

Table 1

6502	Z-80	8085
1-1'	1-1'	1-1'
A-B	2-2'	2-2'
C-D	J2	3-3'
E-F	J3	4-4'
G-H	J4	5-5'
J8	J5	J1
J9	J6	J2
	J9	J4
IC22 is omitted		J6
	IC22 is omitted	J9
		J10

Table 1. This indicates which links are required on the printed circuit board when using the 6502, the Z80 or the 8085.

Table 2

output IC5	address 4 Kbyte-block	A15	A14	A13	A12
Ø	ØØØØ . . . ØFFF	Ø	Ø	Ø	Ø
1	1ØØØ . . . 1FFF	Ø	Ø	Ø	1
2	2ØØØ . . . 2FFF	Ø	Ø	1	Ø
3	3ØØØ . . . 3FFF	Ø	Ø	1	1
4	4ØØØ . . . 4FFF	Ø	1	Ø	Ø
5	5ØØØ . . . 5FFF	Ø	1	Ø	1
6	6ØØØ . . . 6FFF	Ø	1	1	Ø
7	7ØØØ . . . 7FFF	Ø	1	1	1
8	8ØØØ . . . 8FFF	1	Ø	Ø	Ø
9	9ØØØ . . . 9FFF	1	Ø	Ø	1
A	AØØØ . . . AFFF	1	Ø	1	Ø
B	BØØØ . . . BFFF	1	Ø	1	1
C	CØØØ . . . CFFF	1	1	Ø	Ø
D	DØØØ . . . DFFF	1	1	Ø	1
E	EØØØ . . . EFFF	1	1	1	Ø
F	FØØØ . . . FFFF	1	1	1	1

Table 2. The address range can be defined by linking the outputs of IC5 to points V, W, X and Y. Each connection provides 4K bytes, so that four connections are needed for a total of 16K.

```
0010: 0004                    ORG   $0004
0020:
0030:
0040:                 *** RAM TEST PROGRAM ***
0050:
0060:
0070:                 DEFINITIONS
0080:
0090: 0004            BEG     *     $0000  BEGIN OF MEMORY
0100: 0004            END     *     $0002  END OF MEMORY
0110: 0004            CUR     *     $00E6  CURRENT ADDRESS POINTER
0120: 0004            POINT   *     $00FA  MONITOR'S ADDRESS POINTER
0130: 0004            PATTER  *     $00E5  CURRENT TEST PATTERN
0140: 0004            MONITO  *     $1C1D
0150:
0160:
0170: 0004 20 45 00   RAMTST  JSR   WRZERO FILL WORKSPACE WITH $00
0180: 0007 20 54 00           JSR   CURBEG CUR = BEG
0190:
0200: 000A 20 84 00   TSTA    JSR   WALK   WALKING BIT ROUTINE
0210: 000D D0 2B              BNE   TSTC   BRANCH IF MEMORY CELL IS DEFECT
0220: 000F A9 FF              LDAIM $FF    TEST PATTERN FOR DOUBLE ADDRESSING
0230: 0011 91 E6              STAIY CUR
0240: 0013 20 5D 00           JSR   INCCHK INCREMENT AND CHECK CUR
0250: 0016 B0 F2              BCS   TSTA   TEST FINISHED?
0260: 0018 20 45 00           JSR   WRZERO FILL WORKSPACE WITH $00
0270: 001B A6 02              LDX   END    CHECK FROM BOTTOM TO TOP
0280: 001D 86 E6              STX   CUR
0290: 001F A6 03              LDX   END    +01
0300: 0021 86 E7              STX   CUR    +01
0310:
0320: 0023 20 84 00   TSTB    JSR   WALK
0330: 0026 D0 12              BNE   TSTC   BRANCH IF MEMORY CELL IS DEFECT
0340: 0028 A9 FF              LDAIM $FF    TEST PATTERN FOR DOUBLE ADDRESSING
0350: 002A 91 E6              STAIY CUR
0360: 002C 20 6D 00           JSR   DECCHK DECREMENT AND CHECK CUR
0370: 002F B0 F2              BCS   TSTB
0380: 0031 A9 00              LDAIM $00    DISPLAY "0000 XX" IF
0390: 0033 85 FA              STA   POINT  MEMORY IS O.K.
0400: 0035 85 FB              STA   POINT  +01
0410: 0037 4C 1D 1C           JMP   MONITO
0420:
0430: 003A A5 E6      TSTC    LDA   CUR    DISPLAY THE ADDRESS OF
0440: 003C 85 FA              STA   POINT  THE DEFECT MEMORY CELL
0450: 003E A5 E7              LDA   CUR    +01
0460: 0040 85 FB              STA   POINT  +01
0470: 0042 4C 1D 1C           JMP   MONITO
0480:
0490:
0500:                 SUBROUTINES
0510:
0520:
0530: 0045 20 54 00   WRZERO  JSR   CURBEG FILL THE MEMORY BETWEEN BEG & END
0540: 0048 A0 00              LDYIM $00    WITH $00
0550:
0560: 004A A9 00      WRZ     LDAIM $00
0570: 004C 91 E6              STAIY CUR
0580: 004E 20 5D 00           JSR   INCCHK
0590: 0051 B0 F7              BCS   WRZ
0600: 0053 60                 RTS
0610:
0620: 0054 A6 00      CURBEG  LDX   BEG    CUR = BEG
0630: 0056 86 E6              STX   CUR
0640: 0058 A6 01              LDX   BEG    +01
0650: 005A 86 E7              STX   CUR    +01
0660: 005C 60                 RTS
0670:
0680: 005D E6 E6      INCCHK  INC   CUR    CUR = CUR+01
0690: 005F D0 02              BNE   IA
0700: 0061 E6 E7              INC   CUR    +01
0710:
0720: 0063 38         IA      SEC          C=0 IF CUR >END
0730: 0064 A5 02              LDA   END
0740: 0066 E5 E6              SBC   CUR
0750: 0068 A5 03              LDA   END    +01
0760: 006A E5 E7              SBC   CUR    +01
0770: 006C 60                 RTS
0780:
0790: 006D 38         DECCHK  SEC          CUR = CUR -01
0800: 006E A5 E6              LDA   CUR
0810: 0070 E9 01              SBCIM $01
0820: 0072 85 E6              STA   CUR
0830: 0074 A5 E7              LDA   CUR    +01
0840: 0076 E9 00              SBCIM $00
0850: 0078 85 E7              STA   CUR    +01
0860: 007A 38                 SEC          C=0 IF CUR < BEG
0870: 007B A5 E6              LDA   CUR
0880: 007D E5 00              SBC   BEG
0890: 007F A5 E7              LDA   CUR    +01
0900: 0081 E5 01              SBC   BEG    +01
0910: 0083 60                 RTS
0920:
0930: 0084 A9 01      WALK    LDAIM $01    INIT. PATTERN
0940: 0086 85 E5              STA   PATTER
0950: 0088 A0 00              LDYIM $00
0960: 008A B1 E6              LDAIY CUR    IS STILL $00 IN THE CELL
0970: 008C D0 0F              BNE   WALKB  IF NOT, THEN BRANCH
0980: 008E A2 08              LDXIM $08    WALKING BIT COUNTER
0990:
1000: 0090 A5 E5      WALKA   LDA   PATTER CURR. PATTERN INTO ACCU
1010: 0092 91 E6              STAIY CUR    STORE IT IN MEMORY
1020: 0094 D1 E6              CMPIY CUR    DOES IT MATCH?
1030: 0096 D0 05              BNE   WALKB  IF NOT, THEN BRANCH
1040: 0098 06 E5              ASL   PATTER WALKING BITS!
1050: 009A CA                 DEX
1060: 009B D0 F3              BNE   WALKA
1070:
1080: 009D 60         WALKB   RTS
1090:
1100:
```

Table 3. The RAM test program. The start and end addresses of the range-under-test must be stored at addresses 0000 . . . 0003. The program starts at address 0004.

when is an OTA not an OTA?

. . . when it's a 13600!

Many readers will be familiar with the 3080 and 3094 Operational Transconductance Amplifiers, or OTAs. Since their introduction by RCA in the early seventies, this type of device has been used extensively in the most varied applications. Recently, a new and improved version has been announced – the 13600. It includes linearizing diodes at the input, to allow for higher input levels and a greater linear control range (over six decades!), as well as controlled impedance buffers at the output.
In this article, we will take a closer look at the device. The conclusion is surprising: when used in the 'ideal' circuit arrangement, this OTA isn't an OTA!

The difference between an OTA and a normal opamp can be summed up in a few words. An opamp is voltage-driven: the differential input voltage is multiplied by a fixed gain (100,000 times, or so), so that a much larger voltage appears at the output. In other words: it's a voltage amplifier with fixed gain.
The input to an OTA is also a differential voltage, but the output is a *current*.

This means that the relationship between input and output signals is not a simple (voltage) gain: it is the 'forward transconductance', g_m, expressed in 'mho' or mA/V. The output current can be converted back into a voltage by the simple expedient of passing it through a load resistor, R_L. This leaves us with a voltage amplifier, with a gain of $g_m \times R_L$. This is not so spectacular, until you discover that g_m can be controlled by a DC bias current (I_{ABC}), over an extremely wide range. In other words, an OTA is a voltage-driven current source (or, with an external load resistor: a voltage amplifier) with a 'gain' that can be varied over a wide range by means of a control current.
As we have seen in recent years, this leads to a wide range of interesting applications. Take figure 1, for example: a voltage-controlled volume control! The control voltage, U_C, determines the bias current I_{ABC}. The higher the voltage, the higher the overall gain; when U_C is zero, the output is also zero. For obvious reasons, there is no feedback around this circuit – the gain must be set by I_{ABC}, not by the values in a feedback loop!
Applications are not restricted to 'pure' audio, as illustrated in figure 2. This is an oscillator, with triangular and square-wave outputs. The output frequency is voltage controlled, over an extremely wide range: 2 Hz to 200 kHz! This corresponds to control currents from 10 nA to 1 mA. This is by no means the only alternative application for OTAs: we have seen them used (and used them!) in AM modulators, multipliers, true RMS converters, automatic level controls, voltage-controlled resistors, filters, sine-wave generators, timer circuits, phase-locked loops, sample-and-hold circuits, logarithmic amplifiers, and so on . . . The new DNR circuit also uses an OTA, to construct a filter with a variable cut-off frequency.

The 13600

The 13600 contains two current-controlled transconductance amplifiers, each with differential inputs, linearizing diodes and controlled output buffers. The internal circuit for one OTA is given in figure 3.
At the input, T4 and T5 are a straightforward differential amplifier ('long-tailed pair'). The current source in the 'tail' (T1, T2 and D1) is actually a current 'mirror': the collector current of T2 is equal to the bias current I_{ABC}. At this point, we are faced with the choice: dive deeply into the theory or skip it? . . . We will attempt a compromise.
For small differential input signals, the collector currents of T4 and T5 (I_4 and I_5) are almost identical; together, they are equal to the sum of their emitter currents, so each is equal to approximately $\frac{1}{2}I_{ABC}$. At the same time, the ratio between these two currents is determined by the differential input voltage. For small signals, it can be shown that the difference between the collector currents, $I_5 - I_4$, is equal to the input voltage times the bias current ($U_{in} \times I_{ABC}$), multiplied by a constant factor:

$$U_{in} \times I_{ABC} = K\,(I_5 - I_4).$$

So far, so good. The next step is to add three more current mirrors (T6-T7-D4, T10-T11-D6 and T8-T9-D5), in such a way that the collector current of T11 is equal to I_5 and that of T9 is equal to I_4. This means that the output current is equal to the difference between I_5 and I_4, so:

$$U_{in} \times I_{ABC} = K \times I_{out}.$$

In other words, I_{out} over U_{in} (the transconductance) is equal to I_{ABC} over K. It is determined by the bias current! And that is precisely why an OTA is

1

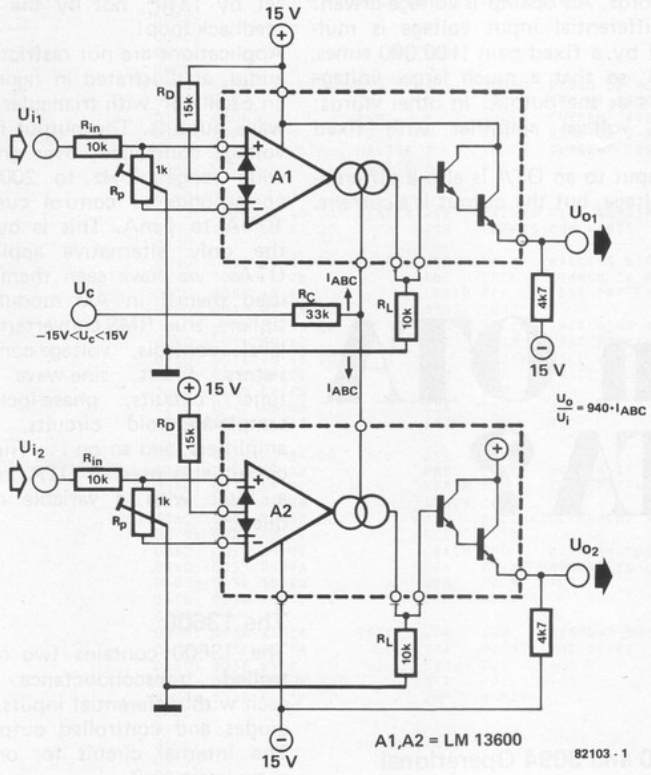


Figure 1. The OTA can be used as a 'STEREO' volume control. The level is set by the voltage on the control input.

2

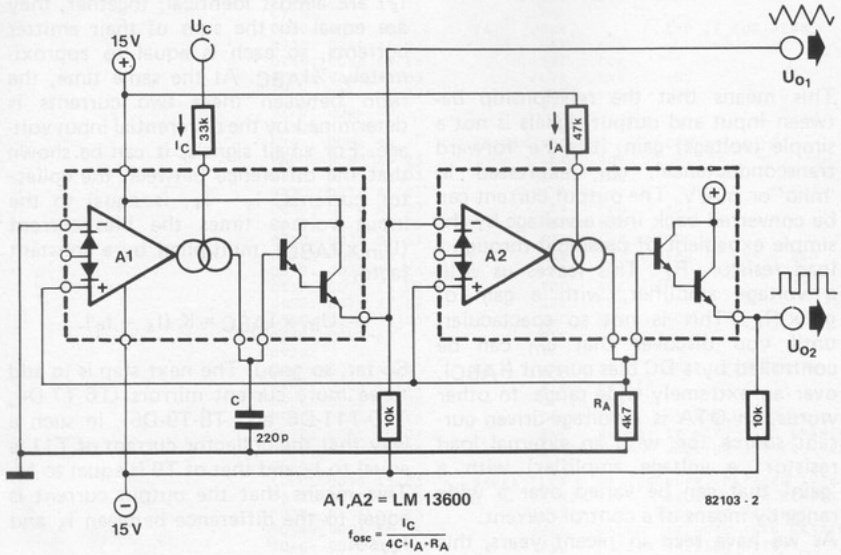


Figure 2. A voltage controlled oscillator (VCO), with a frequency range of 2 Hz to 200 kHz.

such a useful and versatile device.

It will be obvious that when the bias current I_{ABC} is zero, all other currents must also be zero – the device draws no current at all. Furthermore, the maximum output current is delivered when I_4 or I_5 is zero, so that the other current (and, with it, the output current) is equal to I_{ABC}.

To avoid a lot of laborious calculations, the transconductance of the device is plotted as a function of the bias current in the graph shown in figure 3. Note that the transconductance is given in μmho (μA/V), so that the overall gain is obtained by multiplying this by the value of the load resistor in megohms.

What have we got, so far? The circuit to the left of the dotted line in figure 3, ignoring diodes D2 and D3 for the moment, is an OTA. The bias current is applied to the base of T2; the input voltage is connected between the bases of T4 and T5; and the output current appears at the collectors of T9 and T11. This leaves us with only a few 'odd' components that must, apparently, make the difference between a normal OTA and a 13600.

To the right of the dotted line, there are three transistors. At first sight, T12 and T13 appear to be a normal 'Darlington' stage. However, a closer examination shows that the emitter current of T12 is controlled by T3. The latter is connected to the current mirror circuit around T1 and T2, in such a way that the collector current of T3 must equal that of T1 – which, in turn, is equal to the bias current I_{ABC}. In a nutshell: the emitter current of T12 is equal to I_{ABC}. This is very intriguing . . . but what's the point?!

The thing to realise is that the output of the OTA is a rather sensitive point. Preferably, it should be connected to a high-impedance buffer stage; this becomes all the more important at low levels of I_{ABC}, when the output impedance of the OTA is high and the signal level is low. Loading the output with a relatively low impedance would lead to poor linearity under those conditions. In other words, if T12 and T13 are used as an output buffer, it is advisable to set them at as low a current as possible – in the interest of good performance at low output levels.

When the OTA is delivering a high output level, however, the following buffer stage must have a high slew rate – so that it can cope with rapid variations of the output current, over a wide range. The normal way to achieve this is to set T12 and T13 at a fairly high current. Which poses a problem: these transistors must be set at a low current – to provide good linearity, especially at low levels – *and* at a high current, to provide a high slew rate for large signals. We can't very well do both at the same time!

The solution is to vary the setting of the output buffer in accordance with the bias current, I_{ABC}. This is where T3

comes in: as stated above, it ensures that the current setting of T12 is determined by I_{ABC}. Neat! T12 and T13 now provide an almost ideal buffer stage between the high-impedance output of the OTA and a following (low-impedance) input.

Add a few diodes . . .

In most applications, OTAs are used without feedback. As mentioned above, this is unavoidable when the device is to set the overall gain in the circuit. However, there is a major drawback: any non-linearity in the transfer characteristic will give rise to distortion . . .

For this reason, it is essential for the total circuit to be as linear as possible. This is no mean trick, when you consider that the bias current through the input stage may vary over an extremely wide range – from nano-amps to milli-amps! To make matters worse, the input stage of an OTA is inherently non-linear – the transconductance is determined by the 'diode'-characteristic of the input transistors. For the older type of OTA, this meant that the input voltage should not be more than some 50 mV peak-to-peak, in other words, the dynamic range is rather limited.

If we could eliminate the non-linearity at the input, it would be possible to apply much higher input levels – improving the signal-to-noise ratio, for the same maximum distortion. An alternative solution is to pre-distort the input signal in such a way that the distortion caused by the input stage will result in a 'clean' signal. In other words, distort the signal 'in the opposite direction' before applying it to the input.

This, effectively, is what the two diodes at the input are for (D2 and D3 in figure 3). To see how these work, it is easier to re-draw the input circuit as shown in figure 4. The two diodes are now shown as transistors, with base connected to collector (which is precisely what they are, on the chip!), and all the currents in the circuit are assumed to be controlled by current sources.

The common emitter current for the long-tailed pair (I_{ABC}) is set by the current source I_B; the total bias current for the two diodes is I_D. To ensure that the same current flows through both diodes, under static conditions, a further current source ($\frac{1}{2}I_D$) is connected between D2 and the negative supply rail. Finally, and rather surprisingly, the input signal is also assumed to be a *current*, I_S. For the present, we will not consider what happens when a voltage is applied to the input! For the purpose of this explanation, we will also assume that the base currents of T4 and T5 are so small that they can be ignored.

When the input current is zero, the currents through D2 and D3 must be identical (both equal to $\frac{1}{2}I_D$). Since all transistors are identical, this means that the voltages across the two diodes must also be the same. This, in turn, leads to identical base-emitter voltages for T4 and T5; therefore $I_4 = I_5$, and so $I_5 - I_4 = 0$. No signal in means no signal out, as you would expect . . .

Now, when a current I_S is supplied to the input, the current through D2 will be reduced: I_S plus the current through D2 must be equal to $\frac{1}{2}I_D$, as determined by the lower left-hand current source. But when the current through D2 is reduced, that through D3 must increase by the same amount: the sum of the two currents must remain equal to I_D. Less current through D2 means that the voltage across this diode must also be reduced; similarly, the greater current through D3 corresponds to a larger voltage across this diode. As a result, a voltage difference appears between the base of T4 and that of T5. The differential amplifier converts this voltage difference into a differential output, $I_5 - I_4$.

In effect, the input current is first converted into a (distorted) voltage, by means of D2 and D3; when this voltage is applied to T4 and T5, the distortion effects cancel out and the differential output current is undistorted! This is further illustrated in figure 5. In the upper half of the drawing, the input signal is zero. The currents through the two diodes are identical ($= \frac{1}{2}I_D$), so the voltages across them are also the same. In the lower half of the drawing, an input current (I_S) has reduced the current through D2 to $\frac{1}{2}I_D - I_S$; as explained above, the current through D3 must then increase to $\frac{1}{2}I_D + I_S$. When we 'bounce' these values off the

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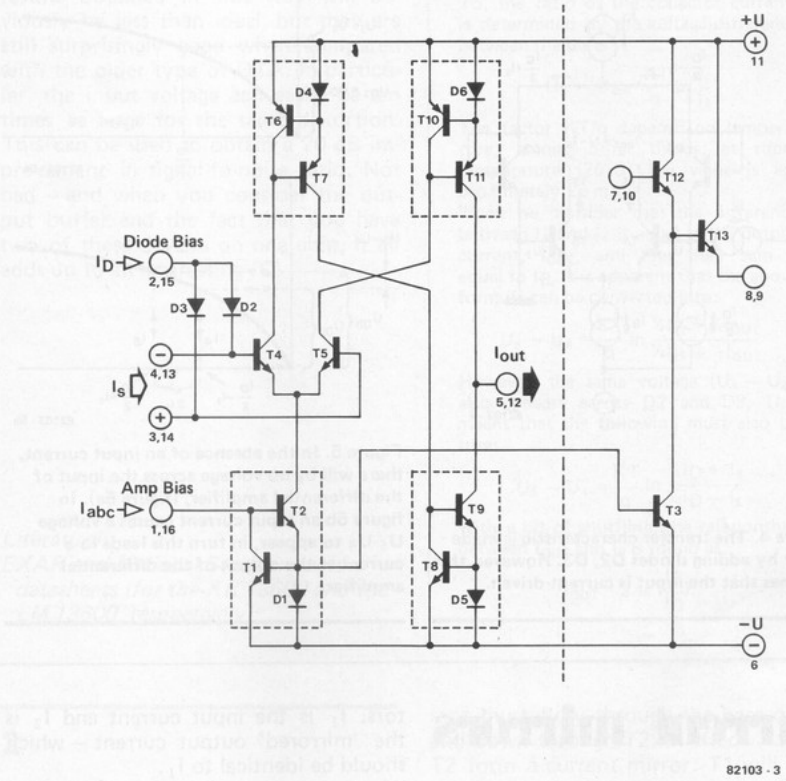

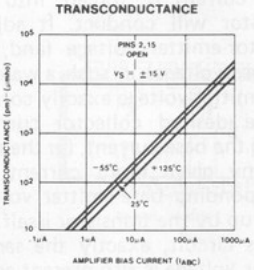

$$I_{out} = \frac{2I_S\, I_{abc}}{I_D}$$

Figure 3. The circuit diagram of the new OTA. It consists of little more than four current mirrors and an ordinary differential amplifier. Diodes D2 and D3 are the linearizing diodes, which allow for larger input signal amplitudes.

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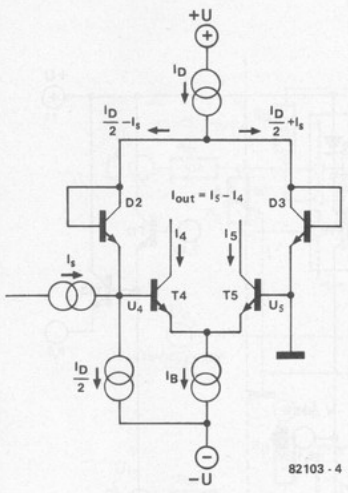

Figure 4. The transfer characteristic is made linear by adding diodes D2, D3. However, this assumes that the input is current-driven.

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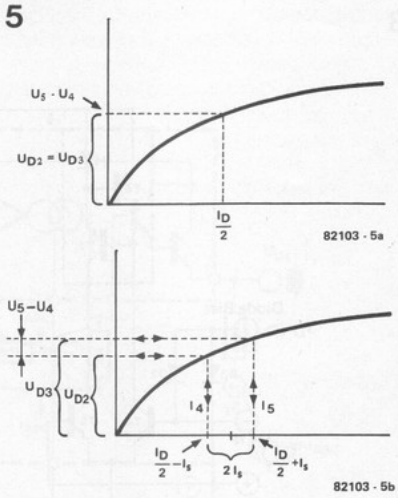

Figure 5. In the absence of an input current, there will be no voltage across the input of the differential amplifier, (figure 5a). In figure 5b an input current causes a voltage U_5-U_4 to appear, in turn this leads to a current at the output of the differential amplifier.

curve that represents the characteristic of the diodes (figures 5a & b), we find the voltages U_{D_3} and U_{D_4} as shown. The difference between these voltages is the differential input voltage, $U_5 - U_4$.

In the special case when the bias current (I_B) is equal to the diode bias current I_D, the next step is very easy. The base-emitter voltages of T4 and T5 are then identical to U_{D_2} and U_{D_3}, respectively. The collector currents are therefore found by 'bouncing' these values back off the same curve; as can be seen, the difference between the two currents is equal to 2 I_S.

As the amplifier bias current, I_{ABC}, is reduced, the base voltages of T4 and T5 'slide down the curve'. This leads to a smaller difference between I_4 and I_5, as can be seen; however, the linear relationship between I_S and the differential output current is maintained. This not only 'seems reasonable', when you look at the plot; it can also be proved mathematically. In fact, the calculation is given elsewhere; the less mathematically-minded can forget the proof, however, and believe the result:

current mirrors

A current mirror is nothing new: it is simply a circuit that ensures that two currents are identical. However, the idea is extremely useful in IC technology, since excellent accuracy can be achieved without the need for any external calibration or on-chip trimming. The trick is to make good use of the identical characteristics of transistors – certainly when they are on the same chip, as in normal IC manufacture.

As with all the best ideas, the basic principle of a current mirror is quite simple. When current is passed through a diode, a voltage will appear across it. The converse is also true: if exactly the same voltage is applied across the diode as that which appeared in the previous case, a current will flow through the diode that is also identical. A current will define an exact voltage, and that voltage will define the same current.

Taking this idea one step further: if the same voltage is applied to two identical diodes, the same current will flow in each! The same applies to transistors: provided they are identical, the same base-emitter voltage will lead to equal base currents and, since the transistors are identical, the collector currents will also be the same. It should be noted that this is true over the entire range of permissable currents – in spite of the fact that the voltage/current characteristic of a diode (or transistor) is anything but linear.

From this point, it is only a small step to a current mirror. Figure 1 shows the simplest version, using only two transistors. I_1 is the input current and I_2 is the 'mirrored' output current – which should be identical to I_1.

When current is 'forced' into T1, this transistor will conduct. It adjusts the collector-emitter voltage (and, with it, the base voltage) in such a way that the base-emitter voltage exactly corresponds to the desired collector current – ignoring the base current, for the moment. For any given input current, I_1, the corresponding base-emitter voltage will be set up by the transistor itself.

In this circuit, exactly the same base-emitter voltage is also present across T2. Since this transistor is identical to T1, the collector current I_2 must be the same as the collector current of T1!

To sum it up: when a current (I_1) is applied to T1, this transistor will set up a corresponding voltage between base and emitter. This voltage also appears between base and emitter of T2, so the collector current of T2 (I_2) must be identical to I_1 (once again: ignoring the base currents!).

Basically, that is all there is to a current mirror. There is nothing mysterious or 'earth-shattering' about it! In fact, you can easily build one, as shown in figure 2. For best results, the transistors should be identical. An easy way to make sure of this is to use a CA 3046 (or CA 3086). This IC contains five identical transistors, two of which can be used for the current mirror. By the way, although two meters are shown in the circuit, it is quite possible to use only one. First set the current through T1, by adjusting P1; then move the meter to the other 'leg' (and substitute a wire link in the original position): the collector current through T2 will prove to be identical.

While we're at it, we can add a further transistor (T3) in parallel with T2. Obviously, it will also draw the same collector current as the other transistors. In other words, the total collector current of T2 and T3 must be exactly equal to twice the collector current of T1! A precision current multiplier . . . which might prove useful for a cheap-and-reliable D/A converter? Don't bother trying to patent it: Philips already have . . . it's what they use in the 'compact disc' players!

So far, we have consistently ignored the base current. In the basic circuit, however, they must all come out of I_1. This means that the collector current of T1 is actually slightly less than I_1, so all 'mirrored' currents will also be slightly smaller. Going back to figure 1: if the current gain of the transistors (ß) is 100, the base currents will be 1% of the collector currents. If we assume that the base currents are both '1', the collector currents will both be '100'. As can be seen, this means that $I_1 = 102$ and $I_2 = 100$ – a 2% error!

Obviously, this error will be reduced as the current gain of the transistors is increased. However, for a precision current mirror the gain would need to be almost infinite . . . which is not so easy to achieve. A better solution is to add one more transistor, as shown in figure 3. This reduces the error by a factor that is equal to the gain of the additional transistor!

At first sight, this circuit may seem 'reversed' – with I_2 as the input current – but it's not that bad. Let's assume that a current, I_1, is forced down at the left. If T1 is blocked, initially, the cur-

$$I_{out} = I_5 - I_4 = 2\ I_S\ (\frac{I_B}{I_D}).$$

From this formula, and from the circuit, several things are apparent. In the first place, the current gain is proportional to the ratio between I_B and I_D. With one proviso: the current through the diodes can only flow in one direction! This means that I_S must always be less than $\frac{1}{2}I_D$. If too small a value is chosen for I_D, the distortion can become extremely high . . .

A further conclusion is rather surprising: this OTA isn't an OTA – it's a current amplifier! In the ideal case, it requires an input current; it produces an output current; and the ratio between the two (the current gain) is set by the amplifier bias current, I_{ABC}, and the diode bias current (I_D). 'Voltage' doesn't come into the story! In fact, if a (differential) voltage is applied to the input, the two diodes cannot pre-distort it. The total circuit will then behave like any other OTA – with all the distortion associated with that operation mode!
In practice, an intermediate mode will normally be used. Instead of current sources, resistors are used to 'convert' voltages into the necessary currents. The results obtained in this way will obviously be less than ideal, but they are still surprisingly good when compared with the older type of OTA. In particular, the input voltage can easily be ten times as large for the same distortion. This can be used to obtain a 20 dB improvement in signal-to-noise ratio. Not bad – and when you consider the output buffer and the fact that you have two of these devices on one chip, it all adds up to an interesting IC!

Literature:
EXAR and National Semiconductor datasheets (for the XR 13600 and the LM 13600, respectively).

Linear relationship between I_S and I_{out}

For the differential input stage, T4 and T5, the ratio of the collector currents is determined by the voltage difference between the bases:

$$U_5 - U_4 = \frac{KT}{q} \ln \frac{I_5}{I_4}$$

The factor KT/q depends on temperature, among other things; at room temperature (25°C) the value is approximately 25 mV.
When we consider that the difference between I_5 and I_4 is equal to the output current, I_{out}, and that their sum is equal to I_B, it is apparent that the above formula can be converted into:

$$U_5 - U_4 = \frac{KT}{q} \ln \frac{\frac{1}{2}I_B + \frac{1}{2}I_{out}}{\frac{1}{2}I_B - \frac{1}{2}I_{out}}$$

However, the same voltage ($U_5 - U_4$) also appears across D2 and D3. This means that the following must also be true:

$$U_5 - U_4 = \frac{KT}{q} \ln \frac{\frac{1}{2}I_D + I_S}{\frac{1}{2}I_D - I_S}$$

With a bit of shuffling, the relationship between I_{out} and I_S is found as:

$$I_{out} = 2\ I_S\ (\frac{I_B}{I_D}).$$

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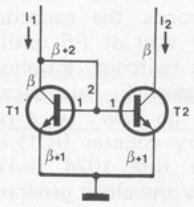

Figure 1. The basic version of a current mirror.

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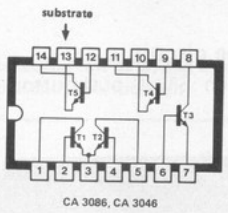

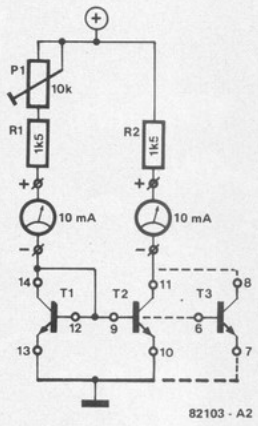

Figure 2. The test circuit.

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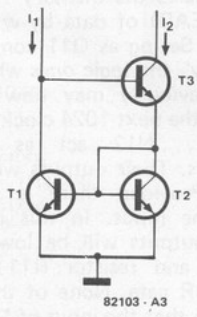

Figure 3. An extended version of the current mirror.

rent must flow through the base of T3 and down through T2. In effect, T1 and T2 form a current mirror: T1 will now draw a current that is equal to the collector current of T2. This, in turn, is almost identical to the collector current of T3. Now, let's look at the base currents. All transistors are set to virtually identical collector currents, so their base currents must also be the same. Two base currents (for T1 and T2) are derived from the emitter of T3; half of this current must correspond to the base current of T3 (which comes from I_1) and the other half comes from I_2. This means that I_1 and I_2 are almost identical: the only difference is the slightly higher base current needed by T3 to pass the marginally higher collector current. As stated above, this error is reduced in proportion to the current gain of T3.
This three-transistor current mirror is almost perfect. It is used in the OTA. Note that T2 is actually connected as a 'diode'; it is drawn as such in the circuit of the OTA. Needless to say, awkward things like temperature fluctuations have no adverse effect, since the transistors are all on the same chip. ◀

2114 RAM tester

A memory IC is a tiny 'black box' in that none of its inner activities can be seen from the outside. We have to rely on the facts and figures published in data sheets. It is extremely difficult to know whether the IC is functioning properly, since about as much is going on inside as at the London stock-exchange!
Where digital data is concerned, however, operators can find out how the IC will react to a certain logic input signal, using for instance the 2114 IC tester introduced here.

The 2114 RAM is a highly popular IC and is used in just about every type of personal computer. Consequently it has dropped in price considerably in recent years. Nevertheless, quite a few RAMs are required for a computer to have a reasonable memory capacity, so that it would be nice if they could be tested there and then in the shop — with the dealer's permission, of course! — to avoid buying any 'duds'.
Before we consider the circuit, let's take a look at the test program in figure 1. As mentioned earlier, a digital IC must react to a specific input level. If the IC is 'out of order' a red LED lights by way of warning. Initially, every memory location is loaded with a logic 1. Should the tester detect a low logic level anywhere, something is bound to be wrong and the indicator will light. If, on the other hand, everything is perfectly O.K., the next section in the test program is run. This time low logic levels are stored throughout the memory range. Again, as soon as the tester encounters a logic one, the LED lights. Otherwise, the test program simply starts all over again. More details about the test cycle will follow later.
At the same time, the tester checks the current consumption of the RAM. An additional red LED lights whenever the power supply is 'shorted' or the IC consumes more than 100 mA.

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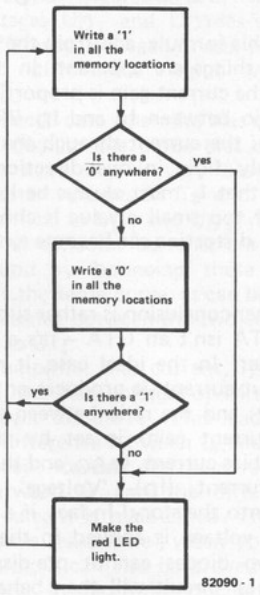
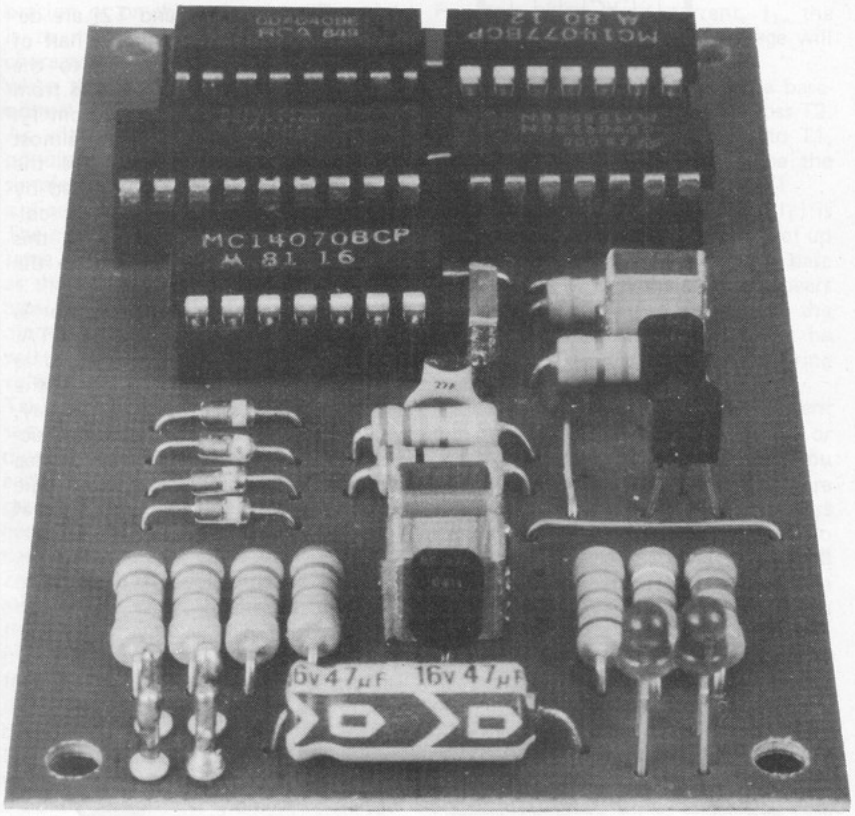


Figure 1. The test program flowchart. A red LED lights whenever the output data does not correspond to the input information.

The circuit

When S1, a pushbutton switch, is depressed the output of N2 is 'high' to start with. This resets IC1 and the flipflop N3/N4 (by way of N5) and the Q outputs of IC1 are all 'low'. After about 100 milliseconds the capacitor C2 is charged by way of R6 until its level reaches the switching threshold of the Schmitt trigger N2. This makes the output of N2 go 'low'. As a result, the 12-bit binary counter (IC1) is started. During the first 1024 (= 1k) pulses produced by the clock generator N1 (at a clock frequency of about 10 kHz), outputs Q10 and Q11 remain 'low'. This means that the $\overline{WE}$ input will also be logic 0. Since the inputs of gates N6 and N7 are 'low' and their outputs are therefore 'high', inputs I/01 . . . I/04 of the RAM will be 'high'. In other words, one nibble (4 bits) per clock pulse is stored.
After 1024 clock pulses, Q10 goes high, which prepares the memory IC for the output (READ) of data by way of the $\overline{WE}$ input. Seeing as Q11 continues to remain 'low', the logic *ones* which were entered previously may now be read out during the next 1024 clock pulses.
Gates N9 . . . N12 act as (EXOR) comparators. Their outputs will always be high. Provided there is a logic 1 at only one input. In this particular case, the outputs will be low. Diodes D1 . . . D4 and resistor R11 together form an OR gate. None of the diodes conduct, so that the input of N8 will be low. Gate N8 acts as an inverter and under the conditions described here its output will be high.
Since the inverter N5 also produces a high logic level at its output, which reaches the RS flipflop N3/N4, the Q output and the base of transistor T1



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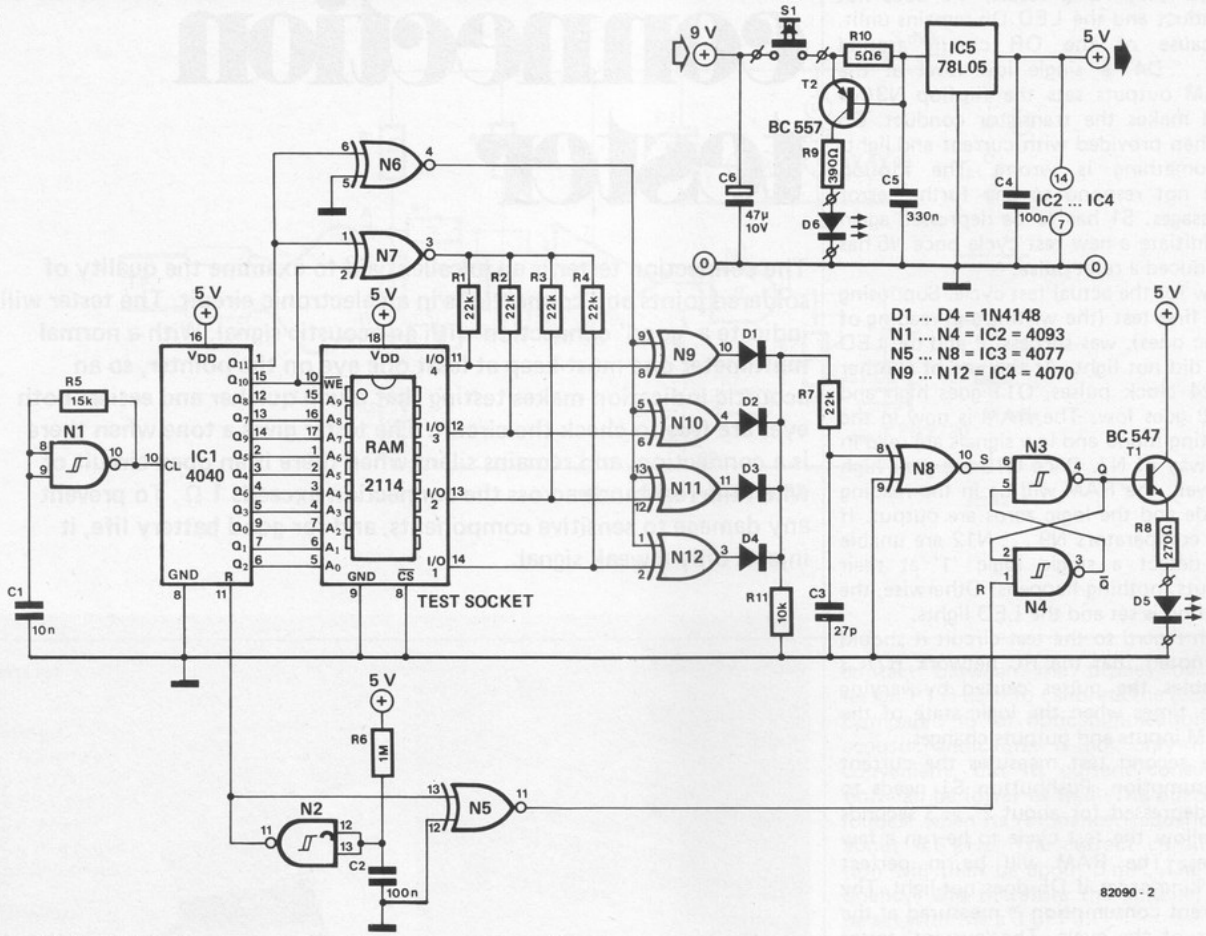


Figure 2. The RAM tester circuit consists of a counter, which furnishes the test data, and a comparator circuit that controls an LED. In addition, the circuit measures the current consumption and provides an indication if it is too high.

Parts list

Resistors:
R1 . . . R4,R7 = 22 k
R5 = 15 k
R6 = 1 M
R8 = 270 Ω
R9 = 390 Ω
R10 = 5,6 Ω
R11 = 10 k

Capacitors:
C1 = 10 n
C2,C4 = 100 n
C3 = 27 p
C5 = 330 n
C6 = 47 µ/10 V

Semiconductors:
D1 . . . D4 = 1N4148
D5,D6 = LED red
T1 = BC 547
T2 = BC 557
IC1 = 4040
IC2 = 4093
IC3 = 4077
IC4 = 4070
IC5 = 78L05

Miscellaneous:
S1 = sp pushbutton switch
9 V battery

3

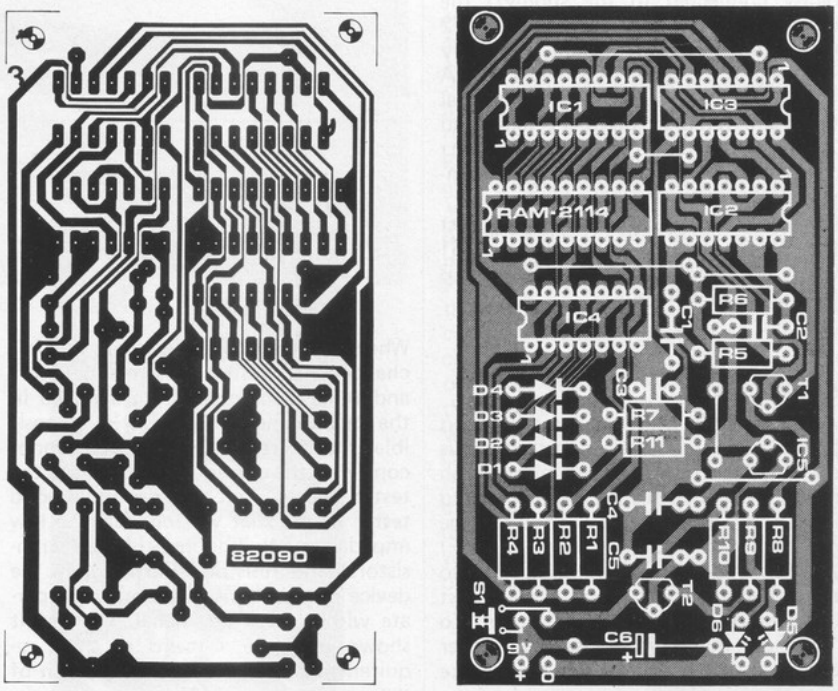


Figure 3. The track pattern and the component overlay of the RAM tester printed circuit board. The RAM socket shown here may also be a test socket. The circuit can be powered with the aid of a 9 V battery.

stay 'low'. As a result, T1 does not conduct and the LED D5 remains unlit. Because of the OR circuit around D1 . . . D4, a single low level at the RAM outputs sets the flipflop N3/N4 and makes the transistor conduct. D5 is then provided with current and lights – something is wrong. The flipflop will not respond to any further error messages. S1 has to be depressed again to initiate a new test cycle once N5 has produced a reset pulse.

Now for the actual test cycle. Supposing the first test (the writing and reading of logic ones), was successful and the LED D5 did not light. At the end of another 1024 clock pulses, Q11 goes high and Q10 goes low. The RAM is now in the writing mode and low signals are read in by way of N7. Once Q10 has gone high as well, the RAM will be in the reading mode and the logic zeros are output. If the comparators N9 . . . N12 are unable to detect a single logic '1' at their inputs, nothing happens. Otherwise, the flipflop is set and the LED lights.

With regard to the test circuit it should be noted that the RC network R7/C3 disables the pulses caused by varying gate times when the logic state of the RAM inputs and outputs changes.

The second test measures the current consumption. Pushbutton S1 needs to be depressed for about 2 . . . 3 seconds to allow the test cycle to be run a few times. The RAM will be in perfect working order if D5 does not light. The current consumption is measured at the start of the cycle. The 'current' tester consists of R9, R10, T2 and D6. If the RAM consumes more than 100 mA, because of an internal 'short' for instance, (or if the RAM has been incorrectly connected to the supply!) the drop in voltage across R10 will cause T2 to conduct and D6 to light. Normally speaking, the L-type RAM draws 25 mA (40 mA maximum), whereas the normal types are rated at 50 mA typical and 70 mA maximum. The maximum short circuit current is 140 mA and is controlled by IC5.

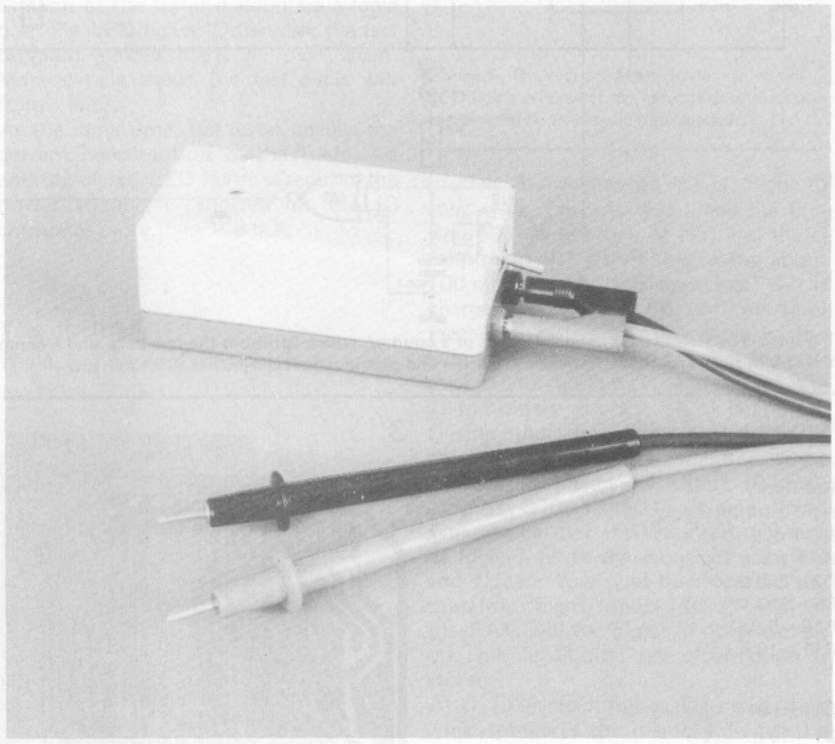
Note that it is also possible to self-test the RAM tester. Simply depress S1 when no RAM is inserted and if all is well LED D5 will light.

Construction

As can be seen from the printed circuit board in figure 3, the construction is quite straightforward. The photograph shows what the finished product should look like. The RAM may, of course, be mounted in a zero insertion force (ZIF) socket if required, but these do tend to be rather expensive. The circuit must be powered with a 9 V battery. To 'wrap up' the project, insert the tester circuit into a small plastic case. Make sure there is plenty of room around the RAM on the test socket and that it doesn't come into contact with other components. ◀

connection tester

The connection tester is an excellent aid to examine the quality of soldered joints and connections in an electronic circuit. The tester will indicate a 'good' connection with an acoustic signal. With a normal multimeter one must keep at least one eye on the pointer, so an acoustic indication makes testing that much quicker and easier: both eyes are free to check the circuit. The tester gives a tone when there is a connection, and remains silent when there is an open circuit or when the resistance across the connection exceeds 1 Ω. To prevent any damage to sensitive components, and for good battery life, it injects only a weak signal.



When testing connections there is a fair chance that resistors, semiconductors and other components are involved in the measurement. Moreover it is possible that certain components cannot cope with the current and/or voltage the tester injects. For this reason, a good tester is one that will not react to low impedance PN junctions (diodes, transistors) and resistors. Furthermore the device must be sensitive enough to operate with a weak test signal. The circuit shown in figure 1 meets all these requirements. Thanks to the high gain of the opamp (type 741) used in this circuit, the current and voltage for the test signal can be limited to 200 μA and 2 mV, respectively.

The opamp is connected as a differential amplifier; the voltage difference between the inverting (pin 2) and non-inverting input (pin 3) is increased considerably. The voltage drop across R2 ensures that the output of the opamp becomes negative, since the inverting input has a higher potential than the non-inverting input. The potential at the non-inverting input can be increased by turning P1, so that this input becomes more positive than the inverting one (as soon as the voltage across R2 drops). The result is a positive voltage at the output of the opamp. The oscillator constructed around N1 will then produce a tone via the buzzer. The voltage drop across R2 is caused by a good

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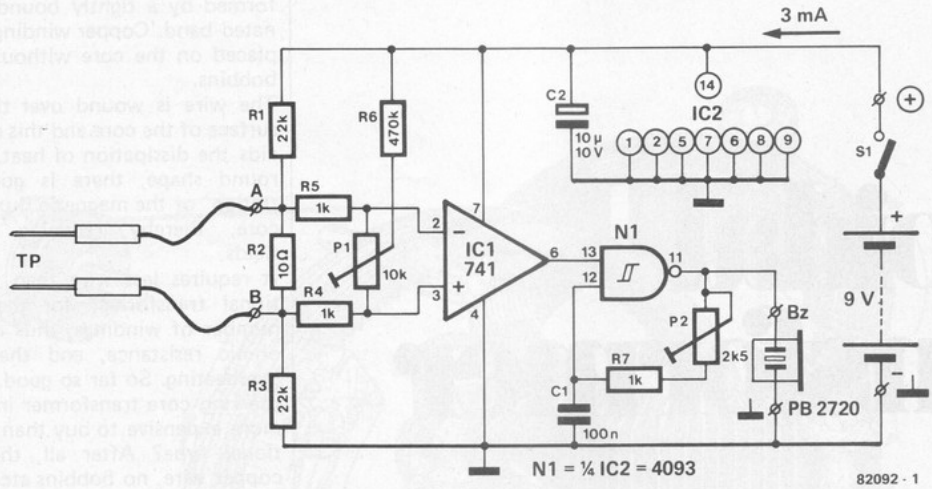


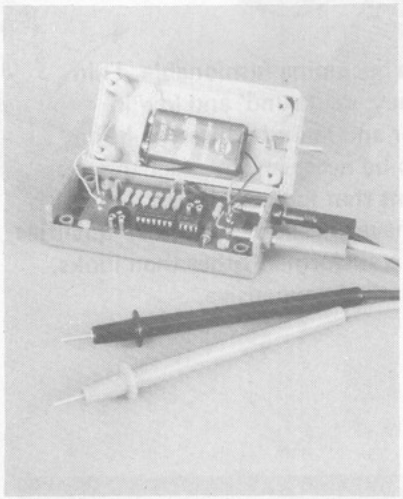
Parts list

Resistors:
R1,R3 = 22 k
R2 = 10 Ω
R4,R5,R7 = 1 k
R6 = 470 k
P1 = 10 k preset
P2 = 2k5 preset

Capacitors:
C1 = 100 n
C2 = 10 µ/10 V

Semiconductors:
IC1 = 741
IC2 = 4093

Miscellaneous:
Bz = buzzer Toko (Ambit)
S1 = on/off switch



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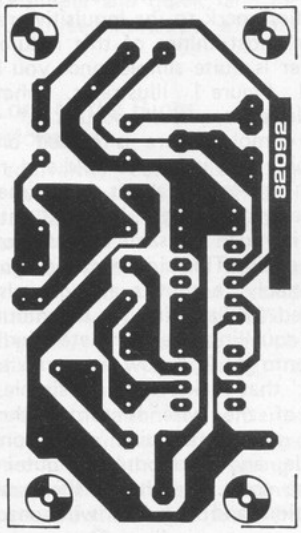
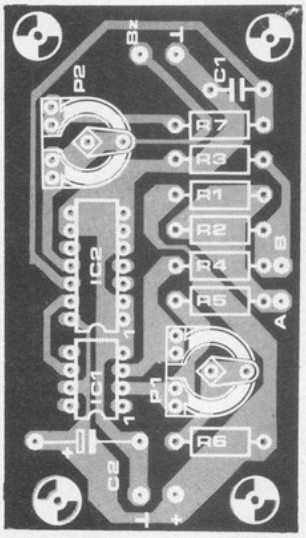




contact between the probes of the tester. P1 is used to calibrate the tester. Compared to an optical indication an acoustic indication is not only more convenient, but its current consumption can be lower as well. The buzzer is loudest when its resonance frequency is about 4.6 kHz. The current consumption will then be about 3 mA. The frequency, and therefore the volume, can be set with the aid of P2.

Calibration

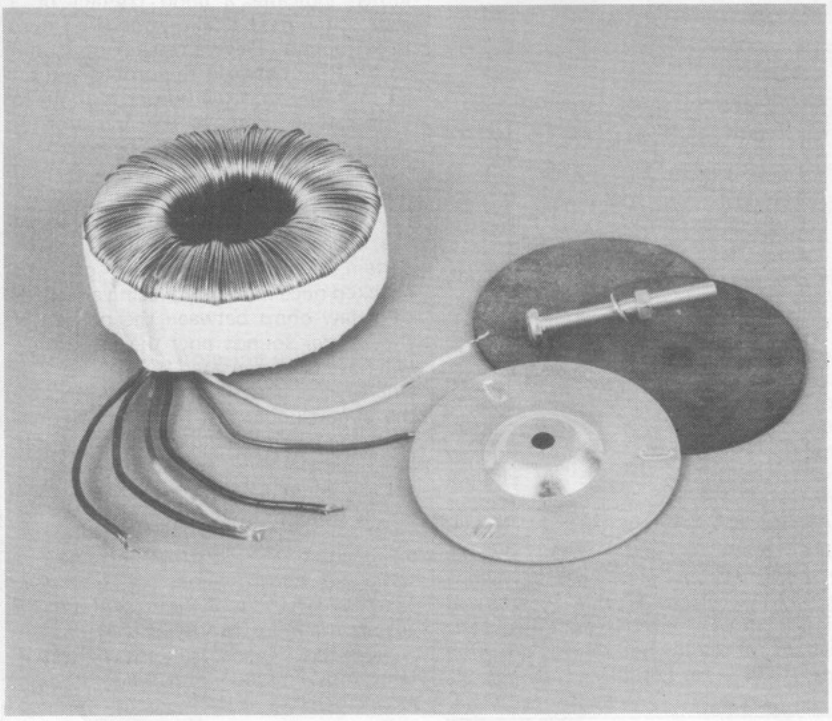
After correct calibration, only resistances of up to 1 ohm (in a connection) are tolerated. A value lower than 1 ohm either indicates a good contact or a short circuit. The calibration procedure is as follows: Place a resistor of 1 ohm (5 or 10%) between the probes and set P1 in a way that the buzzer is about to give a tone. Remove the 1 Ω resistor and cause a short circuit between the probes; again the buzzer will make itself noticeable. Volume can now be set with P2. When the short circuit is removed the buzzer must remain silent. To be certain, correct operation can be checked once more, by placing a resistor of a few ohms between the probes. If the buzzer sounds now the calibration will have to be repeated.

One final remark: The supply voltage of the circuit under test must be switched off when being examined with the tester described in this article. The supply voltage could have a negative influence on the tester or even damage it.

toroidal transformer

the best transformers . . . around!

Ring core or toroidal transformers are becoming fashionable. Thin is beautiful? As their name implies, they are 'round' and low in profile, allowing the home constructor and manufacturer, to build highly compact circuits. This seems to be necessary in order to satiate the public's appetite for any equipment that looks like a permanent 'Weight-Watcher'. Seriously, they do have excellent 'electrical' qualities, and advantages over the conventional transformer, other than looks. Unfortunately good taste is always relatively expensive.



The toroidal transformer has a ring core formed by a tightly bound metal laminated band. Copper windings are simply placed on the core without the use of bobbins.

The wire is wound over the complete surface of the core and this considerably aids the dissipation of heat. Due to the round shape, there is good 'concentration' of the magnetic flux lines in the core, thereby reducing the 'stray' fields.

It requires less wire than the conventional transformer for the equivalent number of windings, thus reducing the ohmic resistance, and the chance of overheating. So far so good. But why is the ring core transformer in most cases more expensive to buy than the conventional type? After all, they use less copper wire, no bobbins etcetera! Good question. The answer is that they take a lot longer to manufacture than conventional transformers, and today more than ever, time is money.

The core is formed as a complete ring without an air gap. It is made from a strip of high grade sheet steel, which is rolled up very tightly. The end of the strip is then welded, to prevent it unwinding. This form of construction helps to concentrate the lines of flux within the core and keeps losses to a minimum. An added advantage is its lack of buzz; due to the very tight 'laminations', which are completely enclosed by the winding. The result: an inbuilt disability for the production of noise.

Mains toroidal transformers are readily available in the 15 to 680 VA range, and up to 5000 VA types are supplied by some manufacturers. Most are available with two secondary windings, of between 6-60 V.

Winding toroidal transformers

The manufacture of toroidal transformers may present something of a question mark to the inquisitive reader. As in most things of this nature, the answer is quite simple; once you know how! Figure 1 illustrates, what, in simple terms, actually occurs.

The complete core is loaded onto a machine that is able to hold and, rotate it. A ring, that is about three times the diameter of the core, is linked onto the core in much the same way as two links of a chain. This ring is called, not unreasonably, a shuttle and can also be rotated. While doing so, an amount of wire equalling one complete winding is fed onto it. And now we come to the 'trick' that makes it all so simple. The end of the wire is turned through 180° around a guide wheel on the shuttle, and held onto the outer edge of the core. The shuttle then reverses direction and lays the wire onto the core as one winding. The core is of course rotated slowly as this happens, so that the winding is evenly spread around it. Tension of the wire is easily

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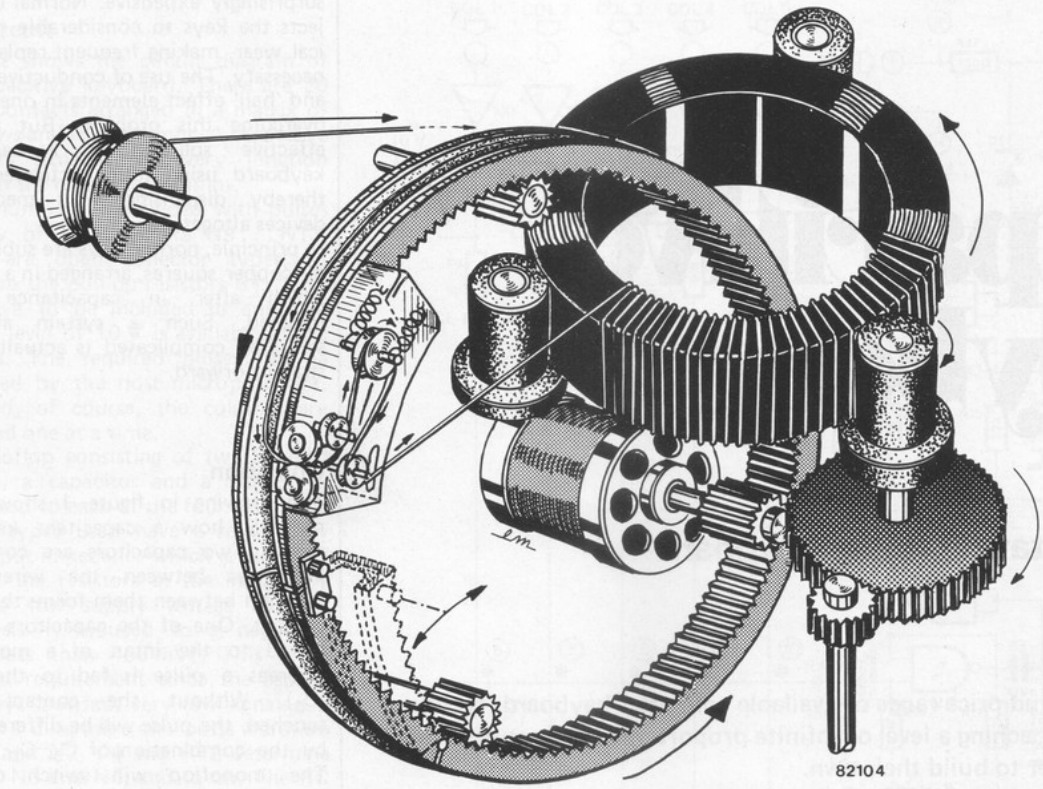


controlled. Mechanically this method is both simple and quick, and in fact takes just three minutes per winding.

The Lord of the Rings (Transformers)

The equivalent conventional transformer is in most cases 2 to 3 times heavier. The same ratio in size also holds true.

The ring core transformer's 'iron losses', (when compared with the 'standard' conventional type), are only 10%. The advantage of the ring type are clearly noticeable when comparing 'stray fields'.

In a no-load situation the conventional field is at a maximum and the ring core at a minimum. With an increasing load the 'stray field' of the conventional decreases and the ring core's field increases in strength.

No matter what the situation, the stray field of the ring core type is always considerably smaller. Therefore using a toroidal transformer reduces the risk of unwanted noise being generated in any power supply circuit.

Quality costs money?

Toroidal transformers up to power ratings of 200 VA are more expensive to buy than conventional types. Above 200 VA and up to 500 VA this situation is reversed. A reasonably priced, compact, transformer above 200 VA is certainly useful, especially when building high power amplifiers.

Final remarks

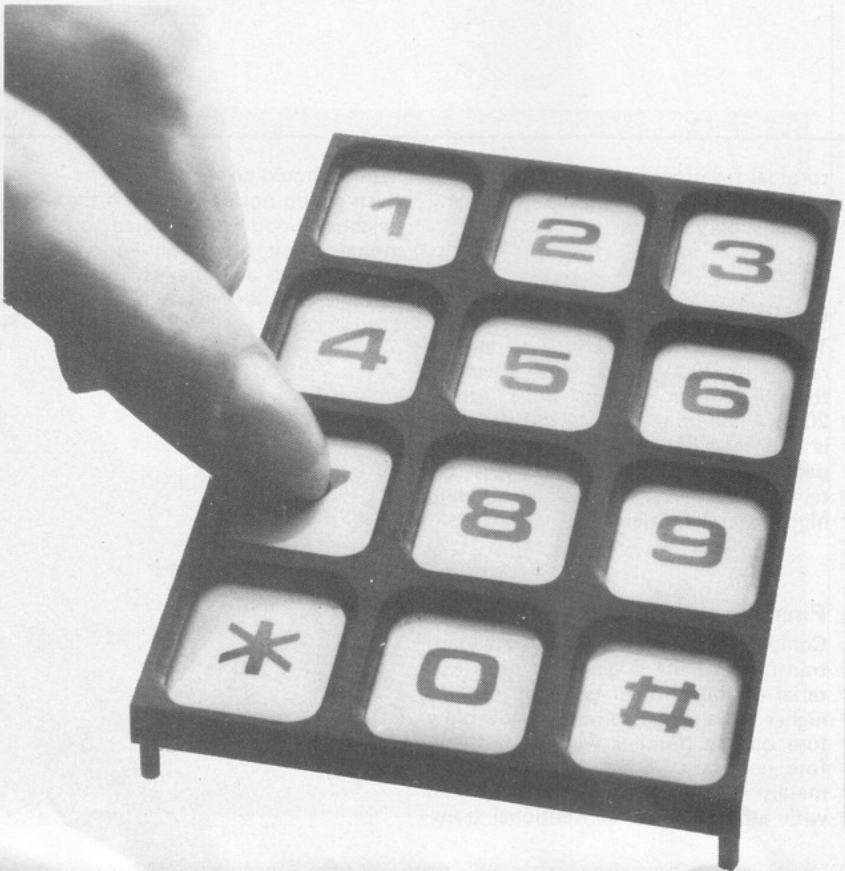
Compared to the ordinary standard transformer, the high-grade core material of the toroidal type will cause a higher initial surge current; A slow-blow fuse on the primary winding is therefore necessary. A fuse having approximately double the value normally used with an equivalent conventional transformer should do the trick.

Even so, do not be alarmed if the whole neighbourhood is 'blacked out' the moment you switch on your new 2 x 50000 . . . W amplifier (with multiple toroidal transformers). This is a normal occurance! ◀

capacitive keyboard

a solid state 'keyless keyboard'

The choice and price range of available computer keyboards is today swiftly approaching a level of infinite proportions. As a result, many readers prefer to build their own.
A system using mechanical keys, although being simple, is relatively expensive. Capacitive touch activated keyboards are an economical alternative. They achieve a high standard of reliability, without the need to use expensive conventional mechanical equipment.



Small, single-board microprocessor systems require a keyboard consisting of between 10 and 20 keys. Keyboards of this kind look very simple, but are surprisingly expensive. Normal use subjects the keys to considerable mechanical wear, making frequent replacement necessary. The use of conductive rubber and 'hall' effect elements in one way to overcome this problem. But a more effective solution is a capacitive keyboard using touch activated keys, thereby dispensing with mechanical devices altogether.
In principle, normal keys are substituted by copper squares, arranged in a matrix, which alter in capacitance when touched. Such a system although sounding complicated is actually quite straightforward.

Operation

The drawing in figure 1 shows, in a nutshell, how a capacitant keyboard works. Two capacitors are connected in series between the wires. The junction between them forms the touch contact. One of the capacitors (C_b) is linked to the input of a monoflop, whereas a pulse is fed to the other (C_a). Without the contact being touched, the pulse will be differentiated by the combination of C_a, C_b and R. The monoflop will switch on the leading edge of the differentiated waveform and will produce an output pulse with a specific length.
Touching the contact plate causes a leakage capacitant and/or resistance path to earth, which reduces the amplitude of the pulse to the monoflop to below its input trigger threshold. Consequently the monoflop does not generate an output pulse.
A complete keyboard can be operated along these lines. A short program makes sure pulses are generated and enables the system to detect any interruptions in the pulse flow (i.e. when one

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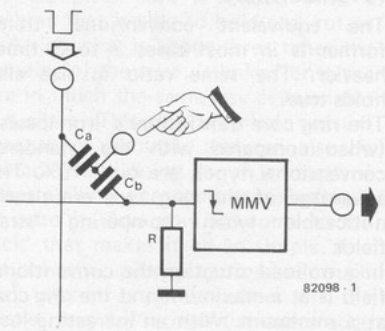

Figure 1. The basic principle behind a capacitive keyboard.

of the contacts is touched). The result is a economical, durable keyboard.

The circuit

Figure 2 shows the circuit diagram of the capacitive keyboard. There are 20 touch contacts arranged in a matrix of four rows and five columns. A capacitive 'key' is situated at every junction between the rows and columns.

The columns are provided with pulses by way of the inverters N9 . . . N13. These are open collector types, so therefore the pull-up resistors R1 . . . R5 will have to be included to ensure a voltage level of 10 V is available at the outputs. The required pulses can be generated by the host microprocessor, provided, of course, the columns are activated one at a time.

A monoflop consisting of two Schmitt triggers, a capacitor and a resistor, is connected to each of the four rows. The CMOS types used have a remarkably high input impedance which is cancelled out by the resistors at the inputs. By using a low supply voltage (3.3 V), hysteresis is reduced to a negligible level (less than 400 mV). This is an essential requirement since the capacitive 'keys' transmit very low signals. C2 and R14 determine the pulse duration of N1 and N2, C4 and R18 determine that of N3 and N4, and so on. The RC network connected to every monoflop input (C1/R12, C3/R16, etc) constitutes a high-pass filter that cuts down the circuit's sensitivity to hum, noise and other electrical interference. The transistors with an open collector output act as buffers/inverters at the monoflop outputs.

The potentiometers P1 . . . P4, at the inputs of the gates set the input pulse amplitude level. This will be at a point just below the trigger threshold level of the gate, providing that no contact at that particular junction is touched.

Since N9 . . . N13 invert the positive input pulses, the monoflops will switch on the leading edge of a pulse from CL1 . . . CL5. In order to clarify matters, several signal waveforms are shown in figure 3. As can be seen, a key was not touched until after the second pulse. Figure 3 also clearly indicates the DC voltage level which should be used.

Calibration

First of all, the wipers of P1 . . . P4 are turned to the positive end of the potentiometer. A squarewave voltage is then fed to CL1. P1 is adjusted slowly until the corresponding monoflop triggers on the arrival of a positive-going edge of the squarewave signal. Or in other words, upon the arrival of the negative-going edge to the input of N1. If a key belonging to that row is now touched, the monoflop should not switch. The potentiometer is now turned back a

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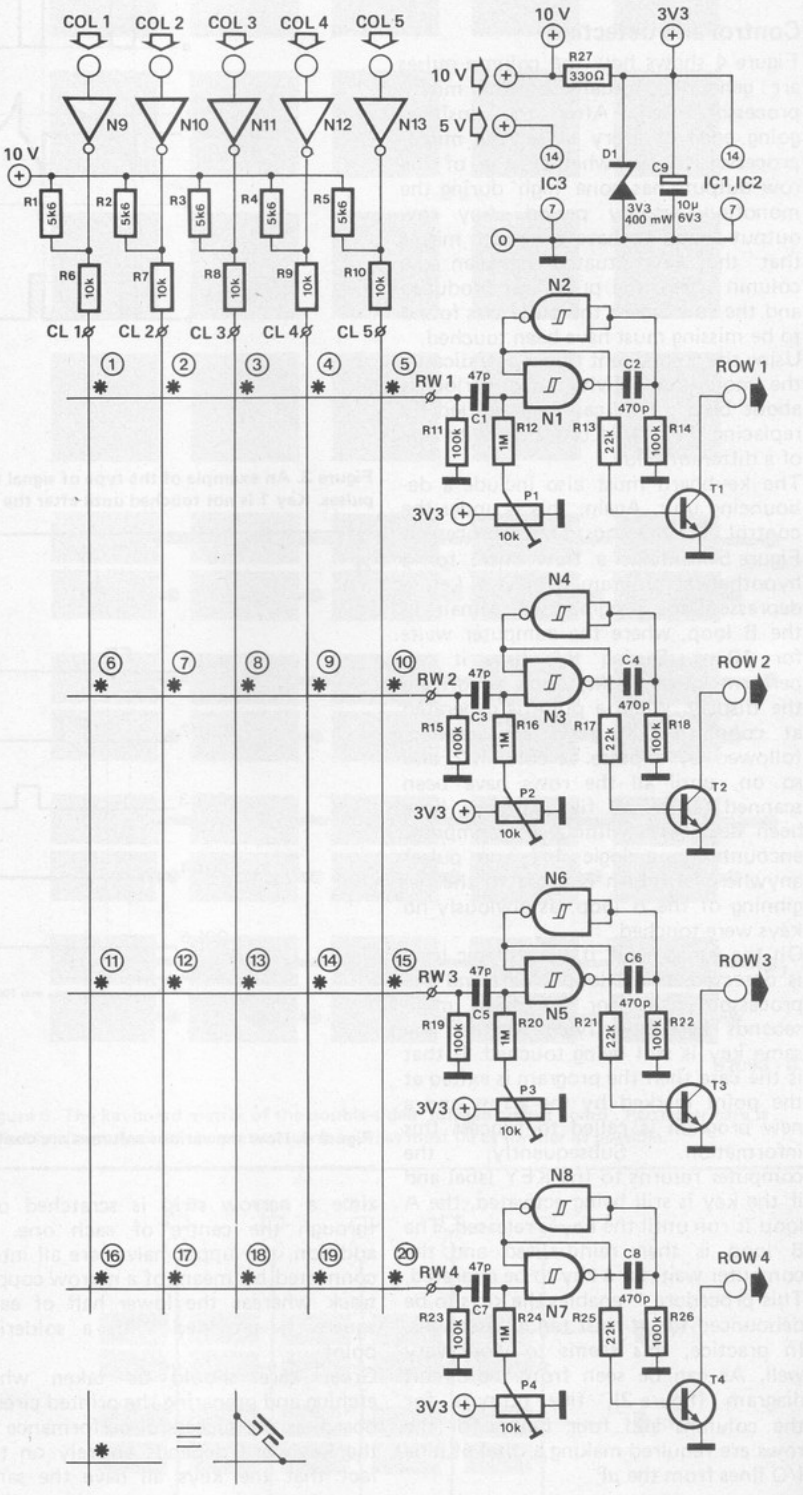

N1 ... N4 = IC1 = 4093B (RCA, MOTOROLA)
N5 ... N8 = IC2 = 4093B (RCA, MOTOROLA)
N9 ... N13 = 5/6 IC3 = 7406

T1 ... T4 = BC 547B

82098 - 2

Figure 2. Circuit diagram of a capacitive keyboard with 20 touch contacts. Very few components are required, since the host microprocessor looks after the control and detection.

little further, to the point at which the monoflop will be triggered when a 'key' is firmly pressed. The same procedure is carried out for each column in turn.

Control and detection

Figure 4 shows how the column pulses are generated, usually by the microprocessor used. After the positive-going edge of every pulse, the microprocessor checks whether one of the row outputs has gone 'high' during the monoflop activity period. Any row output found to have gone high means that the key situated between the column where the pulse was produced and the row where the pulse was found to be missing must have been touched.
Using the component values as indicated the monoflop activity time period is about 50 μs. This can be modified by replacing the 470 pf capacitor with one of a different value.
The keyboard must also include a debouncing unit. Again, this is under the control of the host microprocessor. Figure 5 contains a flow chart for a hypothetical program. Unless a key is depressed, the program will remain in the B loop, where the computer waits for 10 ms. During this time it can perform other tasks, such as driving the display. When a pulse is generated at column 1, the rows are scanned, followed by a pulse at column 2, and so on, until all the rows have been scanned. Once all five columns have been dealt with without the computer encountering a logic 1 (= no pulse) anywhere, a return is made to the beginning of the B loop, as obviously no keys were touched.
On the other hand, if a high logic level is detected, the B loop is left and the processor waits for 10 more milliseconds before verifying whether the same key is still being touched. If that is the case then the program is exited at the point marked by the arrow and a new program is called to process this information. Subsequently, the computer returns to the KEY label and if the key is still being activated, the A loop is run until the key is released. The B loop is then reinitialised and the computer waits for a key to be operated. This procedure enables the keys to be debounced for at least ten milliseconds. In practice, this seems to work very well. As can be seen from the circuit diagram (figure 2), five outputs for the columns and four inputs for the rows are required making a total of nine I/O lines from the μP.

The 'keys'

The keyboard is made using a piece of double-sided printed circuit board. Twenty copper squares (each 1.5 x 1.5 cm) arranged in a 4 x 5 matrix are etched onto the upper side, leaving a 5 mm space between each (see figure 6). Identical copper squares are then etched on the lower side of the board, in the same corresponding position, only this time a narrow strip is scratched out through the centre of each one. In addition, the upper halves are all interconnected by means of a narrow copper track whereas the lower half of each square is provided with a soldering point.
Great care should be taken when etching and preparing the printed circuit board, as the successful performance of the keyboard depends entirely on the fact that the keys all have the same capacitance. In order to achieve this, they must all have the same surface area, and they must be situated in identical relative positions on both sides of the printed circuit board.
The 'Keyboard' is shown in figure 6. Readers may feel that they wish to include the electronics on it. Once the board has been etched, the column soldering points are interlinked in the manner shown in figure 7. Again, a fair amount of care is called for. Thin copper wire can be used for this purpose.
The 'Keyboard' can be covered with a piece of transparant cellophane. Readers are invited to experiment with rub-on lettering.
It would be wise to recalibrate the Keyboard after it has been fitted in a case.
To ensure maximum protection, fit a metal plate about 2 cm below the keyboard. The plate should be parallel to the printed circuit board, otherwise some 'keys' may turn out to be more sensitive than others. The metal plate should be earthed to the case. Finally, keep the column and row connection wires as short, and as symmetrical as possible.
Readers are of course free to select any number of key they like. The performance of the circuit is largely depend-

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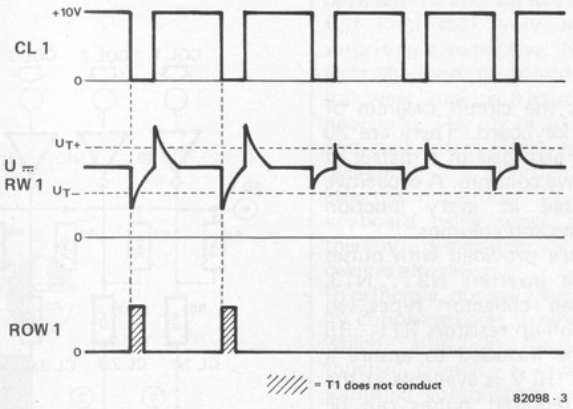

Figure 3. An example of the type of signal waveforms that occur when column 1 is fed with pulses. Key 1 is not touched until after the second pulse.

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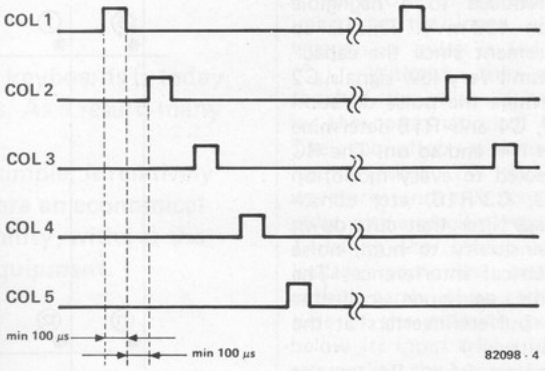

Figure 4. How the various columns are controlled.

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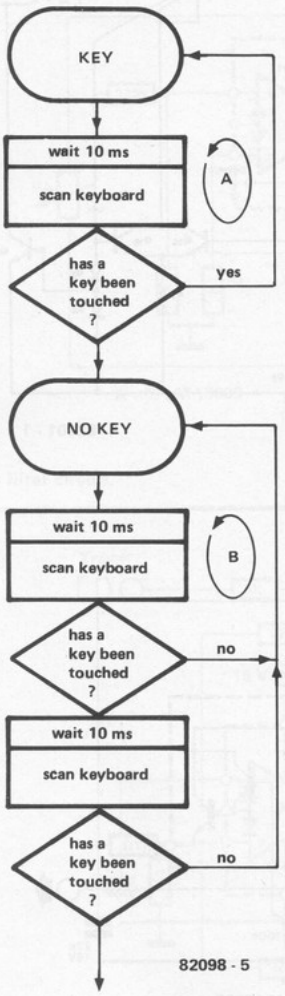

Figure 5. A program can be written on the basis of this flow chart for the purpose of scanning and debouncing the keyboard.

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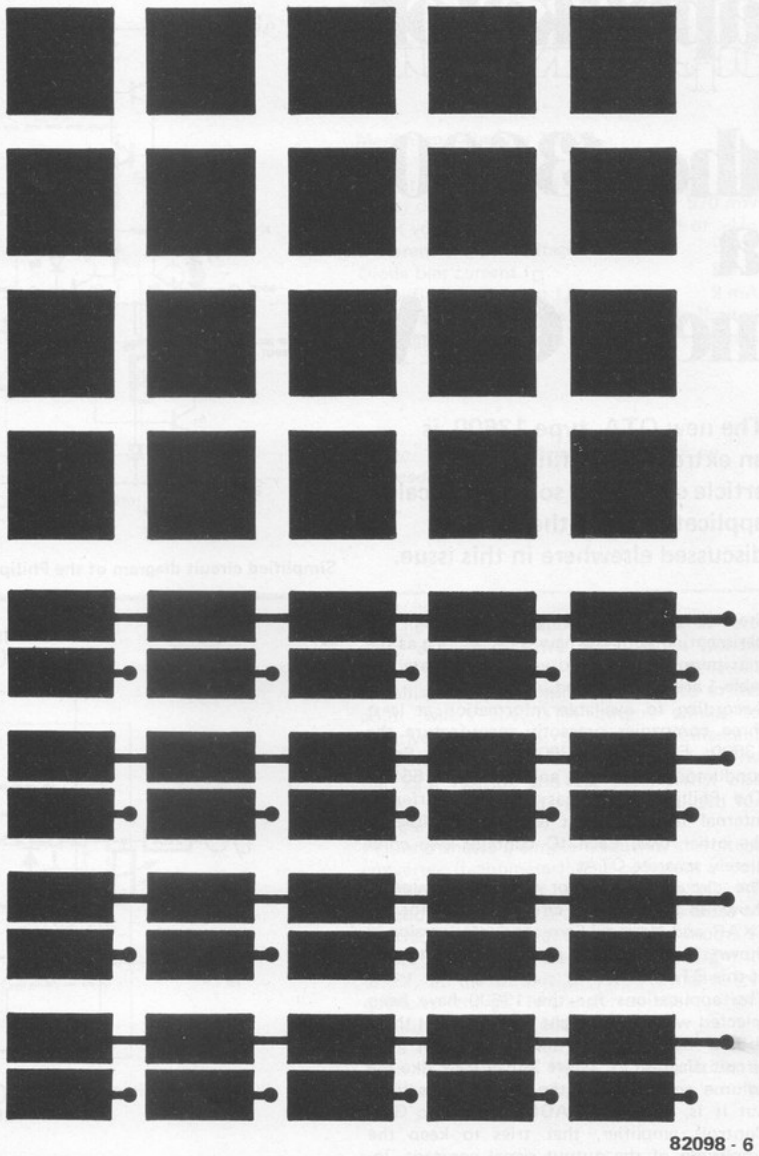

Figure 6. The keyboard matrix of the double-sided 'printed circuit board'. Particular care is called for here, since all the contact surface areas must be as similiar as possible.

ent upon the accuracy with which the keyboard is constructed. Readers can experiment with potentiometer settings and touch surfaces.

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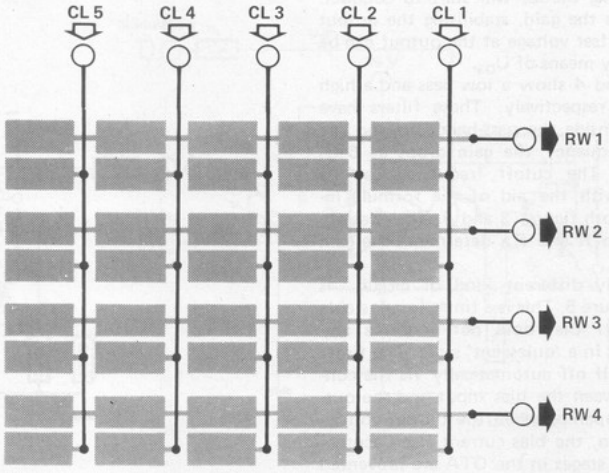

Figure 7. All the squares belonging to one column are interconnected by means of thin copper wire. The row squares are linked by copper tracks.

applikator

the 13600, a new OTA

The new OTA, type 13600, is an extremely useful IC. This article deals with some practical applications; the theory is discussed elsewhere in this issue.

Practically nothing can go wrong when experimenting with the new OTA, as long as the maximum currents and voltages indicated in table 1 are not exceeded.

According to available information at least three companies presently manufacture the 13600; EXAR (XR13600), National Semiconductor (LM13600), and Philips (NE5517). The Philips version has a slightly different internal layout, but it is pin-compatible to the other two. Each IC contains two completely separate OTAs.

The circuit diagram for the Philips type is shown in figure 1. The circuit diagram for the EXAR and National Semiconductor version is shown in the article describing the theory of this OTA.

The applications for the 13600 have been selected with the thought in mind, that there should be something for everybody. The circuit diagram in figure 2 may look like the volume control from the theoretical article, but it is, in fact, an AGC (Automatic Gain Control) amplifier, that tries to keep the amplitude of the output signal constant, independent of the input signal. Its operation is as follows; As soon as the output voltage is high enough, (more than three times the voltage at a PN junction), the darlington stage and linearising diodes will start to conduct. This reduces the gain, stabilising the output level. The offset voltage at the output can be set to zero by means of U_{OS}.

Figures 3 and 4 show a low pass and a high pass filter, respectively. These filters have unity gain inside the pass-band; beyond the turnover frequency the gain drops at 6 dB per octave. The cutoff frequency can be calculated with the aid of the formula indicated in both figures 3 and 4. The relationship between R and R_A determines the gain of the OTA.

A completely different kind of circuit is shown in figure 5. This is a timer (monostable multivibrator) that does not consume any power when in a 'quiescent' state. The timer switches itself off automatically via the connection between the bias input and the output of the opamp. When the output voltage drops to zero, the bias current also becomes zero and all stages in the OTA are prevented from consuming power. The timer is started with a positive pulse at the input. Provided the pulse is higher than 2 V, the OTA will be switched on, and its output will swing high.

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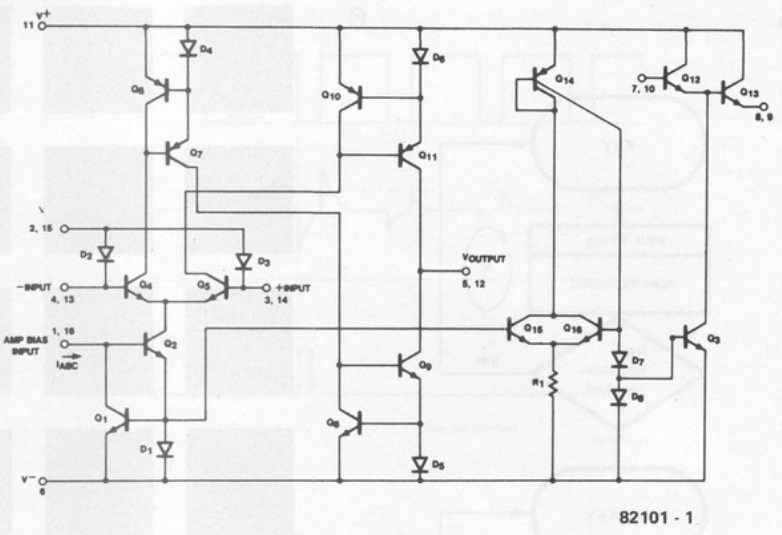

Simplified circuit diagram of the Philips NE 5517.

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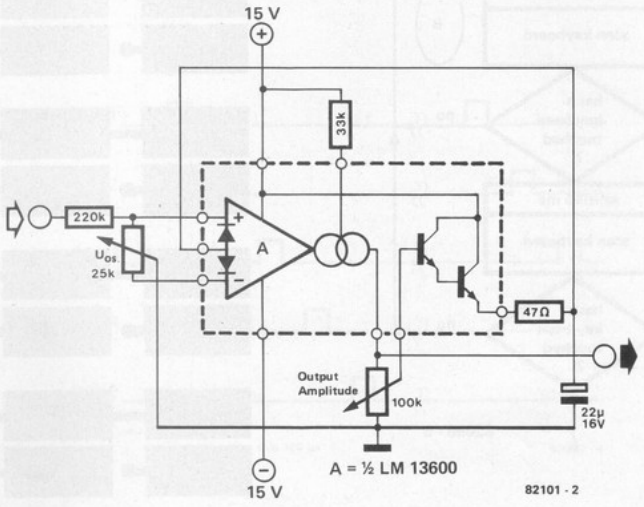

Automatic gain amplifier (AGC).

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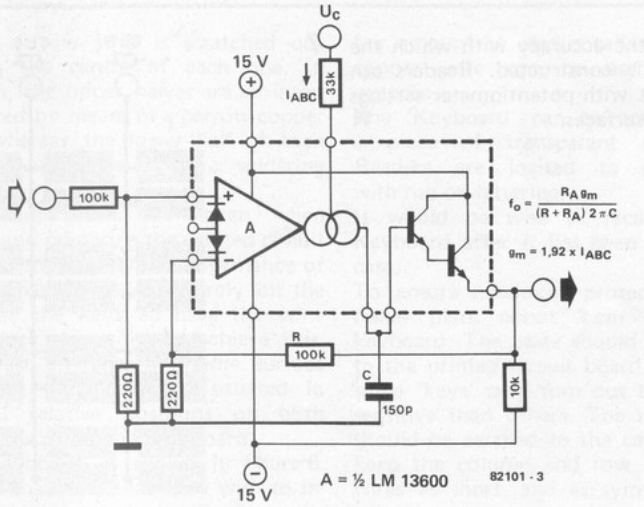

Low-pass filter circuit.

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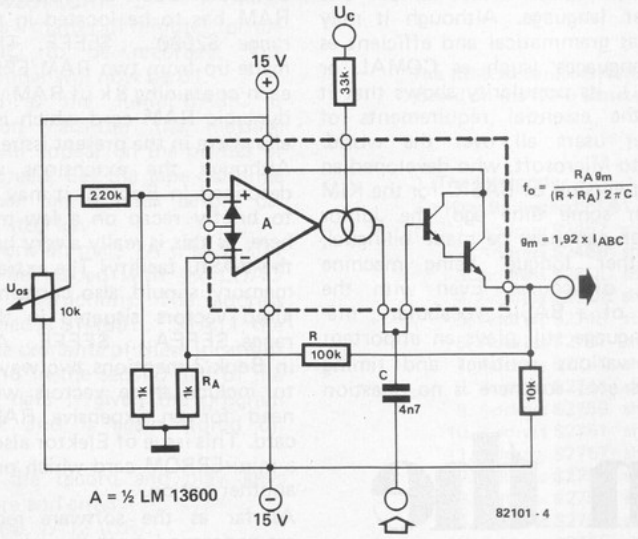

High-pass filter circuit.

Table 1

Maximum values for 13600

Operational voltage U_B:	36 or ± 18 V
Power dissipation:	570 mW
Input voltage:	+ or $-U_B$
Differential input voltage:	± 5 V
Diode bias current I_D:	2 mA
Amplifier bias current I_{ABC}:	2 mA
Amplifier output current:	internally limited
Darlington stage output current*:	20 mA

** Note: The power dissipation may not be exceeded!*

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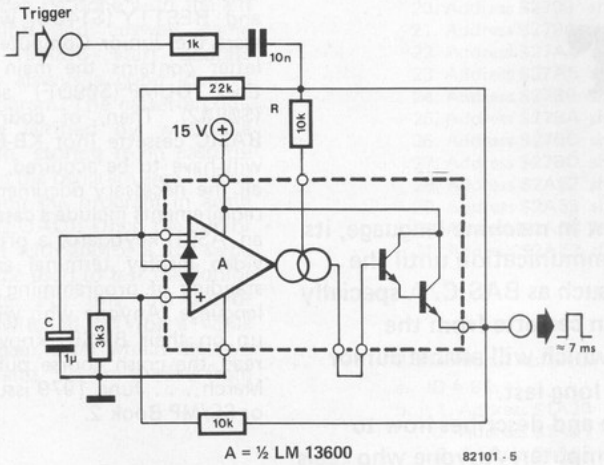

Circuit of a timer (monostable multivibrator).

The non-inverting input will remain at zero volts, and the positive output pulse will be fed to the inverting input. This situation remains, until capacitor C has charged to the point where the OTA output swings to negative again, thus restoring the quiescent condition. Capacitor C is discharged both via the 22 k resistor and via the internal bias diode, which should not really be used for this purpose.

Figure 6 shows a simple frequency-to-voltage converter (tachometer). The complete circuit can be constructed with a single IC. A1 functions as a comparator. In some cases an interface may be required at the input. A square wave voltage transfers 'charge' from Ct to Cf, at the output of A1. At higher frequencies 'charge' is transferred more often, resulting in a higher output voltage.

As a final application, an amplitude modulator is shown in figure 7. Modulation is obtained by varying the gain.

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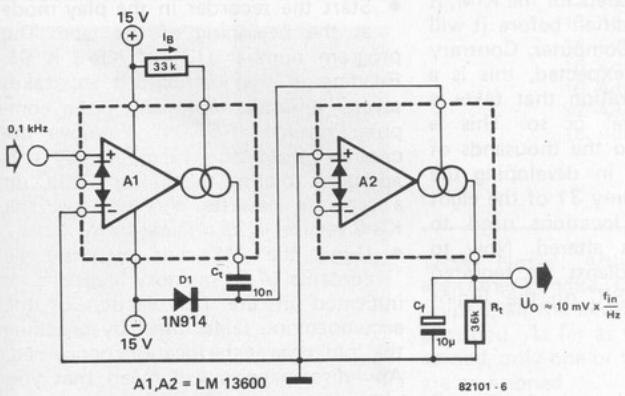

A simple tachometer.

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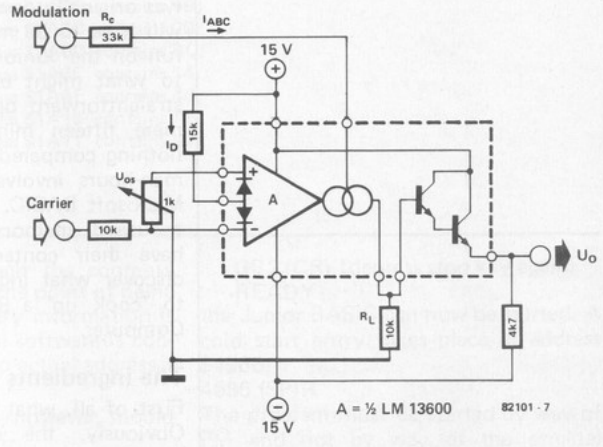


An amplitude modulator.

BASIC on the Junior Computer

. . . puts the microprocessor in touch with the world

Although the Junior Computer is quite fluent in machine language, its linguistic skills cannot lead to full 'adult' communication until the machine has learned a 'high level' language, such as BASIC. A specially adapted version of BASIC is now available on cassette from the Microsoft/Johnson Computer Corporation, which will enable Junior Computer operators to fulfil their dreams at long last.
This article introduces the Microsoft cassette and describes how to implement the new facility on the Junior Computer. Anyone who feels that their BASIC has become rather 'rusty' will welcome the opportunity to brush up their knowledge. As for beginners, it is never too late to learn!

BASIC still remains the number one computer language. Although it may not be as grammatical and efficient as other languages (such as COMAL or PASCAL), its popularity shows that it meets the essential requirements of computer users all over the world. Thanks to Microsoft, who developed an excellent version of BASIC for the KIM computer some time ago, the Junior Computer can now be made bilingual, its 'mother tongue' being machine language of course. Even with the addition of a BASIC vocabulary, machine language still plays an important role in various routines and timing processes etc., so there is no question of it being completely replaced.

The KB-9 BASIC by Microsoft is a nine digit 8k BASIC on cassette. Since this was originally developed for the KIM, it will have to be modified before it will run on the Junior Computer. Contrary to what might be expected, this is a straightforward operation that takes a mere fifteen minutes or so. This is nothing compared to the thousands of man-hours involved in developing the Microsoft BASIC. Only 31 of the eight thousand memory locations need to have their contents altered. Now to discover what ingredients are required to 'cook up' a BASIC on the Junior Computer.

The ingredients

First of all, what about the hardware? Obviously, the computer will have to be a fully extended version, that is, equipped with an interface board and extended memory. How this is accomplished is fully described in Junior Computer Book 3. In addition, 16k of RAM has to be located in the address range $2000 . . . $5FFF. This can be made up from two RAM/EPROM cards each containing 8k of RAM, or the 16k dynamic RAM card which is described elsewhere in the present issue.

Although the extensions were fully described in Book 3, it may be an idea to briefly recap on a few main points here, as this is really a very basic part of the BASIC facility! The extra bus board memory should also contain the three jump vectors situated in the address range $FFFA . . . $FFFF. Appendix 3 in Book 3 mentions two ways in which to include these vectors without the need for an expensive RAM/EPROM card. This issue of Elektor also describes a mini EPROM card which provides yet another option.

As far as the software requirements are concerned, both the printer monitor (PM) and the tape monitor (TM) routines must be available. The former contains the input/output subroutines RECCHA ($12AE), PRCHA ($1334) and RESTTY ($14BC) which serve to start the Junior Computer BASIC. The latter contains the main cassette routines DUMP ($Ø9DF) and RDTAPE ($ØBØ2). Then, of course, the KB-9 BASIC cassette (not KB-6 nor KB-8!!) will have to be acquired, together with all the necessary documentation. Other requirements include a cassette recorder, an ASCII keyboard, a printer and/or a video display terminal and an understanding of programming in the BASIC language. Anyone who wishes to brush up on their BASIC knowledge should read the crash course published in the March . . . June 1979 issues of Elektor or SC/MP Book 2.

The recipe

- Switch on the Junior Computer and start up the PM routine. Place the KB-9 cassette in the tape recorder:
RST 1 Ø Ø Ø GO RES
G1 (CR)
- Start the recorder in the play mode at the beginning of the tape. The program number (ID) of KB-9 is Ø1. Reading in the instructions etc. takes several minutes, after which the computer reports 'READY'. Remove the cassette from the recorder as it is advisable to store the Junior BASIC on a separate cassette and preserve the KB-9 version in its original form.
- Using the PM routine, alter the contents of 31 memory locations, as indicated in the first section of the accompanying table. Start by checking the 'old' data at the locations concerned. Any discrepancies will mean that you have been landed with the wrong version of BASIC!
- Place a new cassette in the recorder. Start at the beginning, reset the counter and depress the record and play buttons. After about ten seconds enter:

SB1, 2ØØØ, 4261 (CR)
It only takes a matter of minutes for the Junior BASIC to be recorded. The program number will now be B1.

- As soon as the Junior BASIC is stored on cassette, the message 'READY' will appear on the printer or the video screen. Let the tape continue for a further ten seconds before depressing the stop key.
- 18 locations on page 1A (PIA RAM) need to be loaded with six LOAD and SAVE instructions. The address area concerned is $1AØØ . . . $1A11; the details of the contents of these locations can be found in the second half of the table. This data is given the program number B2 and is again stored on cassette.
- Depress the record and play keys once more and enter:
  SB2, 1AØØ, 1A12 (CR).
- After the 'READY' message, the cassette recorder can be stopped.

Now it is time to check whether the Junior BASIC is correctly stored in memory. This can be done with the aid of the 'question and answer' game following the BASIC start address ($4Ø65). It is always a good idea to enter a test program. The cassette commands can be verified by writing a BASIC program, storing it on cassette (SAVE), erasing the program area (NEW) and then reading the program in again from cassette (LOAD). Once the Junior BASIC has met with approval, the same procedure can be used to test the Junior BASIC cassette. For this, the Junior Computer is switched off for a while and then on again, after which the two programs (B1 and B2) are loaded from cassette.

Ready to serve

By now the operator is all set to dish up the Junior Computer BASIC. Do not forget to read the manual supplied with the cassette. This consists of the 'Microsoft Introduction', 'Dictionary' and 'Usage Notes'. Although the contents are rather concise, to the point of being cryptic, all the necessary information is provided. As far as the software is concerned, only one or two actual addresses are mentioned.

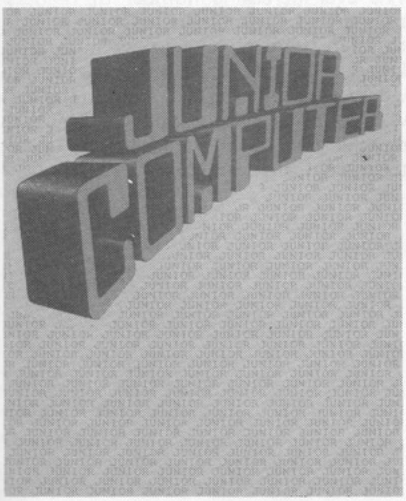
The following remarks, however, should make things a bit clearer:

1) After entering:
   RST 1 Ø Ø Ø GO RES (RUBOUT)
   GB1 (CR)
   READY (depress stop key)
   GB2 (CR) (depress stop key again)
   READY

the Junior BASIC can now be started. A cold start entry takes place at address $4Ø65.

4Ø65 (SP)R

The program must be started by way of PM and not by way of the original monitor routine, as otherwise the input/output parameters will be incorrectly defined. In any case, PM is indispensable for reading in data.



The KB-9 to Junior BASIC conversion table
(based on the KB-9 cassette, # 4065 © 1977 by Microsoft Co.; version V1.1).

1. The interpreter

a. ID = B1 instead of Ø1.

b.
1. Address $2457 should contain AE instead of 5A;
2. Address $2458 should contain 12 instead of 1E;
3. Address $26DD should contain 8Ø instead of 4Ø;
4. Address $26DE should contain 1A instead of 17;
5. Address $2746 should contain 79 instead of F9;
6. Address $2747 should contain 1A instead of 17;
7. Address $274D should contain 7Ø instead of F5,
8. Address $274E should contain 1A instead of 17;
9. Address $275Ø should contain 71 instead of F6,
10. Address $2751 should contain 1A instead of 17;
11. Address $2757 should contain 72 instead of F7;
12. Address $2758 should contain 1A instead of 17;
13. Address $275A should contain 73 instead of F8;
14. Address $275B should contain 1A instead of 17;
15. Address $275E should contain 1A instead of 18,
16. Address $2791 should contain 7Ø instead of F5;
17. Address $2792 should contain 1A instead of 17;
18. Address $2794 should contain 71 instead of F6;
19. Address $2795 should contain 1A instead of 17;
20. Address $2799 should contain 79 instead of F9;
21. Address $279A should contain 1A instead of 17;
22. Address $27A4 should contain Ø9 instead of 73;
23. Address $27A5 should contain 1A instead of 18;
24. Address $27B9 should contain FA instead of ED;
25. Address $27BA should contain ØØ instead of 17;
26. Address $27BC should contain FB instead of EE;
27. Address $27BD should contain ØØ instead of 17,
28. Address $2A52 should contain 34 instead of AØ;
29. Address $2A53 should contain 13 instead of 1E;
30. Address $2AE6 should contain AE instead of 5A;
31. Address $2AE7 should contain 12 instead of 1E.

2. Additional instructions on page 1A

a. ID = B2.

b.
1. Address $1AØØ contains 2Ø;
2. Address $1AØ1 contains DF;
3. Address $1AØ2 contains Ø9,
4. Address $1AØ3 contains 2Ø;
5. Address $1AØ4 contains BC;
6. Address $1AØ5 contains 14,
7. Address $1AØ6 contains 4C;
8. Address $1AØ7 contains 48;
9. Address $1AØ8 contains 23;
10. Address $1AØ9 contains 2Ø;
11. Address $1AØA contains Ø2;
12. Address $1AØB contains ØB;
13. Address $1AØC contains 2Ø;
14. Address $1AØD contains BC,
15. Address $1AØE contains 14;
16. Address $1AØF contains 4C;
17. Address $1A1Ø contains A6;
18. Address $1A11 contains 27.

2) The Junior BASIC utilises the following memory range on page zero: $ØØØØ . . . $ØØDC and $ØØFF. Thus one of the locations (MODE) belonging to the original monitor is used. This merely serves to start PM.

3) The start address for a warm start entry is $ØØØØ. In the KIM the warm start entry allows the computer to return to BASIC after writing or reading a BASIC program to or from cassette. In the case of the Junior Computer things are slightly different (see point 9). Here, the warm start entry may be used to return to BASIC from PM. The jump from BASIC to PM occurs either as a result of a non-maskable interrupt (NMI) or because the BREAK key on the ASCII keyboard was depressed. The BRK jump vector points to the label LABJUN ($1Ø5F) of the PM routine. After printing the text 'JUNIOR', the computer jumps to the central label RESALL of PM (see Book 4 chapter 14). In the event of an NMI, RESALL is reached at the end of the STEP initialisation routine ($14CF).

4) The ST key may be used during PM to examine the contents of various memory locations, such as the ones on page zero (see point 2) for instance. A warm start entry heralds the return to the BASIC program.

5) Supposing the operator is executing a BASIC program (RUN) making use of the Elekterminal (up to 16 lines on the display) and the BASIC program turns out to contain more than 16 lines. This is what should be done:

RUN (CR)
BRK (while 16th line is being printed)
examine result
(SP) R The computer prints
OK Start the program again: RUN (CR) enter the 16th and following 14 lines, etc.

6) When starting the Junior BASIC by way of a cold start entry, the operator will be requested to state the 'TERMINAL WIDTH'. If the Elekterminal is being used, this is set at 64 (CR).

7) The ASCII keyboard does not provide a '↑' nor a '^' key necessary for power functions, where A↑4 corresponds to A^4. What is required is an ASCII key which generates the code $5E. This can be improvised by sacrificing another key. One contact is connected to row x7 and the other to column y9 in the keyboard matrix (pins 32 and 22 of IC1). Only two keys are suitable: the 'PAGE↑' key at the far right in the top row and the 'ESC' key at the far left in the second row. The latter affords the most elegant solution, as the ESC function is preserved (a matter of combining it with the Shift key). Interrupt the two connections x5 and Y10 (without actually cutting the wires!) and link the ESC key to pins 22 and 32 of IC1. Further details are provided in the article concerning the ASCII keyboard (Elektor November 1978), in Book 3 of the Junior Computer series and in SC/MP Book 2.

8) In order to start the Junior BASIC by way of a fresh cold start entry during a computer session, the program (file B1) will have to be loaded from cassette all over again. This is necessary as a relatively large section of data block B1 is reserved as the first section of the BASIC work area if any trigonometric functions are required. After the cold start entry, the computer will request the operator to specify its task. Whether trig functions are to performed or not, the computer must be informed by way of a cold start entry, (once B1 has been loaded again).
N.B. In file B1 ($2ØØØ . . . $426Ø), locations $4Ø41 . . . $426Ø are added to the user work space if the operator wishes to utilise the trigonometric functions (depress the Y key); locations $3F1F . . . $426Ø are added to the user work space if the trig functions are not required (N key); locations $3FD3 . . .$426Ø are added if the ATN function (A key) is cancelled.
The first memory location is loaded with ØØ (BOF: Beginning Of File). Now that 16k of RAM has been added, the user work space will cover the following ranges:
$4Ø42 . . . $5FFF (8126 bytes) when Y is depressed;
$3F2Ø . . . $5FFF (8416 bytes) when N is depressed;
and $3FD4 . . . $5FFF (8236 bytes) when A is depressed.

9) Thanks to the Junior Computer subroutine system, reading and writing BASIC programs to and from cassette (SAVE and LOAD) is much easier than with the KIM BASIC. The only snag is that this occupies the second file, B2. After SAVE has been entered, the BASIC program is stored on tape (where ID = FE). After a while, the 'OK' message will appear followed by an empty line. After LOAD (CR) is entered, a BASIC program is read from tape (where ID = FF, so make sure the required BASIC program is stored *before* this!). A little later 'LOADED' is printed. This is not followed by the message OK and the computer does not start a new line. In other words, the video screen will display 'LOADEDLIST' if the entered program is to be checked.

Any questions?

Here are the answers to one or two questions which are likely to be asked:

1) Elektor cannot comply with requests for a copy of the notes accompanying the Microsoft/Johnson BASIC cassette as this would be an infringement of copyright.

2) The source listing of the KB-9 costs a few thousand dollars. Not surprisingly, Elektor is not in a position to sell it to readers.

3) The KB-9 BASIC cassette should be available from Calist Computers Ltd. 119 John Bright Street Birmingham B1 1BE Tel. 021/63 26 458. ◀

coming soon...

Many new projects and designs are on the way, with subjects ranging from audio to microprocessors. In keeping with the policy of Elektor every reader will find something to his liking. Here are some of the projected articles:

For the musician the guitar premplifier would be of interest. This is a sophisticated circuit including such facilities as active tone controls, equalisation, reverb, fuzz, and many more.

Part two of the polyformant enables readers to start building. Provides constructional details together with the printed circuit board designs.

The motorist is also catered for: the auto burglar alarm. An alarm with an automatic reset facility. It does not matter how many attempts are made to break in, the alarm is always ready.
A versatile counter that can be used for many different applications as well as a lap counter for Slotcar racing.

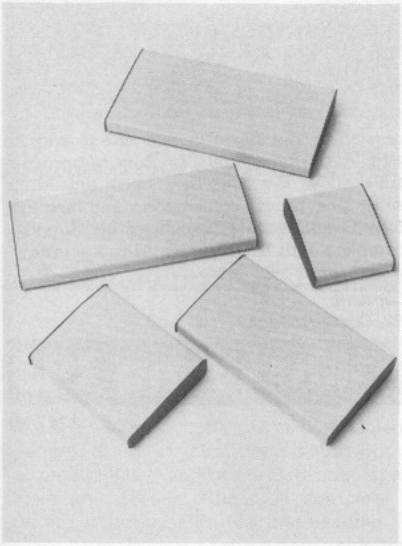
Readers whose prime interest is R.F may breathe a sigh of relief. A 20 metre S.S.B. receiver comparable in performance with professional equipment, without costing the earth.

The ever-increasing number of readers having home computers will find plenty to keep them busy. As regular readers know, Elektor stays one step ahead where electronics is concerned, and we will continue to produce articles and designs keeping in step with the latest technological advances.

market

Bimconsoles

Recently introduced by BOSS Industrial Mouldings Ltd their new BIM 2600 range of small and medium size desk consoles are ideally suited to applications where meters, keyboards or switches are incorporated, with adequate space also being available on the side and rear panels for mains sockets and connectors etc.



Ranging in size from 178 x 210 mm to 483 x 261 mm and with an overall height of 51 mm, these sloping front units have been ergonomically conceived to permit comfortable operation of switches etc, yet still offer excellent display visibility.
Utilising a two piece, all aluminium, construction in which the base and top are nominally 2 mm and 1.6 mm thick respectively, the standard colour scheme is brown base and beige top panels, with the whole unit held rigidly together by screws running through base rubber feet into hank bushes. Alternative colour schemes, together with special ventilation slots, keyboard cut-outs or switch punchings etc. can be included, subject to normal commercial viability criteria.

Boss Industrial Mouldings Ltd.,
James Carter Road,
Mildenhall,
Suffolk IP28 7DE,
Telephone: 0638 716101

(2294 M)

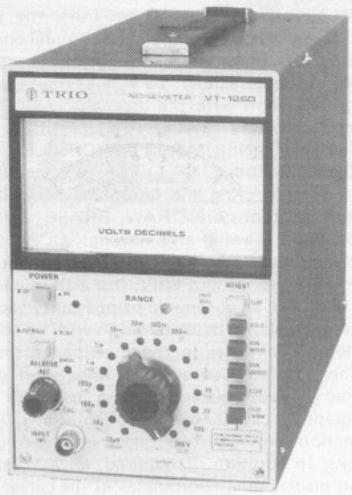
Quad FM4 tuner

Designed primarily as an adjunct to the Quad 44, the Quad FM4 uses advanced micro circuitry to provide exemplary audio performance combined with simplicity and ease of handling. Once the Quad FM4 is programmed,

the listener has only one decision to make: Which station to listen to? Once he has pressed the appropriate button the microprocessor takes over, recalls the required station from memory and tunes it in accurately taking care of muting and A.F.C. Manual tuning used principally when programming the seven presets and occasionally to tune in a station not already programmed, is very easy to operate.
A conventional tuning knob is used to find the desired frequency which is shown in figures. A bar graph which displays signal strength and centre tune simultaneously ensures accurate tuning. There are no controls on the FM4 apart from the preset buttons and tuning knob. The microprocessor controls all other functions.

Quad Electroacoustics Ltd.,
Huntingdon,
Cambs., PE18 7DB,
Telephone: 0480 52561

(2299 M)



Ultra sensitive noise meters

Noise meters are ultra sensitive electronic voltmeters with a wide frequency bandwidth and a range of selectable 'weighting' filters enabling the measurement of noise level, S/N ratio, O/P voltage and frequency response in accordance with various standards. VT126 and VT125 are two new noise meters with full scale sensitivities of 10 microvolts to 300 volts (VT125 30 microvolts). VT126 has a 0.2 microvolt graduated scale for measurements down to –120 dB. Both new units have pushbutton selection of JIS-A, DIN NOISE, DIN AUDIO, CCIR and CCIR/ARM weighting filters enabling noise and S/N measurements in accordance with the relative standard. In addition to average detection and RMS display, DIN and CCIR semi-peak detection with RMS display is also available. AC OUT and DC OUT terminals are provided for waveform observation, recording measured values or for use as an amplifier.
Relative reference adjustment from 0 to 10 dB makes possible relative measurements of signals with respect to an arbitrarily set reference level which is particularly useful in measuring S/N. An over-load indication prevents measurement errors caused by undetected distortion. Options include the provision of remote logic control of range selection with, if required, a remote control unit.
Both units measure only 128 (W) x 190 (H) x 285 (D) mm and weigh approximately 4.6 kg.

Clifton Chambers 62,
High Street,
Saffron Walden,
Essex CB10 1EE,
Telephone: 0799 24922

(2289 M)

market

market

Low cost computer graphics with Robocom BIT STIK

Designed and produced by the robotics research and development company, Robocom Ltd of London N4, this new hardware/software package enables microcomputer users to create multi-colour graphics, sketches, technical drawings, electronic circuit diagrams, typography, etc.

Apart from opening up new creative possibilities, the precision of the BIT STIK hardware and speed of its machine-coded, user-friendly software, facilitates drawing and the inputting of information for any personal or business user of a microcomputer. The software package included in the system also allows originated creative material to be manipulated and replayed at will.

Once the software has been loaded from the DOS 3.3 disc provided, the user can draw directly on the video screen using the BIT STIK as the only input. A comprehensive MENU can be called at the edge of the screen and accessed simply by 'pointing' to the required items with the drawing cursor. The menu provides PALLETTE facilities for automatic LINES, ARCS and CIRCLES, six COLOURS, four LINE TYPES, plus a variable NIB for colouring and lettering. The MENU mode selections are DRAW, ERASE, ZOOM (for detail drawing and viewing), COPY (for reducing and compiling), FIND (locks onto a particular point) and WIPE (for a clean page). In addition, an automatic paint facility allows line drawings to be coloured in with up to 16 colours. To assist in the drawing of three-dimensional views, parallel lines, and grid based layouts such as those used in typography, circuit diagrams, etc., a LOCK function provides two angle and two grid locks. In addition, if required, an X,Y selection displays the coordinates of the cursor on the VDU for exact positioning whilst actually drawing.

A secondary MENU can also be selected in order to SAVE and LOAD drawings onto floppy disc. In this way a file of drawings can be built up with easy access for use as components of other drawings. Selections are also available to TEXT IN GRAPHICS (positions text at any scale, angle and colour in a drawing) DIMENSION (for dimensioning technical drawings) and ANIMATE which allows for the dynamic recording and replay of a series of drawings.

Two PAGES are available at any time, either can be used for direct drawing or to hold components or scaled parts of the work in hand. Finally a memory COUNTER is provided to indicate the available workspace and a valuable COMPRESS function allows drawings to be squeezed into the minimum memory space.

An integral function of the system is the ability to retain hidden detail. A single page can in fact hold up to 16,000 pages of information which can be viewed by zooming in on specific areas, the additional detail being called from the disc as required.

PAPER COPIES of drawings created with the BIT STIK graphics system can be produced on any X-Y plotter, by inserting a short interface programme. The resolution of the drawings is limited only by the capabilities of the plotter, not the original video page.

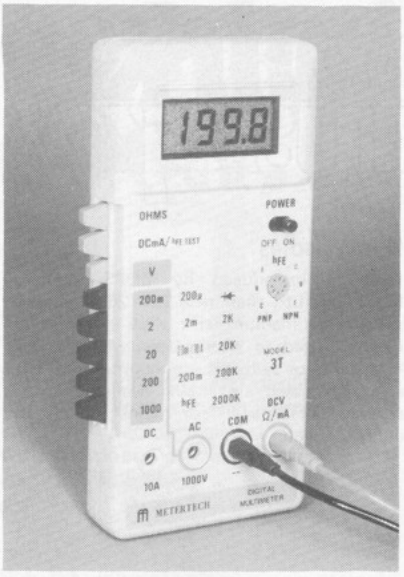
A fully illustrated user-friendly MANUAL is provided. As well as containing easy-to-follow instructions and examples of how to get the best out of the BIT STIK system, information on writing programs and using drawings in other routines is given.

Robocom Ltd.,
CIL Trading Estate,
Fonthill Road,
London N4.
Telephone: 01 263 3388

(2291 M)

LCD multimeter

The Model 3T is a battery operated 3½ digit hand held digital multimeter with a bold 0.5" liquid crystal display. The meter provides six functions in 16 ranges permitting measurement of DC voltages, AC voltages, DC current,



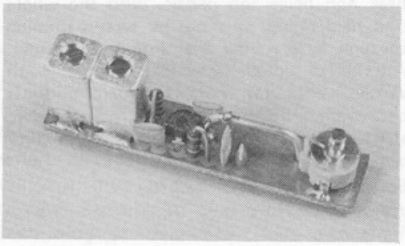
resistance, diode/continuous check and an HFE measurement facility. Push button controls allow fast and easy operation whilst small size, robust construction and long battery life make the 3T truly portable. Supplied complete with battery, test leads and instruction manual.

Centemp,
62, Curtis Road,
Whitton.
Hounslow.
Middlesex TW4 5PT

(2247 M)

Miniature UHF tuned preamplifier

The TE/435P is a tiny UHF preamplifier that employs a tuned line on the input, and a twin chamber helical filter on the output. In view of the ever-increasing numbers of both VHF and UHF communications systems, it is increasingly important for antenna preamplifiers to use tuned selectivity to avoid intermodulation and spurious products appearing at the main receiver's first mixer.



Various versions are available to cover the range 410 to 510 MHz, with 3 dB bandwidths of between 8 and 12 MHz as standard. Narrower bandwidth types are available to special order. All operate from 5-15 V DC. The preamp is supplied as a bare board, since its small size is capable of being accommodated in almost any available space — including antenna balun casings, or even being wrapped 'in line'.

Ambit,
299, North Service Road,
Brentwood,
Essex CM14 4SG.

(2290 M)

EPS print service

Many Elektor circuits are accompanied by printed circuit designs. Some of these designs, but not all, are also available as ready-etched and pre-drilled boards, which can be ordered from any of our offices. A complete list of the available boards is published under the heading 'EPS print service' in every issue. Delivery time is approximately three weeks.

It should be noted however that only boards which have at some time been published in the EPS list are available; the fact that a design for a board is published in a particular article does not necessarily imply that it can be supplied by Elektor.

Technical queries

Please enclose a stamped, self-addressed envelope; readers outside UK please enclose an IRC instead of stamps.

Letters should be addressed to the department concerned – TQE (Technical Queries). Although we feel that this is an essential service to readers, we regret that certain restrictions are necessary:

1. Questions that are not related to articles published in Elektor cannot be answered.
2. Questions concerning the connection of Elektor designs to other units (e.g. existing equipment) cannot normally be answered, owing to a lack of practical experience with those other units. An answer can only be based on a comparison of our design specifications with those of the other equipment.
3. Questions about suppliers for components are usually answered on the basis of advertisements, and readers can usually check these themselves.
4. As far as possible, answers will be on standard reply forms.

We trust that our readers will understand the reasons for these restrictions. On the one hand we feel that all technical queries should be answered as quickly and completely as possible; on the other hand this must not lead to overloading of our technical staff as this could lead to blown fuses and reduced quality in future issues.

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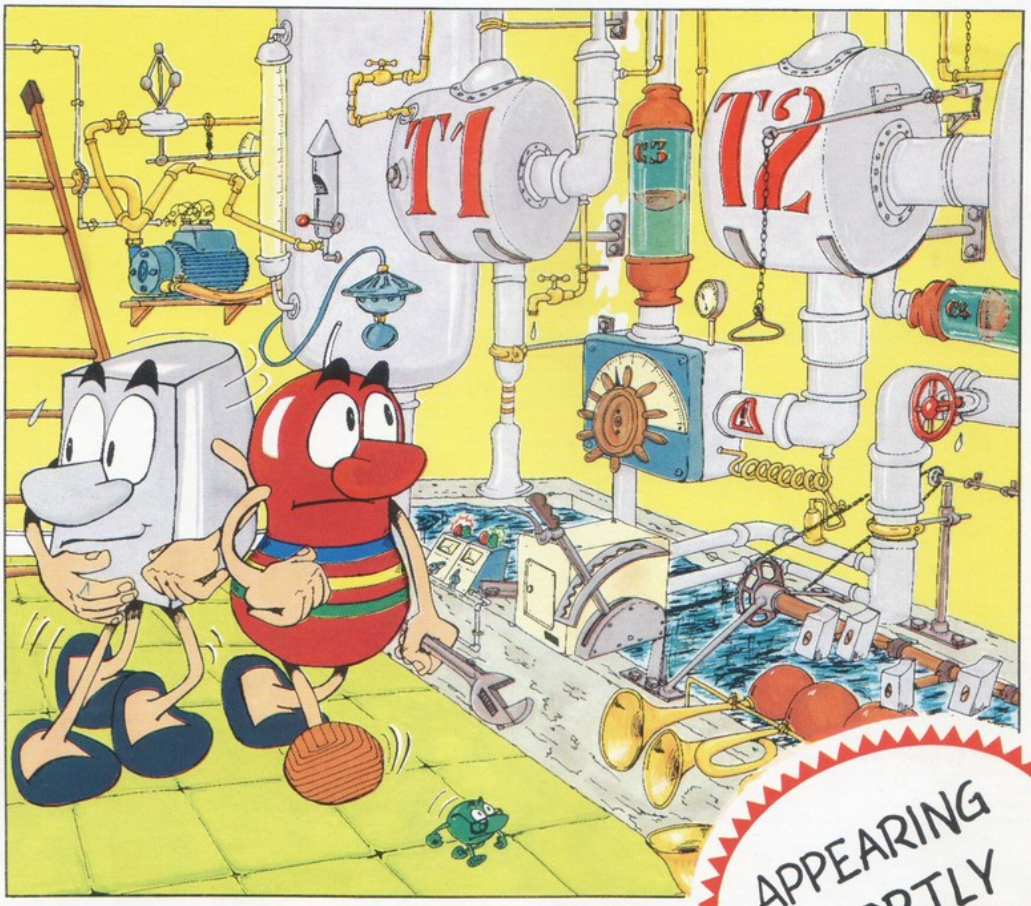

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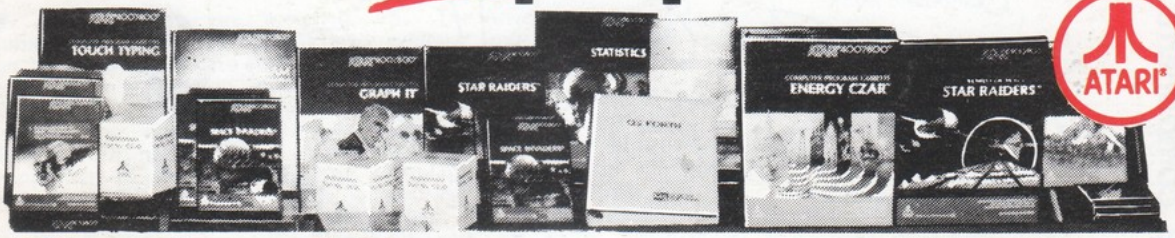
MAPLIN the people for Atari



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