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# ELEKTOR II

*Summe Zeit!*

## SSB receiver

a simple, low-cost design

## super PLAM

AM receiver with PLL

## DNL

tape noise reduction system



March 1976 40p

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SSB (single sideband) modulation is used almost exclusively as the modulation method in the 20, 40 and 80 metre amateur bands, and because of this it is possible to construct a simple amateur receiver using a single demodulator (for SSB signals). With this small compromise it is possible to produce a simple but effective design for the reception of SSB signals in the above-mentioned bands, using only two coils. This receiver has, among its other desirable properties, a sensitivity of 0.5 $\mu$ V.	
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The cover illustration is an artist's impression of coils that were etched on the printed circuit board of a VHF-FM receiver. Regrettably, production tolerances of the printed circuit board manufacturing process have proved so large that the project has had to be abandoned.





# ELEKTOR BACK ISSUES ARE STILL AVAILABLE

This is a selection from the contents of the various issues:

## number 1:

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- quadro systems
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# SUPER- PLAN

The applications and advantages of phase locked loop (PLL) systems have already been discussed in Elektor (Elektor, April 1975). In this article a practical design is discussed for a superhet receiver featuring a Phase Locked demodulator for AM signals, hence the name. The receiver is versatile in that it allows the user to choose between a wide or narrow i.f. pass band, and also between a conventional envelope detector or a novel synchronous detector using a PLL.

## Design Problems

The main problem to be overcome when designing a Medium Wave receiver is that of waveband congestion. A disregard for frequency allocations, and the enormous transmitter powers used by some stations, have resulted in the clutter that is apparent on the medium wave band today. Even high quality sets suffer from heterodyne whistles, buzzes, 'chatter' and other interference.

As the situation is unlikely to be resolved except by international agreement on the proper use of the medium wave band (such as changing to SSB) the designer of a medium wave radio must usually accept a compromise between sensitivity, selectivity and i.f. bandwidth.

It was decided, in the present design, not to accept this sort of compromise, but instead to provide two completely separate i.f. strips. A wideband i.f. strip is used to obtain the maximum possible audio bandwidth under favourable reception conditions, while under poor conditions the receiver can be switched to a narrow band i.f. to minimise adjacent channel interference. The receiver also features two different types of demodulator, a conventional envelope detector and a PLL synchronous detector.

When designing the receiver it was taken

into consideration that the home constructor would not have sophisticated test gear at his disposal, so the design must be problem free, and setting up as simple as possible.

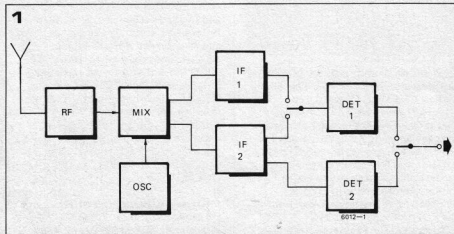
## The Circuit

Figure 1 shows the block diagram of the receiver, which more or less follows the conventional superhet pattern. The circuitry within the blocks, however, is somewhat unconventional.

The input signal first passes through a tuned r.f. amplification stage. It is then mixed with the output of the local oscillator to produce the intermediate frequency of 455 kHz. This i.f. signal passes through the wide and narrow band i.f. amplifiers. The envelope detector is connected permanently to the output of the narrowband i.f. but the synchronous detector may be switched between the two i.f. strips.

For the mixer a symmetrical mixer IC, the Siemens SO42P, was used. The internal circuit of this IC is given in figure 2, and the principal specifications in Table 1. The input local oscillator and mixer stages of the receiver are shown in figure 3a. A FET is used for the tuned r.f. input stage for low noise, and a FET is also used in the local oscillator, for stability. Both the input and output of the r.f. input stage are tuned, which improves the selectivity of the front end.

A secondary winding on L2 feeds a balanced signal into the mixer at pins 11 and 13, while the local oscillator is fed into pin 7. Although the E300 is specified for T1 and T2 other types of N channel junction FET may prove suitable in these positions. When using other types, however, it is essential to verify that the local oscillator will function reliably over the entire medium wave band (i.e. with C1 varied from minimum to maximum). If it fails to oscillate at any point (often towards the high frequency end of the band), a remedy can sometimes be found by reducing the value of R3.



Oscillator stability is ensured by taking the output signal from a low impedance point (the drain of T2) so that the oscillator cannot be affected by interaction with the mixer. This method is also less susceptible to supply voltage variations.

The two outputs of the mixer (pins 2 and 3) are fed to the two separate i.f. amplifier via an i.f. transformer L4, while the output from pin 3 is taken direct to the input of the narrowband amplifier (figure 3b) uses ceramic filters as the frequency selective elements. These were chosen because of their narrow passband, the 3 dB bandwidth of the SFD 455B type used being about 4.5 kHz. The use of three such filters in cascade gives an overall i.f. bandwidth of no more than 3 kHz. The disadvantage of these filters is their high insertion loss, about 9 dB, and the i.f. amplifier stages must have sufficient gain to overcome this. Furthermore, they are easily damped by capacitive loading, so great care must be taken in the p.c. board design to minimise stray capacitances.

The i.f. amplifier has an automatic gain control (AGC) loop, which derives its control voltage from the output of the envelope detector (figure 3c). The output from point 6 of the i.f. amplifier is rectified by diodes D1 and D2 and the resulting negative voltage is applied to point 8 via R22, which varies the bias and alters the gain of T3 and T4. The greater the negative output voltage the more the gain is reduced, so large variations in r.f. input signal are compressed. C21 and R22/R23 provide a control time constant so that the AGC does not follow the modulation of the r.f. signal but only responds to the average level. The AGC circuit is so designed that for r.f. input levels of greater than  $1 \mu\text{V}$  the average a.f. output level varies very little.

The output of the envelope detector is filtered by R24 and C24 to remove the r.f. component, and the a.f. output is taken out via C25.

## Tuning Meter

The narrowband i.f. amplifier is equipped with a tuning meter connected

in a somewhat unusual manner. A moving coil meter is connected between the emitters of T4 and T5. Under quiescent conditions these transistors have approximately the same D.C. operating point, so the voltage on the emitters is the same, and the voltage across the meter is zero. When the input signal increases the AGC alters the biasing of T4, so its emitter voltage falls and the meter reads the voltage difference between the emitter of T4 and that of T5. P1 is used to zero the meter with no input signal by altering the portion of the T5 emitter voltage which is tapped off, while P2 alters the sensitivity and can therefore be used to set the full scale deflection of the meter to a useful value.

## Wideband i.f.

The wideband i.f. amplifier relies on RC filtering for its selectivity, and as a

result the passband is much wider than that of the narrowband i.f. amplifier, in fact about 12 kHz. Both the wideband and narrowband amplifiers are in circuit all the time, and the AGC control voltage derived from the narrowband amplifier is also applied to point E of the wideband amplifier. The overall gain of the wideband amplifier is lower than that of the narrowband amplifier, since it is intended for use with stronger signals under good reception conditions. Even under ideal reception conditions there would be little point in having the high gain of the narrowband amplifier, as a  $1 \mu\text{V}$  signal amplified with a 12 kHz bandwidth would be too noisy to be usable.

## Selection of passband

As mentioned earlier the envelope detector is permanently connected to the output of the narrowband i.f. ampli-

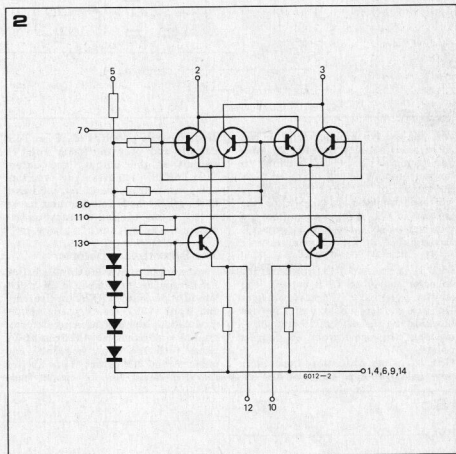


Figure 1. Block diagram of the Super PLAM showing the two i.f. strips and detectors and the switching between them.

Figure 2. Internal circuit of the Siemens SO42P symmetrical mixer.

Table 1. Main specifications of the SO42P.

Table 2. Pinout and specification of the SFD455B ceramic filter.

Table 1

### SO42P Symmetrical Mixer: Electrical Characteristics

$V_{CC} = 10 \text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$ . All parameters typical value.

Total current consumption:	1.9 mA
( $I = I_2 + I_3 + I_5$ )	
Output current ( $I_2 = I_3$ ):	500 $\mu\text{A}$
Input current ( $I_5$ ):	900 $\mu\text{A}$
Breakdown voltage:	25 V
( $I_{11}, I_{12} = 10 \mu\text{A}$ )	
Output capacitance:	6 pF
Conversion transconductance:	5 mS
Noise figure:	7 dB
( $f = 100 \text{ MHz}$ , $R_G = 240 \Omega$ )	

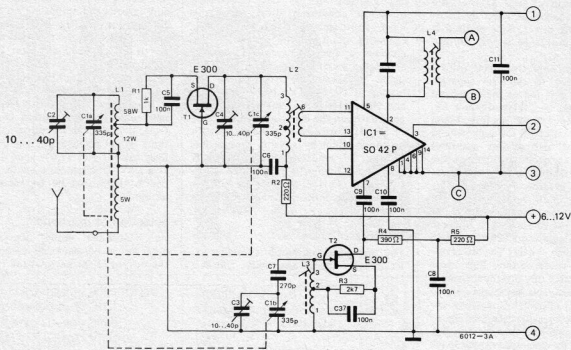
Table 11

### SFD-455B Ceramic Filter

Pin	Function
1 and 2	Coupled by external capacitor
3	Input
4	Output
5	Common

Centre frequency:	455 kHz ( $\pm 2 \text{ kHz}$ )
3 dB bandwidth:	4.5 kHz ( $\pm 1 \text{ kHz}$ )
Out of band rejection:	26 dB min at $-10 \text{ kHz}$ 20 dB min at $+10 \text{ kHz}$
In-band ripple:	1.5 dB max.
Input and output impedance:	3 k
Insertion Loss:	9 dB max.

3a



fier, but the synchronous detector can be switched between the two. The output from the narrowband amplifier to the synchronous detector is taken from the emitter of T6, while that from the wideband amplifier is taken from the emitter of T9. The two emitters are joined at point D, and the changeover is accomplished in the following manner by S1:

with S1 in position Y (narrowband) the collector supply to T9 is cut off. The emitter potential of T6 reverse biases the base-emitter junction of T9, thus blocking the signal from T9 and allowing only the signal from T6 to pass point L.

With S1 in the Z position, the emitter potential of T9 (and hence of T6) ex-

ceeds the base potential of T6, so T6 is cut off and only the signal from T9 appears at the output. The output filter L6/C36 removes any spurious components from the i.f. output signal, as the synchronous detector must have a 'clean' signal to give a distortion-free output.

### The Synchronous Detector

The principle of synchronous detection has already been described in the article 'Modulation Systems' (Elektor February and April 1975). Basically, for AM demodulation, the synchronous detector multiplies together the AM signal and a signal with the same frequency and phase as the AM carrier (remembering that the carrier has, of course, been

converted to the intermediate frequency of the receiver). This signal is derived from the carrier of the AM signal by locking onto the carrier frequency with a PLL. The synchronous demodulator can also be used to detect vestigial carrier SSB signals, where the carrier is not completely suppressed but merely reduced to increase transmitter efficiency and save energy.

Two versions of the synchronous demodulator are in fact described. The 'A' version, for the perfectionist, is capable of locking to a vestigial carrier SSB signal with only a 30% carrier component as well as normal AM signals. The 'B' version is simpler to set up, but will tend to lock onto the strongest component of the signal, and is thus

3c

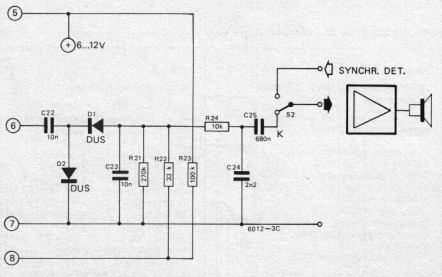
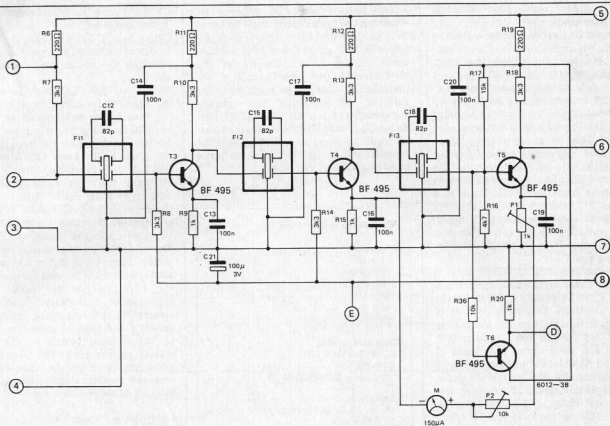


Figure 3a. Input, oscillator and mixer stages of the Super PLAM. b. The narrowband i.f. amplifier. c. The envelope detector, with AGC output (8) to the i.f. amplifiers.

Figure 4. The wideband i.f. amplifier.

3b



## Parts list to figures 3, 4 and 8.

## Capacitors:

C1 = tuning capacitor 3 x 335 p'  
(Toko 3 A-25 M)  
C2, C3, C4 = trimmer 10 . . . 40 p  
C5, C6, C8 . . . C11, C13, C14, C16, C17,  
C19, C20, C26, C27, C28, C30, C31,  
C33, C37 = 100 n  
C7 = 270 p (zero temperature  
coefficient)  
C12, C15, C18 = 82 p  
C21 = 100 µ/3 V  
C22, C23 = 10 n  
C24 = 2n2  
C25, C34 = 680 n  
C29, C32 = 470 p  
C35 = 10 p  
C36 = 330 p

## Semiconductors:

T1, T2 = E 300  
T3 . . . T9 = BF 495  
D1, D2 = DUS  
IC1 = SO42P

## Resistors:

R1, R9, R15, R20, R26, R30 = 1 k  
R2, R5, R6, R11, R12, R19, R28, R32,  
R33 = 220 Ω  
R3 = 2k7  
R4 = 390 Ω  
R7, R8, R10, R13, R14, R18, R25, R27,  
R29, R31 = 3k3  
R16, R35 = 4k7  
R17 = 15 k  
R21 = 270 k  
R22 = 33 k  
R23 = 100 k  
R24, R36 = 10 k  
R34 = 8k2

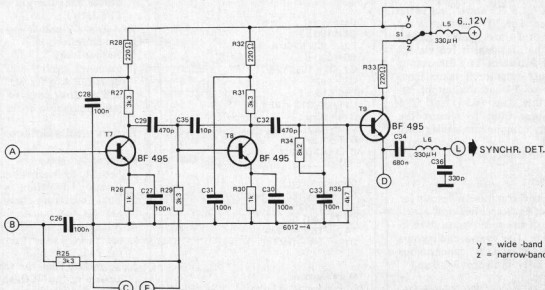
## Coils, inductors:

L1 = 70 turns 0.3 mm wire (31 SWG) on  
ferrite rod (length 20 cm, dia  
10 mm), tapped at 12 turns from  
gnd; external aerial coupling: 5 turns.  
L2 = Toko RW 06A 6693R  
L3 = Toko YXRS 17065  
L4 = IF transformer (Toko YME 18103  
PDR)  
FL1 . . . FL3 = SFD 455B (Murata)  
L5, L6 = 330 µH inductor

## Miscellaneous:

M = 150 µA moving coil instrument  
S1, S2 = SPDT switch

4



y = wide band  
z = narrow band



really suitable only for broadcast AM transmissions.

The circuit of the 'A' version is given in figure 5. It consists of a PLL (comprising Voltage Controlled Oscillator, phase comparator, and low-pass filter), a product detector (multiplier), and low-pass filter to remove the high-frequency components from the product detector output, leaving only the a.f. output.

IC1 functions as an amplifying phase comparator. The input signal from the i.f. amplifier is fed into pin 9. The limiter/amplifier input (pin 14) receives the output from the VCO. Since in a PLL the VCO output at lock has a 90° phase shift with the incoming signal, this is corrected by R2 and C6 so that the VCO output is in phase with the incoming signal.

The limiter/amplifier of IC2 is used as the VCO, tuned by a 455 kHz i.f. transformer L1. The tuning is varied by the varicap diode D1 under the control of the output voltage from the phase comparator, fed via the low-pass filter (C8, C9, R3 and the output impedance of IC1). The VCO locks onto the carrier of the incoming i.f. signal to provide a constant amplitude signal of the same frequency and phase. The phase comparator of IC2 is used as the product detector, and multiplies together the output of the VCO and the incoming i.f. signal. The resultant output from pin 8 of IC2 is filtered by the output impedance of IC2 and C16 to remove the high-frequency components, leaving only the a.f. signal.

The 'B' version of figure 6 may be regarded as a simplified version of the 'A' circuit. IC1 is again used as an amplifying phase comparator. The VCO and product detector, however, are constructed from discrete components. The VCO comprises T1, T2 and T3, while the product detector consists of T4, T5 and T6. In this circuit the i.f. output is fed into the limiter/amplifier input (pin 14), while the VCO output is fed into pin 7 of IC1. The output from pin 8 of the phase comparator is used to control the VCO frequency by altering the biasing of T1. The output impedance of IC1, C8, R5 and C7 act as the low-pass filter. The VCO output is fed to the bases of T4 and T5 via C12 and C11, while the i.f. signal is fed via R7 and C13 to the base of T6. The output of the product detector is taken from the collector of T4 and the output impedance of this stage (R14) and C16 form a low-pass filter to remove the high-frequency components leaving only the a.f. signal.

## Construction

A p.c. board and component layout for the front-end, i.f. amplifiers and envelope detector of the receiver are given in figures 8 and 9. The boards and layouts for the type 'A' and 'B' synchronous detectors are given in figures 9, 10 and 11, 12 respectively.

It should be stressed that for stable, reliable operation of the receiver these

board layouts must be adhered to. Furthermore, great care should be taken over the construction. This is good advice for any project, but it is particularly relevant to r.f. circuits, as the sophisticated test gear necessary for fault-finding may not be available to the amateur. In particular high quality components (especially capacitors) must be used, component lead lengths must be kept as short as possible, and, of course, care should be taken to make good joints when soldering.

### Parts list to figures 5 and 10.

Resistors:  
R1 = 10 k  
R2 = 2k2  
R3 = 47 Ω  
R4 = 1k5  
R5 = 4k7  
R6 = 100 k

Semiconductors:  
IC1, IC2 = TBA 120  
D1 = BB 109  
D2 = zener 4V7/250 mW

Capacitors:  
C1 ... C5, C7, C10, C11, C12, C15 = 100 n  
C6, C16 = 4n7  
C8, C9, C17 = 47 μ/12 V  
C13 = 82 p  
C14 = 10 p  
C18 = 47 μ/12 V

Miscellaneous:  
L1 = I.F. transformer (Toko YME 18103 PDR)  
L2 = inductor 330 μH

### Parts list to figures 6 and 12.

Resistors:  
R1, R3, R4, R9, R10 = 1 k  
R2, R5, R6, R8 = 100 Ω  
R7 = 4k7  
R11 ... R14, R17, R18 = 10 k  
R15 = 2k2  
R16 = 680 Ω  
R19 = 100 k  
P1 = preset 4k7

Capacitors:  
C1 = 180 p  
C2 ... C5 = 100 n  
C6 = 330 p  
C7, C9 = 10 μ/12 V  
C8 = 1n2  
C10, C16 = 1 n  
C11, C12, C13 = 10 n  
C14 = 82 p  
C15 = 4μ7/3 V  
C17 = 1 μ/12 V  
C18 = 47 μ/12 V

Semiconductors:  
IC1 = TBA 120  
T1 = BC 147 B  
T2, T3 = BF 199  
T4 ... T6 = BF 254  
D1 ... D4 = 1N4148

Miscellaneous:  
L1 = inductor 330 μH

C1 is a 3 gang, 335 pF tuning capacitor, Toko type 3 A-25 M.

Other 3 gang 335 pF types that do not fit direct on the board may also be used, provided the connecting wires are kept short.

The ferrite rod (L1) must be mounted as close as possible to the receiver p.c. board. The dimensions of the rod are 200 mm long by 10 mm dia. L2 and L3 are Toko types; the type numbers are given in the parts list. Almost any 455 kHz i.f. transformer would do for L4, and the type actually used was Toko type YME 18103 PDR.

Once the individual boards have been constructed the main receiver board can be wired up to the chosen synchronous demodulator in accordance with the wiring diagram of figure 13. Screened audio cable must be used for connecting the i.f. output to the input of the synchronous demodulator, and also for connecting the outputs of the envelope detector and synchronous demodulator to the selector switch S2. To ensure stable performance the synchronous demodulator must be housed in a screened enclosure such as a small aluminium or diecast box.

## Setting-up Procedure

It need hardly be stressed that for optimum performance the Super PLAM must be correctly set up, in accordance with the following procedure.

1. Set S1 to 'narrowband' and S2 to 'envelope detector'.
2. Connect an aerial wire via a 100 p capacitor to the live end of the aerial coupling winding of L1 (earthly end is grounded).
3. With C1 set to maximum capacitance (vanes closed) adjust the core of L3 to tune in a transmitter at the low end of the MW band (550 kHz).
4. Adjust the core of L2 to give maximum deflection on the tuning meter.
5. Remove the aerial wire and slide L1 along the ferrite rod to give the strongest signal.
6. With C1 set to minimum (vanes open) adjust C3 to tune in a transmitter near the top end of the band (1.6 MHz).
7. Adjust C2 and C4 to give maximum meter deflection.
8. Repeat steps 3, 4, 5, 6 and 7 at frequencies around 600 and 1500 kHz until the receiver will tune at the top and bottom ends of the band with good deflection of the meter.

## Synchronous Detector

### Setting up 'A' version

1. Set S1 to 'narrowband' and S2 to 'envelope detection'.
2. Tune to a strong transmitter.
3. Set S2 to 'synchronous detection'.
4. Adjust core of VCO coil (L1 in figure 5) until a beat note is heard and the PLL locks in.
5. To ensure that the free-running frequency of the VCO is the same as the i.f. carrier frequency, proceed as

Figure 5. 'A' version of the synchronous detector.

Figure 6. 'B' version of the synchronous detector.

follows: momentarily short the input of the demodulator to ground, then release it. Repeat this step, adjusting the core of L1 until, when the short is removed, the PLL will lock in without the beat note becoming audible.

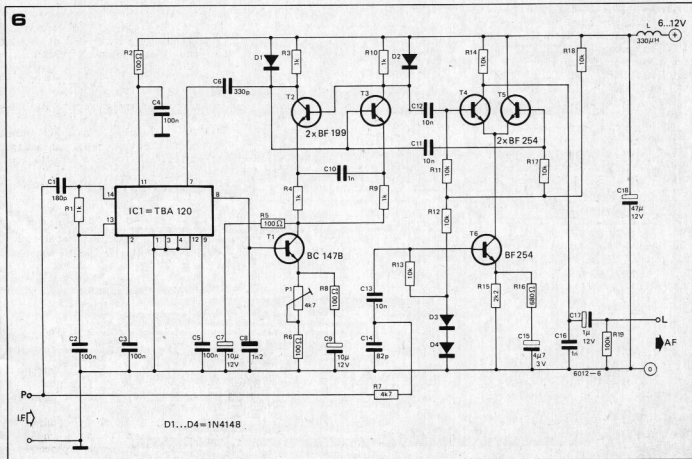
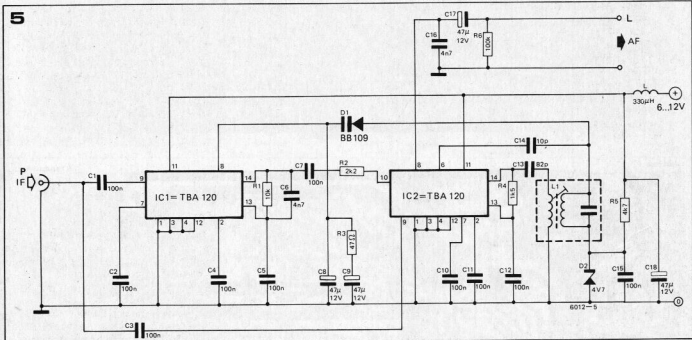
#### Setting up 'B' version

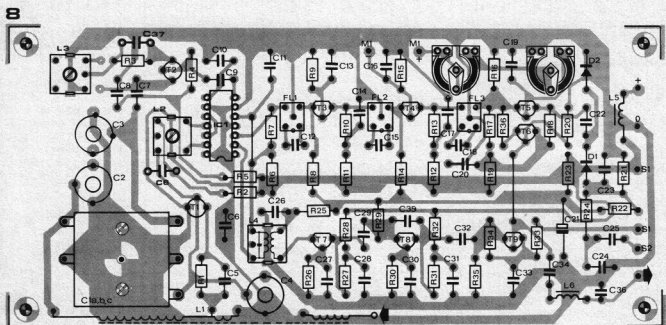
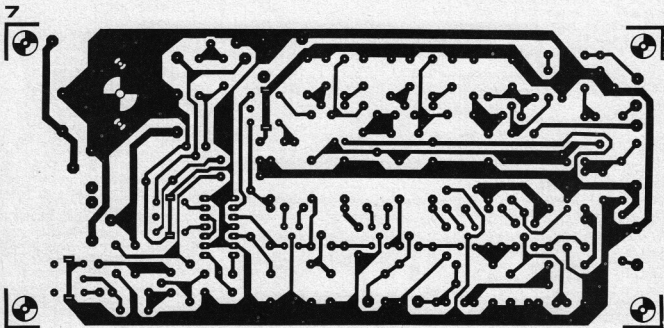
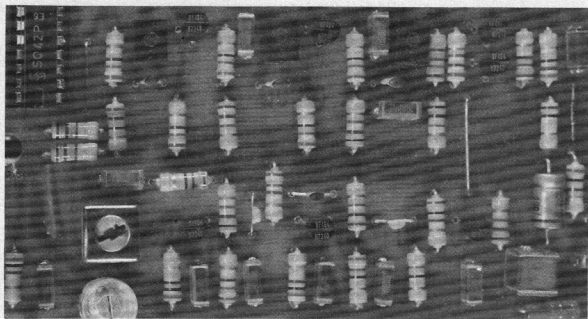
Steps 1, 2 and 3 are identical to those for the 'A' version.

4. Adjust P1 until the PLL locks in and the audio signal is heard.

#### Conclusion

Using the 'B' version of the synchronous detector the performance was already greatly superior to a conventional superhet, but with the 'A' version the performance was surprising. The noise figure was remarkably low and the sensitivity high, and when switched to 'narrowband' the selectivity was unprecedented. Provided the construction is carried out carefully and the setting-up procedures are followed, the Super PLAM should give reliable operation and high performance.





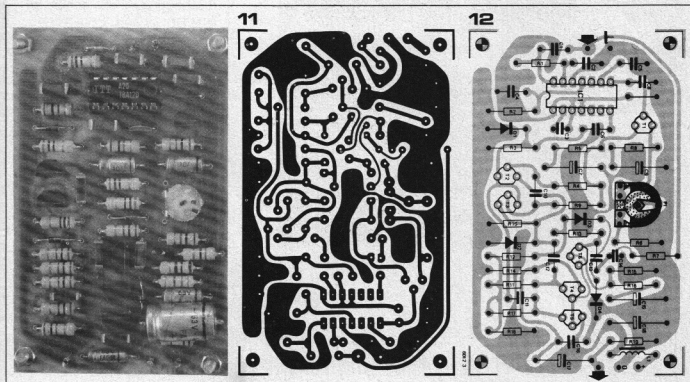
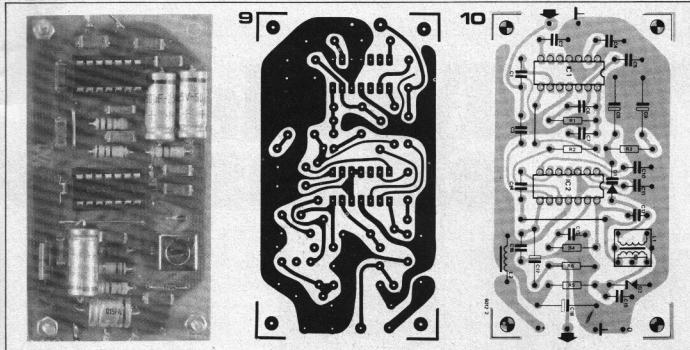


Figure 7. P.c. board for the front end, i.f. strips and envelope detector (EPS 6012-1B).

Figure 8. Component layout for figure 7.

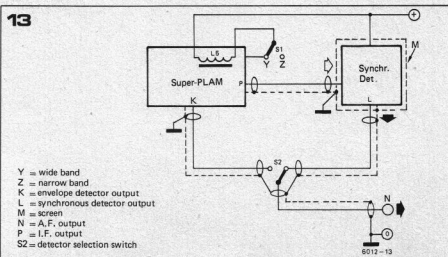
Figure 9. P.c. board for the 'A' version of the synchronous detector (EPS 6012-2A).

Figure 10. Component layout for figure 9.

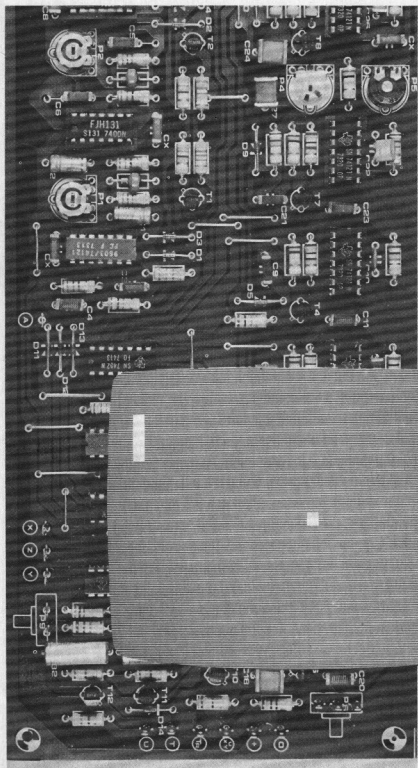
Figure 11. P.c. board for 'B' version of the synchronous detector (EPS 6012-3A).

Figure 12. Component layout for figure 11.

Figure 13. Wiring diagram showing interconnection of the main board and synchronous detector.



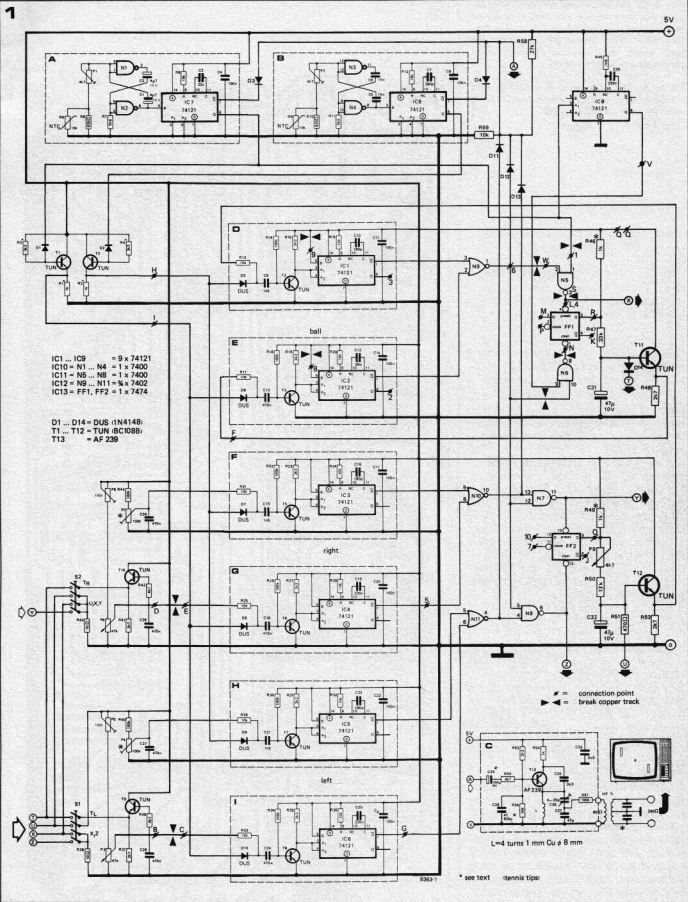
# TV Tennis extensions



The scope of the TV tennis game (Elektor 7) can be considerably extended. In its basic form the circuit provides only the tennis game, with a display consisting simply of bats and ball, with no boundaries or other refinements. By the addition of a number of auxiliary circuits, a number of different games can be played, and boundaries, automatic scoring and other effects can be added.

## part 1

The extensions to the TV tennis game are connected into various points on the existing board. In some cases additional holes must be drilled for connection pins, and in others the track on the existing board must be broken for connection of the auxiliary circuit. Fig-



**Figure 1.** The original circuit of the TV tennis game. The new connection points and the places where connections will have to be broken are shown.

ure 1 gives details of these modifications to the existing board. To simplify the procedure a new board layout has been designed (figure 2), but for those who possess the old-style board the modifications are still quite straightforward. In the course of the article it will be

made clear which connection points are used for the various extensions to the game.

### Automatic opponent

TV tennis, like many other pastimes, is a game that only two can play. How-

Figure 2. The p.c. board for the TV tennis game has been slightly modified to allow for the extensions described in this article. The wire links shown dotted are needed for the basic game, but must be removed when certain extensions are added.

Figure 3. The automatic opponent is very simple to add: two single-pole double throw switches are all that is required.

ever, for solo practice it is a relatively simple matter to provide an automatic opponent, who never gets tired and who never misses a shot. This is accomplished by making the vertical position of the automatic opponent's bat always coincide with the position of the ball. Vertical control of the bat must therefore be disconnected from the player controls (P3 or P6) and must be connected to the vertical ball position control. To do this the connections to the sliders of P3 and P6 from R33 and R25 must be broken, giving 4 new connection points:

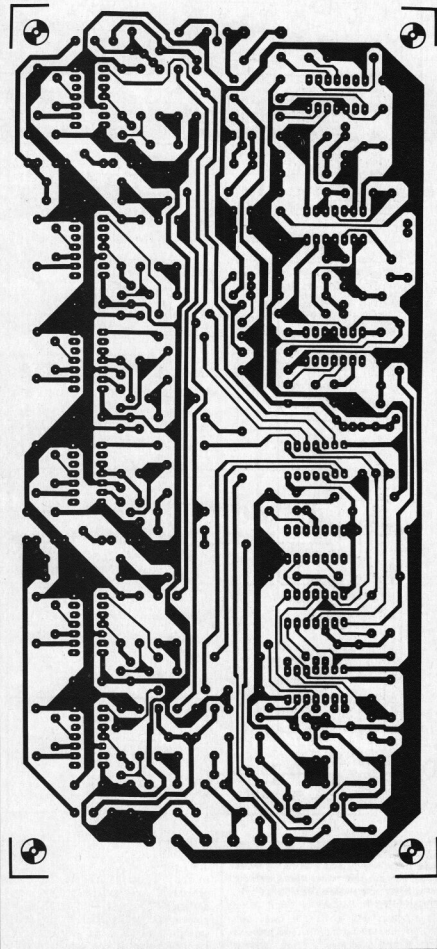
- B : slider P3/C26/R39
- C : left-hand side R33
- D : slider P6/C28/R43
- E : left-hand end R25

A new connection is also made to the emitter of T11 (F). An auto/manual switch is connected to these points so that point C may be switched between points B and F, and similarly a switch is introduced between points E, D and F (figure 3).

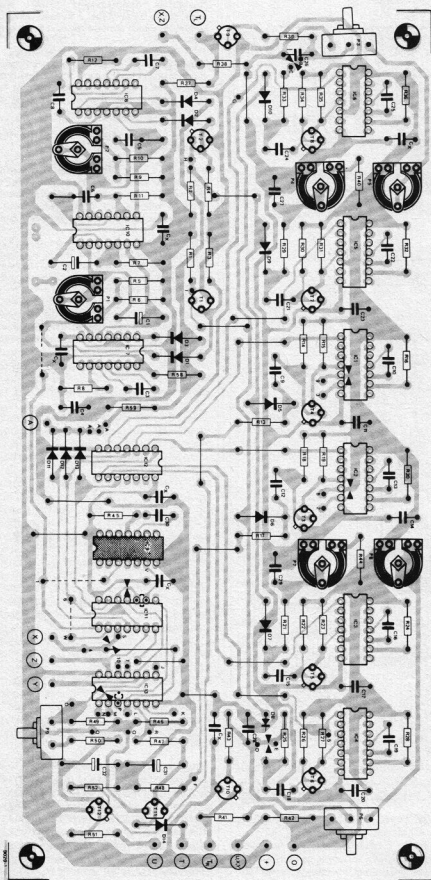
### Vertical Centre Line

It is usual with most ball games to have the field of play divided into two halves. A vertical centre line will serve as the net for TV tennis, or as the centre line for a football game, which will be described later. A white centre line is easily achieved by producing a peak white video pulse halfway along each line sweep. The circuit that performs this function consists of a delay circuit triggered from the line sync pulses, and a monostable to produce the pulse (figure 4). This is almost identical to the circuits used in the original design for the generation of the bats and ball. The circuit is triggered from point H (emitter of T2), and the output is taken to the video mixer (point A). The horizon-

2



2



3



9363.3

tal position of the line may be adjusted by varying the delay with P10.

### Vertical boundaries

In the basic version of the TV tennis game the vertical boundaries at the top and bottom of the picture, from which the ball rebounds, are invisible. Since one of the boundaries is derived from the field sync pulses and occurs during the field blanking interval, the ball may disappear from the screen for short periods. It is much more pleasing if the ball can be seen to rebound from a visible (white) barrier.

To give horizontal white boundaries at the top and bottom of the picture it is necessary to produce a peak white video signal that lasts for several line periods, and overlaps the start and finish of the field sync pulse. The portion of the video pulse before the field sync pulse produces the lower boundary, and the portion after produces the upper boundary. This is shown in the timing diagram of figure 5. The video pulse is again produced by a delay circuit and monostable (figure 6), but here the delay is triggered from the leading edge of the field sync pulse. This entails connecting the input of figure 6 to point I (emitter T1). The output again goes to the video mixer.

P11 adjusts the delay, and therefore the position of the boundaries, while P12 adjusts the duration of the video pulse, and hence the width of the boundaries.

As the ball must now rebound from these new boundaries, the connections to FF1, which determines vertical ball direction in the original circuit, must be somewhat modified. The new connections are shown enclosed in the dotted box in figure 6. Instead of functioning as a set-reset flip-flop, FF1 is now connected in the divide-by-two mode, so every time a pulse reaches its clock input it changes state. The pulses to trigger the flip-flop are obtained from the output of N6, N5 and N6 being connected to form an AND gate. When the vertical ball signal (Q output of IC2 connected to point W) and the Q output of IC15 are both '1' this indicates a coincidence between the ball and the upper or lower boundary, so the output of N6 will become '1' and FF1 will change state, reversing the vertical ball direction.



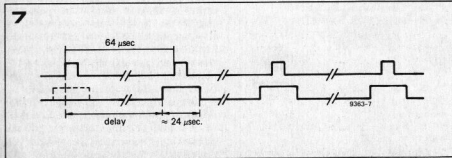
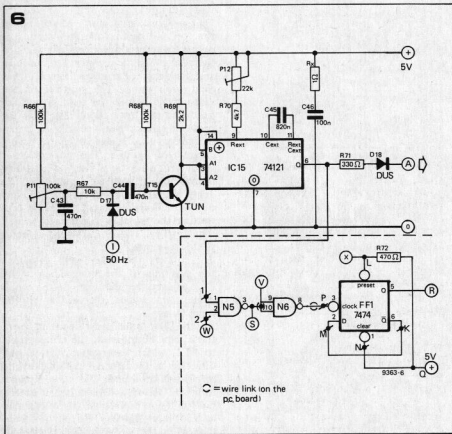
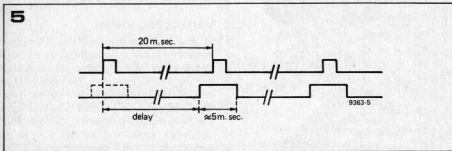
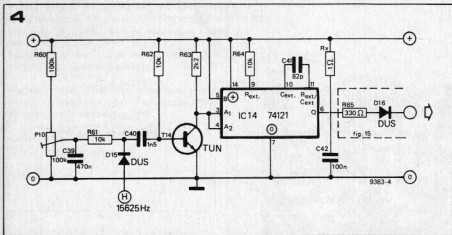


Figure 4. The centre line. As in the rest of the circuit, a combination of pulse delay and monostable multivibrator is used for this.

Figure 5. Pulse diagram of the horizontal boundaries. Approximately 18 msec after each frame sync pulse a 5 msec pulse is produced, which overlaps the next frame sync pulse.

Figure 6. Circuit for producing the horizontal boundaries. This extension entails modifying part of the original circuit, as shown in the lower half of the diagram. IC9 must be removed from the original board.

Figure 7. Pulse diagram for the vertical boundaries.

Figure 8. Circuit for producing the vertical boundaries. In this case, no modifications to the original circuit are required. The extra flip-flop will be used in conjunction with a sound effects generator to be described later.

Figure 9. This circuit can be used for deriving the frame sync pulses from the 50 Hz mains, as described in the original article. The frame sync oscillator on the main p.c. board must be removed if this circuit is used.

Figure 10. The new p.c.b. for the TV tennis game has been modified so that the circuit shown in figure 9 can be mounted on it without any problems, as shown here.

The preset input of FF1 is still connected to point X of the original circuit, but is no longer connected to the output of N5. Instead, a 470 Ω pullup resistor is connected from this point to the positive supply. The connections to the Q output of FF1 (R46/R47) remain unchanged.

To recap, the modifications to this part of the circuit are as follows:

1. tracks connected to the inputs and outputs of N5 and N6 are broken.
2. Pin 2 (point W) of N5 is connected to pin 6 (point 2) of IC2. Pin 1 (point 1) of N5 is connected to pin 6

of IC15 (on new ancillary board). Pin 3 (point S) of N5 is connected to pins 9 and 10 (point V) of N6.

3. Pin 8 of N6 is connected to pin 3 (point P) of FF1. Pins 2 and 6 (M and K) of FF1 are linked, and pins 1 and 4 (N and L) of FF1 are linked by the 470  $\Omega$  resistor. Pin 1 is also connected to +5 V by joining it to pin 14.

4. IC9 is now redundant and may be removed from the board.

These modifications may be carried out by means of wire links on the back of the board.

### Left and Right Hand boundaries

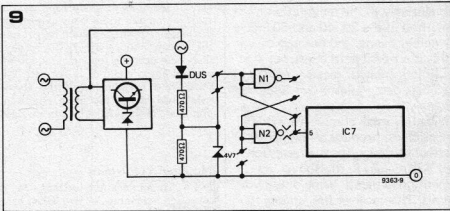
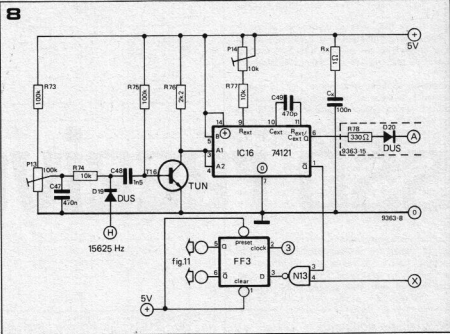
A further logical extension to the TV tennis game is the addition of vertical white bars as boundaries at the left and right-hand extremes of the 'court'. If automatic scoring is to be incorporated these are essential. When the ball crosses one of these boundaries this indicates that a point has been scored, and the signal required to trigger a points counter can easily be derived.

The circuit (figure 8) is almost identical to that which produces the upper and lower boundaries, but it is triggered from the line sync oscillator and produces a video pulse that overlaps the line sync pulse, thus giving a white bar at the left- and right-hand edges of the picture.

The video pulse width is about 24  $\mu$ sec. and the timing diagram for this circuit is given in figure 7. P14 adjusts the pulse width, and hence the width of the vertical bars, while P13 adjusts the delay time, and hence the position of the boundaries. FF3 is used to control the sound effects unit which will be described later. Pin 2 (point 3) of FF3 is connected to pin 6 of IC1, which generates the horizontal ball signal. Within the boundaries of the court the Q output of IC16 is high, and point X is normally high, so the output of N13 holds the D input of FF3 low, and the ball signal cannot trigger it. If, however, the ball crosses the left- or right-hand boundary then the Q output of IC16 will be low, so the D input of FF3 will be high and the flip-flop can be triggered by the horizontal ball signal applied to the clock input (point 3). This means that the sound unit is activated only when the ball crosses the left- or right-hand boundary.

### TV tennis hints

As a conclusion to the first part of this article, a few tips will now be given on minor improvements to the original TV tennis circuit in the light of operational experience with the game. It should be stressed that these are simply minor improvements, not major design changes. The existing circuit will work satisfactorily in its original form, so these modifications should not be expected to produce a cure for units that do not function. The faults here often lie in dry joints, incorrect wiring or defective components.

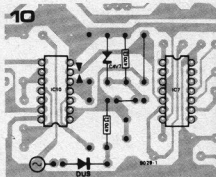


The first improvement is to increase the output capability of the emitter follower buffers T1 and T2. This will prevent them from being overloaded and will give the increased output capability essential to cope with the additional load imposed by the additional circuits of the extensions. R1 and R2 should be reduced to 1 k and R3 and R4 should be reduced to 3k3.

The next item to receive attention is the ball speed. With the existing circuit it is impossible to obtain exactly the same ball speed in both directions. This is not so important in the vertical direction, but different ball speeds in the horizontal direction give one player an unfair advantage. Adjustment to equalize ball speeds in the left-right, right-left, and up-down, down-up directions may be provided by a 4k7 preset in series with R46, and a similar one in series with R49.

In the original modulator circuit capacitor C34, together with the input impedance of the modulator forms a differentiating network that can distort the video signals and hence degrade the picture. Increasing C34 to 100  $\mu$ /10 V will improve this. Picture definition may be improved by reducing C38 to 47 p, which raises the maximum achievable modulation frequency.

Replacement of the field sync oscillator



by a mains driven sync circuit was described in the original article. This modification is strongly recommended whenever mains operation of the unit is intended, as it eliminates distortion caused by the field sync pulses not being locked to the mains frequency. The mains driven sync circuit is given in figure 9, and the modifications to the p.c. board are given in figure 10. The sync circuit is contained on the power supply board given in figures 4 and 8 of the original article.

In the second part of the article new games and the sound effects unit will be described. A p.c. board layout to accommodate all the extensions will also be given.

# ssb receiver

SSB (single sideband) modulation is used almost exclusively as the modulation method in the 20, 40 and 80 metre amateur bands, and because of this it is possible to construct a simple amateur receiver using a single demodulator (for SSB signals).

With this small compromise it is possible to produce a simple but effective design for the reception of SSB signals in the above-mentioned bands, using only two coils. This receiver has, among its other desirable properties, a sensitivity of  $0.5 \mu\text{V}$ .

In the article 'Modulation Systems' (Elektor, February and April 1975), the various methods of modulation used in radio communication were extensively discussed. To obtain a good insight into the design philosophy of the receiver discussed here, a fundamental knowledge of these methods is essential. For those who have not read the above-mentioned article the more important points are recapitulated here in abridged form.

## Modulation Systems

Every communication system, be it television, telephone, or two baked bean cans and a piece of string, has the task of conveying information from one location to another, preferably in the most efficient manner possible. If electromagnetic radiation is used as the transmission medium then the information must be impressed on the electromagnetic carrier wave as a change, or sequence of changes, in one of the parameters of the carrier wave. i.e. the information must modulate the carrier at the transmitter in some way. At the receiving end the modulated carrier is demodulated to retrieve the information.

An electromagnetic wave has two parameters which can be varied, amplitude and frequency, and there are thus two categories of modulation:

### Amplitude Modulation (AM) and Frequency Modulation (FM)

Of these amplitude modulation has the most variants. These are:

- a. Double sideband with carrier (Normal AM)
- b. Double sideband suppressed carrier (DSSC)
- c. Single sideband suppressed carrier (SSB)
- d. Carrier position modulation (CPM)

There are only two types of frequency modulation, namely:

- a. Frequency Modulation (FM)
- b. Phase Modulation (PM)

## AM

Normal AM transmissions as used by long and medium wave broadcast stations are extremely inefficient and very wasteful of carrier power. The information (which for simplicity we will now call an audio signal, which it usually is) is used to alter the amplitude of the carrier in accordance with the audio signal amplitude. Thus on the peaks of the audio signal the carrier amplitude is a minimum, while in the troughs the carrier amplitude is a maximum, or vice versa. The envelope of the modulated carrier is thus the same shape as the audio signal. The depth of modulation can be expressed as a modulation index, which is:

$$m = \frac{A_0 - A_{\min}}{A_0}, \text{ where:}$$

$A_0$  = unmodulated carrier amplitude, and

$A_{\min}$  = minimum modulated carrier amplitude

It may also be expressed as a modulation percentage, which is 100 x the modulation index. Obviously, 100% modulation occurs when the carrier amplitude reaches zero on the peaks of the audio signal.

This method of modulation is very inefficient for several reasons. It can be shown mathematically (see original article) that an AM signal consists of a carrier plus two sidebands. These sidebands occupy a bandwidth equal to the bandwidth of the transmitted audio signal on each side of the carrier (upper and lower sidebands). Each of these sidebands contains the audio information, none is contained in the carrier. Furthermore, even with 100% modulation 50% of the transmitted energy resides in the carrier, and 25% in each of the sidebands. Thus even with 100% modulation 75% of the transmitter energy is wasted (since only one sideband is required to transmit all the audio information). What is more, the AM signal occupies twice the bandwidth necessary to transmit the audio information.

In practice, due to the wide dynamic range of audio signals and the high peak to mean amplitude ratio the average modulation index of broadcast transmitters rarely exceeds a few percent, so over 90% of the transmitter energy is radiated as useless carrier.

Why then is AM so widespread? There are two main reasons. The first is that AM is the oldest established system, so there is a lot of capital tied up in transmission and reception equipment. Were any other modulation method used, all existing AM receivers and much transmission equipment would be so much scrap.

The second reason lies in the simplicity of AM receivers. All that is required to detect (demodulate) an AM signal is to chop it in half, i.e. to half wave rectify the modulated carrier. The audio signal is then superimposed on the rectified r.f. signal. If this signal is then passed through a low-pass filter to remove the r.f. component then the result is an a.f. signal superimposed on a D.C. level. This can be achieved with the simple circuit of figure 1.

### SSB

A great increase in modulation efficiency can be achieved by suppressing the unwanted carrier at the transmitter. A further increase in efficiency, and also a 50% reduction in bandwidth, can be achieved by suppressing one of the sidebands, since either of the sidebands contains all the audio information and the other is clearly redundant. This is what is done in an SSB system, resulting in one of the most efficient AM modulation methods. The method is not without its drawbacks, however, which appear at the receiving end.

### SSB demodulation

As the envelope of an AM signal is the audio waveform, demodulation is a very simple process - as described earlier. However, a glance at an SSB waveform on an oscilloscope will quickly show that this is not the case with SSB, because of the missing carrier. The carrier is indispensable for the demodulation process, so some method of regenerating it in the receiver must be found.

Many commercial SSB stations, instead of suppressing the carrier completely, transmit it at a very much reduced level (vestigial carrier systems). In these cases the demodulation systems of figure 2 may be used. A phase locked loop is used to lock on to the vestigial carrier, and the VCO output of the PLL is thus the same frequency as the carrier but at a much higher level. The SSB signal and the regenerated carrier are then fed to a product detector, the SSB signal first being fed through a 90° phase shift network to compensate for the fact that the VCO output of the PLL is 90° out of phase with the vestigial carrier input.

The product detector multiplies together the two inputs, so that the output contains sum and difference

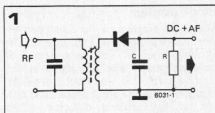


Figure 1. Simple diode envelope detector for AM signals.

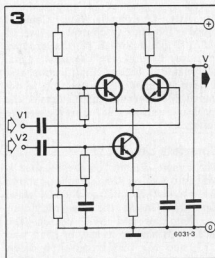
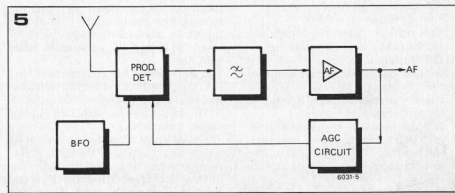
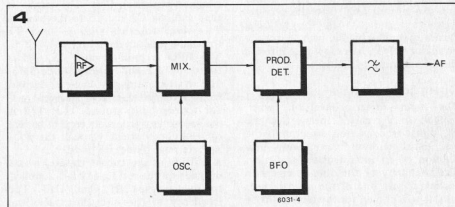
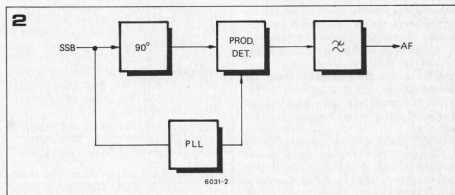


Figure 2. A vestigial carrier SSB signal may be demodulated by regenerating the carrier using a PLL and feeding the SSB signal and regenerated carrier into the product detector.

Figure 3. An asymmetric product detector. A product detector may be used to demodulate SSB signals since it multiplies two signals together. When an SSB signal is multiplied by a regenerated carrier the difference product is the original modulation signal.

Figure 4. When the carrier is completely suppressed it must be regenerated artificially using a stable oscillator in the receiver (BFO). Figure 4 shows a superhet receiver using this principle.

Figure 5. Rather than converting the r.f. input down to an intermediate frequency before demodulation, the direct conversion receiver demodulates direct from the r.f. input frequency. This gives a reduction in cost and complexity at the expense of selectivity.



components of the two sets of input frequencies. The sum components obviously occupy a band from twice the carrier frequency plus the lowest audio frequency to twice the carrier frequency plus the highest audio frequency. In the case of the difference component the regenerated carrier is subtracted from the SSB signal if the upper sideband is used, or the SSB signal is subtracted from the carrier if the lower sideband is used. In either case the resultant output is simply the original audio signal. The output of the detector is passed through a low-pass filter to remove the high-frequency components, and the audio signal appears at the output.

A symmetrical mixer such as the Siemens SO42P may be successfully used as the product detector. This has the advantage that good suppression of the original input signals (SSB and regenerated carrier) is provided by the IC, which is not the case with simpler product detectors. An asymmetric mixer such as figure 3 may also be used, and this has the advantage of providing good AM suppression.

The above is a slight digression from the original subject, since most amateur transmitters do not employ a vestigial carrier system, and carrier suppression is so effective that this reception method cannot be used. It is, of course, still possible to use the product detector for demodulation, but it must now be fed with an artificially generated carrier produced by a stable oscillator in the receiver.

Figure 4 shows a block diagram of such a receiver. The incoming signal passes through a stage of r.f. gain and is then fed, together with a local oscillator signal, into a mixer, in accordance with normal superhet practice. The i.f. output can now be fed into the product detector together with the artificial carrier generated by the beat frequency oscillator (BFO). After low-pass filtering the a.f. output is available.

### Direct conversion

The term direct conversion, when applied to a receiver, means that the r.f. signal is converted direct into the a.f. signal without mixing and production of an intermediate frequency. The simplicity of the direct conversion technique was one of the main reasons why it was chosen for the receiver to be described in this article. When drawing up the specification for the receiver the following points were considered:

1. The receiver must be suitable for mobile as well as fixed operation.
2. The performance must be at least as good as that of average commercial equipment. It should be possible at a later date further to improve the performance if required.
3. In order to appeal to a large number of constructors, including beginners, construction and operation of the receiver should be as simple as possible.
4. The cost should be fairly small.

### Block diagram

The block diagram of the direct conversion receiver is given in figure 5. The extreme simplicity of the system is at once apparent. The r.f. signal is fed straight to the product detector, together with the BFO signal. The output of the product detector is fed through a low-pass filter, which is followed by a stage of a.f. amplification. An AGC (Automatic Gain Control) signal is fed back to control the level of the r.f. input signal to the product detector. In this way the input signal is controlled before amplification and a very effective AGC function is obtained. Moreover the input stages of the receiver are safeguarded against excessive voltages.

### Complete circuit

The circuit diagram of the receiver is split into two sections. Figure 6a shows the product detector and BFO, while figure 6b shows the low-pass filter, a.f. amplifier and AGC circuit. The receiver is varicap tuned by D12 and D13, and the band received is determined by L1, L2 and resistor R33, which can be changed to alter the tuning voltage range. The values of R33 for the 20, 40 and 80 m bands are given in figure 6a. Coil winding details are given later, in the assembly instructions. With the specified coils and the appropriate value of R33 the prototype of the receiver could be tuned over the following wavebands:

- 20 m band — 14.00 to 14.35 MHz.
- 40 m band — 7.00 to 7.10 MHz.
- 80 m band — 3.50 to 3.80 MHz.

The r.f. signal arrives from the aerial, via C1, across L1A. The input is tuned by L1B, the varicap diode D12 and trimmer capacitor C30. The signal is then fed, via C2 and C3 to the base of T1, which together with T2 and T3 forms the product detector.

The BFO is built around T6, and is tuned by L2 and varicap diode D13. The varicap tuning voltage is derived from a temperature compensated voltage source built around T12. T12 is connected as a constant current source and supplies current through the voltage reference diodes D8 and D9.

A portion of the output voltage, which depends on the setting of P1, is supplied to the varicaps D12 and D13. The frequency of the BFO thus tracks the frequency to which the input circuit is tuned as P1 is varied to tune the receiver over the band. To provide fine tuning an additional potentiometer of about 10 k may be included in series with P1.

The BFO circuit has good stability and low temperature coefficient. Nevertheless, to avoid excessive variations in BFO frequency a stabilised power supply is essential.

The BFO signal is fed to the emitter of T3 via C5. Injection of the signal at this point ensures that feedback into the BFO, which might affect the BFO frequency, is extremely small. T1 and T2

Figure 6. a. The input stage, BFO and product detector of the receiver. b. The filter, a.f. stages and AGC control circuit of the receiver.

both receive their D.C. base bias via R8. The choke L3, however, prevents any r.f. signal from reaching the base of T2. The FET (T4) in the collector circuit provides a constant current load for T2, resulting in a high collector impedance and hence a high conversion gain for the product detector.

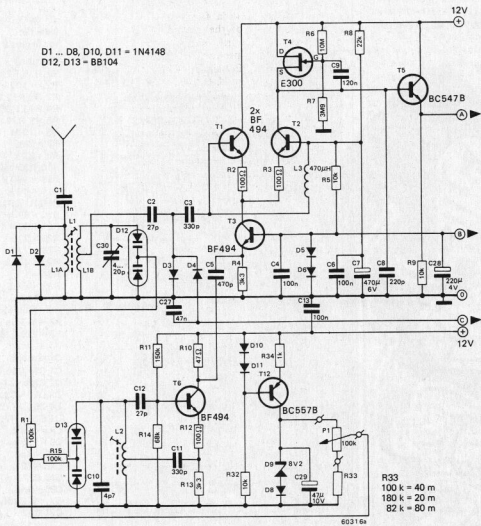
The high collector impedance of course means that the output impedance of the product detector is too high to feed direct into the low-pass filter, so emitter follower T5 is included to provide a lower output impedance. The output at point A (emitter T5) contains, in addition to the required a.f. signal, various r.f. products which must be filtered out. Furthermore, for maximum intelligibility of speech only the band 300-3000 Hz is of interest. The filter must therefore be tailored to meet these requirements.

The filtering is carried out in two stages. An active low-pass filter built around T7 removes all components of the signal above 3 kHz. T8 and T9 then provide about 60 dB of gain. However, the inclusion of C22 in the feedback loop means that the gain rolls off below about 300 Hz as the impedance of C22 increases at low frequencies. A very complicated filter was not felt to be necessary for this function, as the exclusion of frequencies below 300 Hz is less important than the exclusion of r.f. components (and noise) above 3 kHz. Hence the low-pass filter is fairly complex, whereas the high-pass (above 300 Hz) filter is simple.

The output of the receiver is taken from the collector of T9 via C24 to the volume potentiometer P3. The output is also fed via C21 to T10 and T11, which form the AGC control circuit. The a.f. signal appearing at the emitter of T10 is rectified by D7 and smoothed by C25, so that a D.C. level appears at the base of T11 proportional to the a.f. signal level (which is dependent on the r.f. input level). When the voltage at the base of T11 exceeds about 1.5 V D3 and D4 will start to conduct, pre-

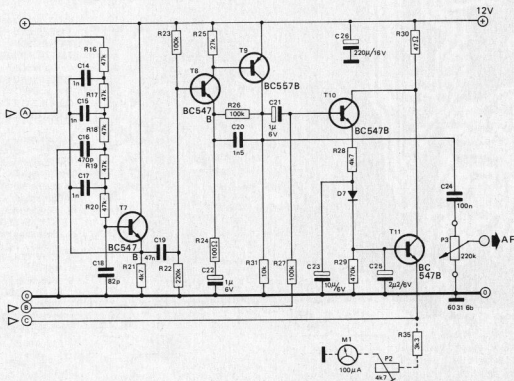
6a

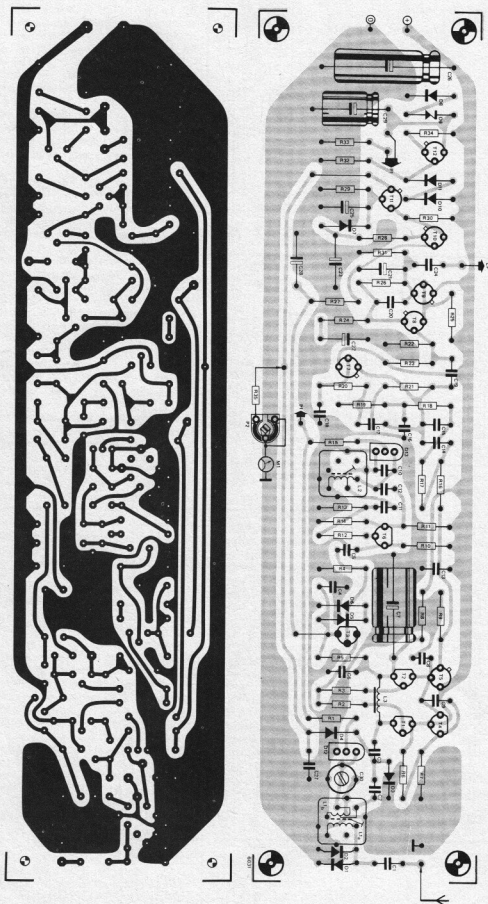
D1 ... D8, D10, D11 = 1N4148  
 D12, D13 = BB104



R33  
 100 k = 40 m  
 180 k = 20 m  
 82 k = 80 m

6b





### Parts list for figures 6 and 8.

**Resistors:**  
 R1, R15, R23, R26,  
 R27 = 100 k  
 R2, R3, R12, R24 = 100  $\Omega$   
 R4, R13, R35 = 3k3  
 R5, R9, R31, R32 = 10 k  
 R6 = 10 M  
 R7 = 3M9  
 R8 = 22 k  
 R10, R30 = 47  $\Omega$   
 R11 = 150 k  
 R14 = 68 k  
 R16, R17, R18, R19,  
 R20 = 47 k  
 R21, R28 = 4k7  
 R22 = 220 k  
 R25 = 27 k  
 R29 = 470 k  
 R34 = 1 k  
 R33 = see figure 6  
 P1 = 100 k lin  
 multitrn pot  
 P2 = 4k7 lin preset  
 P3 = 220 k log pot.

**Capacitors:**  
 C1, C14, C15, C17 = 1 n  
 C2, C12 = 27 p  
 C3, C11 = 330 p  
 C4, C6, C13, C24 = 100 n  
 C5, C16 = 470 p  
 C8 = 220 p  
 C9 = 120 n  
 C10 = 4p7  
 C18 = 82 p  
 C19, C27 = 47 n  
 C20 = 1n5  
 C7 = 470  $\mu$ 6 V  
 C21, C22 = 1  $\mu$ 6 V  
 C23 = 10  $\mu$ 6 V  
 C25 = 2 $\mu$ 2/6 V  
 C26 = 220  $\mu$ 16 V  
 C28 = 220  $\mu$ 4 V  
 C29 = 47  $\mu$ 10 V  
 C30 = 4 ... 20 p (trimmer)

**Semiconductors:**  
 T1, T2, T3, T6 = BF 494  
 T4 = E 300  
 T5, T7, T8, T10, T11 = BC 547 B  
 (or equ.)  
 T9, T12 = BC 557 B (or equ.)  
 D1 ... D8, D10, D11 = 1N4148  
 D9 = 8.2 V Z-Diode  
 D12, D13 = BB 104

**Miscellaneous:**  
 L1, L2 = Kachke screened  
 coil former with ferrite  
 core, consisting of the  
 following parts:  
 1. Base plate, GP 12/12-360  
 2. Coil former,  
 KH 3.5/12-357 I-III  
 3. Screening can,  
 AB 12/12/14-361  
 4. Core, G 3.5/0.5/K3/70/10  
 (pink)  
 5. Ferrite cap,  
 K 10.4/8.5C/K3/70/10  
 (pink)  
 For winding details: see text  
 M1 = 100  $\mu$ A f.s.d.

Figure 7. Layout of the p.c. board for the receiver (EPS 6031).

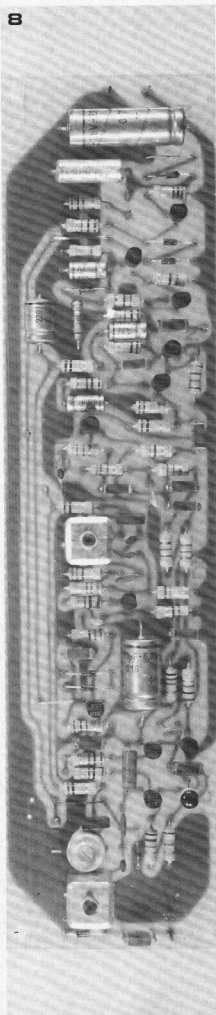
Figure 8. Component layout for figure 7.

senting a low impedance path to earth for the r.f. signal. Although the forward voltage drop of a silicon diode in full conduction is about 0.7 V the diode will start to conduct at about 0.3 to 0.4 volts. In this region the forward resistance is high, but decreases as the voltage across the diode is increased. It is this characteristic that is used to good advantage in the AGC circuit. At low r.f. input levels (and hence low a.f. output levels), the voltage fed back from the emitter of T11 is small and the diodes do not conduct. As the r.f. input increases the voltage applied to the diodes increases, so their forward resistance falls. The diodes form the lower arm of a potential divider with C2, so as the diode resistance decreases the r.f. signal level at the junction of C2 and C3 decreases.

Time constants in the AGC control circuit (R28, R29 and C23) ensure that the AGC does not follow the a.f. signal too rapidly as otherwise a clipping action would result, leading to distortion. Inclusion of the time constants means that the AGC can control only the average signal level, in the manner of a dynamic compressor.

### Construction

Figure 7 shows the printed circuit pattern for the receiver, and figure 8 gives



the component layout. This layout should be adhered to in order to avoid instability and other problems.

The coils are wound with 0.3 mm (31 S.W.G.) enamelled copper wire on screened coil formers with ferrite core (see parts list for details).

For reception on the 20 and 40 m bands L1A has 4 turns, and L1B and L2 each have 40 turns with the tap at 20 turns. For operation on the 80 m band L1A has 8 turns and L1B and L2 each have 80 turns with the tap at 40 turns. R33 must also have the appropriate value for the band to be received, to alter the tuning voltage range. L3 is simply a ready wound, fixed, 470  $\mu$ H inductor, such as Toko type 187LY-471.

The construction requires little additional comment, except that signal strength indication may be provided by a meter connected as shown dashed in figure 6b. The full-scale deflection of the meter should be about 100  $\mu$ A.

### Alignment

For correct operation of the receiver it is essential that the frequency of the BFO should be as close as possible to the frequency of the suppressed carrier, as otherwise the frequency spectrum of the a.f. signal will be shifted. As the a.f. signal is the difference output of the product detector, then if the BFO fre-

quency is shifted away from the true carrier frequency the a.f. signal will be shifted by the same amount. Although a shift of say 100 Hz at 14 MHz is only .0007%, the effect of a 100 Hz shift on the audio signal can be hilarious, with the speech sounding either like a basso profundo, or the chipmunks, depending on the direction of shift.

Fortunately, alignment of the receiver is fairly simple:

1. Select the correct time of day:  
80 m band: sunset to sunrise;  
40 m and 20 m bands:  
approx. 9-17 hrs GMT.
2. Screw in the cores of L1 and L2 until  $\frac{1}{4}$  of their length remains projecting outside the coil, and set C30 in the middle of its range.
3. Connect an aerial (minimum length 5 metres, or 15'-20') and switch on the receiver.
4. Tune to a transmission and adjust the core of L1 for maximum signal strength.
5. Check the frequency band for amateur transmissions. If none are heard, L1 and L2 need re-aligning. The core of L2 is turned very slowly until an amateur transmission is received; after every two or three turns of the core of L2, L1 will have to be re-adjusted for maximum signal strength. Having found the amateur band, L2 should be set so that this band is located symmetrically within the tuning range of the receiver.
6. Tune in to a transmission at the high frequency end of the tuning range, and adjust C30 for maximum signal strength.



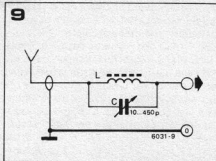


Figure 9. A wavetrapped antenna to reject interference from a medium wave AM broadcast transmitter.

Figure 10. There is scope for the experimenter to convert the receiver to a superhet by adding an r.f. stage, local oscillator, mixer and i.f. stages to the basic receiver.

7. Tune in to a transmission at the low frequency end of the tuning range, and adjust L1 for maximum signal strength.

8. Repeat steps 6 and 7 until no further improvement can be obtained.

Note: It is highly recommended to use the signal strength meter as an aid in aligning, because the AGC will make it very difficult to trim the receiver by ear. F.s.d. of the signal strength meter is set with P2, after tuning in to a local ham.

## Results

Although, in terms of selectivity the direct conversion receiver gives a poorer performance than that of figure 4, taking into account the cost saving the performance is quite acceptable.

Furthermore, the design has the advantage that the AGC controls the r.f. input direct, so the receiver can tolerate extremely high input voltages.

The sensitivity of the receiver is very good, and no significant advantage would be gained in this respect by using the system of figure 4. In the 20 and 80 m bands, the sensitivity for a signal-noise ratio of 10 dB was about 0.4  $\mu\text{V}$ . In the 40 m band it was marginally lower — about 0.5  $\mu\text{V}$ .

AM suppression is also excellent. To obtain the same LF signal output as for a 0.5  $\mu\text{V}$  SSB input, an AM input of 1.6 mV was necessary. This represents an AM suppression of 70 dB.

To give some idea of the AGC characteristic, the following output voltages were obtained:

r.f. input	a.f. output
0.5 $\mu\text{V}$	70 mV
5 $\mu\text{V}$	500 mV
50 $\mu\text{V}$	1 V

This gives some idea of the compression effect of the AGC. A 40 dB change in input voltage is compressed into a 23 dB change in output voltage over the range shown.

The current consumption of the receiver is very low. With an input signal of

150  $\mu\text{V}$  the current consumption was about 6 mA, and even with an input signal of several volts, such as can occur in the neighbourhood of a large transmitter, the current consumption was less than 10 mA.

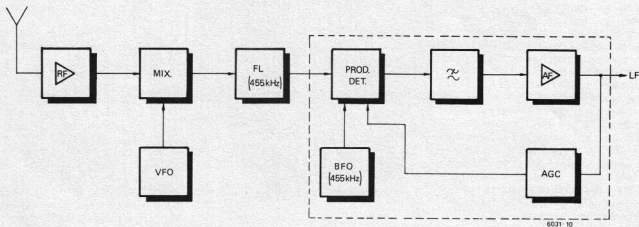
Despite the good AM suppression of the receiver, strong medium wave transmitters at short distances can still prove troublesome. Should this be the case then a filter may be used in the aerial lead of the receiver as shown in figure 9. For this wave trap about 60 turns of 0.2 mm (36 S.W.G.) enamelled copper wire may be wound on a 10 mm diameter ferrite rod 100 mm long. By adjusting the variable capacitor C (10-450 or 10-360 pF) the offending medium wave transmitter can be tuned out.

## Extension of the receiver

It is evident that the direct conversion receiver of figure 5 (i.e. the system used in the present design) has many points of similarity to the single conversion superhet receiver of figure 4.

There is thus scope for converting the receiver to a single conversion superhet by adding a local oscillator and mixer to convert the r.f. input signal to a fixed i.f. of say 455 kHz. Filtering and i.f. amplification may then take place before feeding into the product detector of the existing SSB receiver. The mixer may be preceded by a stage of r.f. amplification. The BFO and input stages of the existing receiver are now tuned to a fixed frequency (455 kHz), and tuning is accomplished in the normal superhet manner, by altering the tuning of the r.f. input stages and the frequency of the local oscillator. Having constructed the basic receiver there is thus great scope for the enthusiastic experimenter.

10



# triac relay

A solid-state replacement for a relay to switch A.C. loads may be constructed using the TCA 280A zero-voltage switch IC, a triac, and a few other components. It has several advantages over an electromechanical relay, such as freedom from contact bounce, elimination of contact wear due to arcing (hence virtually unlimited life) and reduced r.f. interference.

The circuit of the triac relay is given in figure 1. The TCA 280A IC derives its power supply direct from the mains via D1 and dropper resistor R1. R1 becomes very hot during continuous operation, so it should be adequately rated and provision should be made for cooling. The values of R1 and R2 depend on the required gate current of the triac used, the values given being suitable for the specified triacs, which will switch a load up to 1.5 kW resistive (lamps etc.).

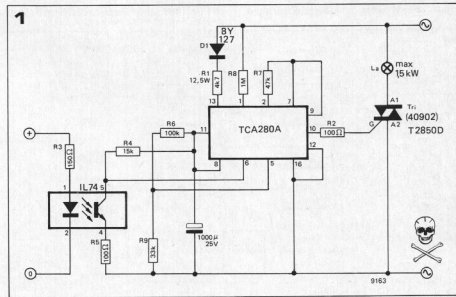
The trigger circuit inside the IC is synchronised to the mains frequency, and when the IC is activated it produces a sequence of ten trigger pulses around the zero-crossing point of the mains waveform. This ensures that the triac is triggered at a point on the waveform where the load voltage and current are small, and the r.f. interference generated is negligible, so no suppression is necessary.

The control input of the TCA 280A is pin 6. While the voltage at this pin is below 0.6 V the trigger pulse sequence is applied to the triac from pin 10. When the voltage at pin 6 exceeds 0.6 V the trigger pulses will be inhibited and the thyristor will not fire. The absolute

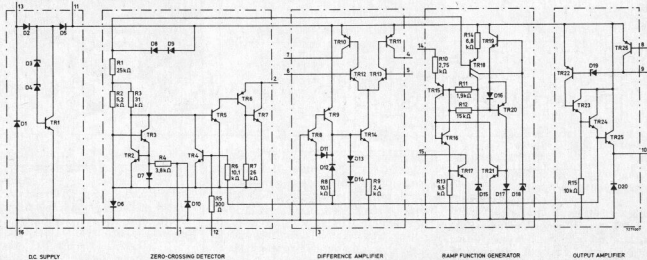
maximum voltage which may be applied to pin 6 is 15 V.

Control of the IC is accomplished using an opto isolator, so that there is no direct electrical connection between the control input and the mains. With no voltage applied to the control input the LED is not lit and the phototransistor is turned off. Pin 6 of the IC is thus pulled up by the voltage on R4 and the IC is inhibited so the triac will not fire. When a voltage is applied to the control input the LED lights, the phototransistor turns on, pulling down pin 6 so that the IC is activated and the triac is triggered. With the specified value of R3 the control voltage should not exceed 10 V. For higher input voltages R3 should be increased pro rata to limit the LED current to a safe value.

Note. When using this circuit (or triac dimmer circuits) to switch large incandescent lamp loads, remember that the cold resistance of a lamp filament is but a small fraction of the hot resistance. Large switch-on current surges of several times the normal running current thus occur, and the circuit must be de-rated accordingly.



TCA 280A: Internal circuit diagram



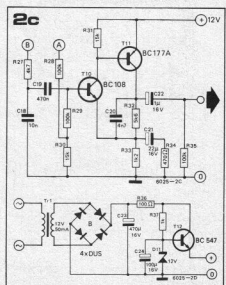
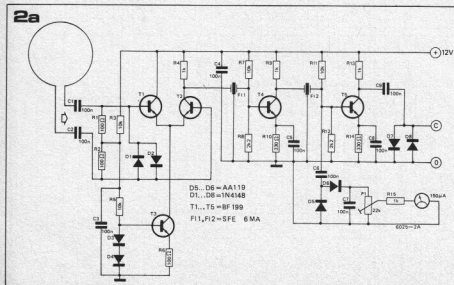
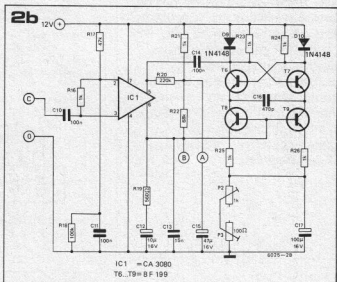
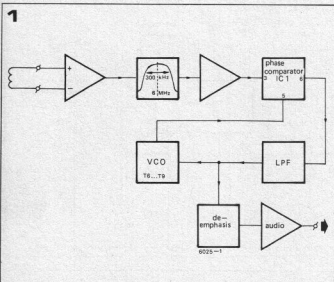
# TV sound - in brief

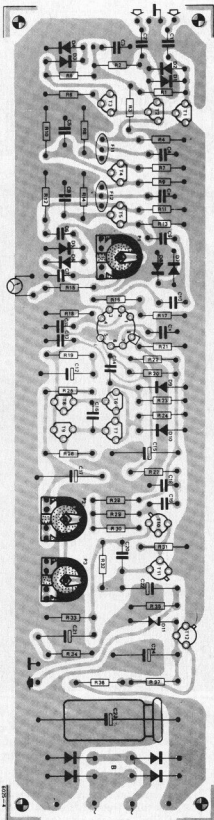
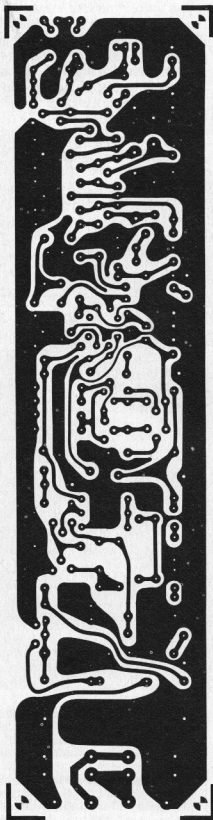
For those readers who have not seen the original 'TV sound' article (Elektor 2, p. 234), the circuits and p.c. board are repeated here.

## Principle of Operation

In figure 1 the signal from the pickup coil is amplified and filtered with a passband of 300 kHz. This filtered intercarrier signal is fed to one of the inputs of the phase comparator IC<sub>1</sub>. The other input comes from a voltage-controlled

oscillator (VCO). The output voltage of the phase comparator is proportional to the phase difference between its two inputs. This output is fed through a low-pass filter to the control input of the VCO. This control voltage alters the VCO frequency so that it tends to become the same as that of the



**Components List:****Resistors:**

$R_1, R_2, R_6, R_{36} = 100 \Omega$   
 $R_3, R_5, R_7, R_{11} = 10 \text{ k}$   
 $R_4, R_9, R_{13}, R_{15}, R_{16},$   
 $R_{21}, R_{23} \text{ to } R_{26}, R_{37} = 1 \text{ k}$   
 $R_{18}, R_{28}, R_{29}, R_{35} = 100 \text{ k}$   
 $R_{30}, R_{31} = 15 \text{ k}$   
 $R_8, R_{12} = 2 \text{ k}2$   
 $R_{10}, R_{14} = 330 \Omega$   
 $R_{17} = 47 \text{ k}$   
 $R_{19} = 560 \Omega$   
 $R_{20} = 220 \text{ k}$   
 $R_{22} = 68 \text{ k}$   
 $R_{27} = 4 \text{ k}7$   
 $R_{32} = 5 \text{ k}6$   
 $R_{33} = 1 \text{ k}2$   
 $R_{34} = 470 \Omega$

**Capacitors:**

$C_1 \text{ to } C_{11}, C_{14} = 100 \text{ n}$   
 $C_{12} = 10 \mu/16 \text{ V}$   
 $C_{13} = 15 \text{ n}$   
 $C_{15} = 47 \mu/16 \text{ V}$   
 $C_{16} = 470 \text{ p}$   
 $C_{17} = 100 \mu/6.3 \text{ V}$   
 $C_{18} = 10 \text{ n}$   
 $C_{19} = 470 \text{ n}$   
 $C_{20} = 4 \text{ n}7$   
 $C_{21} = 22 \mu/6.3 \text{ V}$   
 $C_{22} = 1 \mu/16 \text{ V}$   
 $C_{23} = 470 \mu/25 \text{ V}$   
 $C_{24} = 100 \mu/16 \text{ V}$   
 $C_x = 100 \text{ n}$

**Semiconductors:**

$IC_1 = CA 3080 \text{ (RCA)}$   
 $T_1 \text{ to } T_9 = BF 199$   
 $T_{10} = BC 108$   
 $T_{11} = BC 177 \text{ A}$   
 $T_{12} = BC 547$   
 $D_1 \text{ to } D_{10} = 1 \text{N}4148$   
 $D_{11} = 12 \text{ V}/400 \text{ mW zener diode}$   
 $B = 4 \times 1 \text{N}4002$

**Miscellaneous:**

$Tr = \text{Transformer } 12 \text{ V}/50 \text{ mA}$   
 $FL_1, FL_2 = 6 \text{ MHz ceramic filters,}$   
 e.g. SFE 6 MA (Murata)

intercarrier signal. When a VCO is 'locked-in' to a fixed-frequency signal the output of the low-pass filter is constant. However, the frequency of the intercarrier signal is not constant as it is frequency-modulated and the VCO frequency must follow the changes in frequency to remain locked-in. This means that the VCO control voltage must change. Since the change in control

voltage is proportional to the change in frequency it follows that the changes in control voltage are the audio signal which modulated the intercarrier signal. This phase-locked loop system thus demodulates the 6 MHz intercarrier signal and all that remains is to de-emphasise and amplify it.

Figure 2 shows the complete circuit.

**Alignment**

When this unit is used in conjunction with the front-end adapter, alignment is relatively simple.

All units are interconnected according to the wiring diagram shown. After the power has been switched on, and with no station tuned in, P2 and P3 on the TV sound board are simply set for maximum hiss at the audio output.

# TV-SOUND

## front-end adapter

This unit is intended for use in conjunction with the TV Sound Unit described in Elektor No. 2 (February 1975), to convert it into a complete AM/FM receiver, not only for TV sound but also for VHF FM broadcasts.



The purpose of the original TV Sound circuit was to extract a high-quality intercarrier sound signal from the TV, demodulate and reproduce it through a separate hi-fi audio system, thus bypassing the inferior a.f. stages and loud-speaker of the TV set.

The 'live-chassis' construction of TV sets makes a direct connection to the sound detector output dangerous. This can be overcome by the use of an isolating transformer, but if the set is rented it is unlikely that the rental company would allow modifications anyway. For these reasons it was decided to use a 'wireless' link between the TV set and a hi-fi installation. This took the form of a sensitive intercarrier sound channel with a phase-locked loop FM demodulator, which used a pickup coil on the set to extract the 6 MHz intercarrier signal radiated from the i.f.

transformers in the set.

The intercarrier sound pickup was designed in preference to a completely independent TV sound receiver for several reasons:

1. the TV sound pickup requires no front end and is therefore cheaper.
2. the unit reproduces the sound of whatever programme the TV set is tuned to, and does not have to be independently tuned.

However, with the introduction of TV sets using ceramic filters in the i.f. strip the amount of stray field available has been dramatically reduced. Increasing the sensitivity of the TV sound pickup will not overcome this because of problems due to spurious pickup of short wave transmissions etc. For this reason the front-end adapter was designed as an add-on unit so that constructors whose existing TV sound unit gave

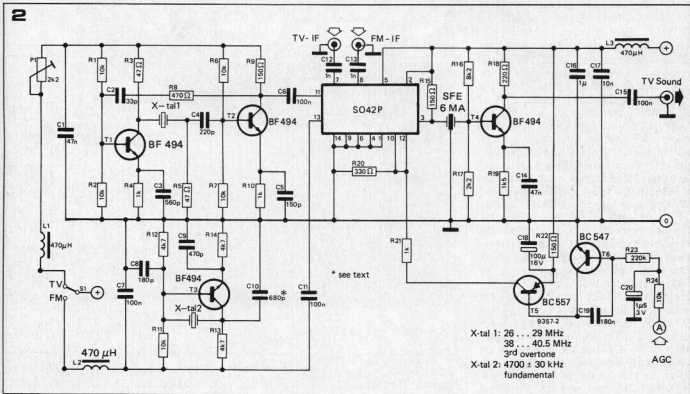
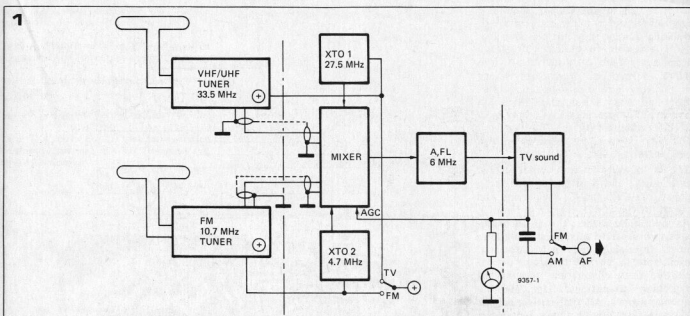
unsatisfactory results could convert it into a complete receiver.

Using commercially available UHF TV and VHF FM front-ends the adapter enables the reception of TV sound and FM broadcasts. As an additional option, provision is made for the reception of AM signals so that the sound from TV transmissions with amplitude modulated sound carrier can also be picked up.

### Principle of operation

Figure 1 shows the block diagram of the system, which is divided into three sections: Two front-ends (VHF/UHF TV and VHF FM radio), the adapter circuit proper and the existing TV Sound unit. The adapter uses double frequency conversion for both the FM radio and the TV sound.

The 33.5 MHz sound carrier leaving the



TV front-end is fed into the mixer together with the output of a crystal-controlled 27.5 MHz oscillator XT01. The resulting 6 MHz sound carrier is fed via an amplifier and bandpass filter to the input of the existing TV Sound unit, where it is further amplified and demodulated. The procedure for the FM signal is much the same. The 10.7 MHz output of the FM front-end is fed into the mixer together with the output of the 4.7 MHz oscillator XT02, and the resulting 6 MHz signal is amplified and demodulated by the TV Sound unit.

A point worth noting is that, since the bandwidth of a TV front-end is about 7 MHz it is not necessary to use a crystal of exactly 27.5 MHz in XT01. In the prototype an easily obtainable 27 MHz (radio control band) crystal was used.

The use of a double mixer (Siemens

Figure 1. Block diagram of complete receiver using TV and FM front-ends, adapter and existing TV sound unit.

Figure 2. Circuit diagram of the adapter.

SO42P) means that both the FM radio and TV-front-ends and their associated oscillators can be connected to the mixer simultaneously, thus simplifying switching between them, which is accomplished by switching off the H.T. supply to whichever one is not in use. The TV/FM changeover switch is shown in figure 1.

AGC is provided by feeding back a detected AM signal to pins 10 and 12

of the mixer. This considerably improves the AM suppression of the circuit. This signal is derived at the meter output on the existing TV Sound board, since at this point the 6 MHz carrier is rectified to drive the meter and thus indicates signal strength. It is also possible to derive an audio output at this point when receiving AM transmissions, and this option will be discussed later.

### Complete Circuit

Figure 2 shows the complete circuit of the central portion of the block diagram i.e. the adapter itself. The internal circuitry of the front ends will not be described as these are commercial units and the circuits will obviously depend on the manufacturer.

A word of warning would not come amiss at this point. There are on the

market vast quantities of scrap TV front-ends, and as many of these are of dubious quality they are best avoided. It is advisable to obtain a front-end from a reputable manufacturer such as Toko, Dormer and Wadsworth etc. or at the very least a new, boxed, surplus front-end from a reputable TV manufacturer. The problem does not arise to such an extent with the front end for FM radio, as there are less scrap ones on the market.

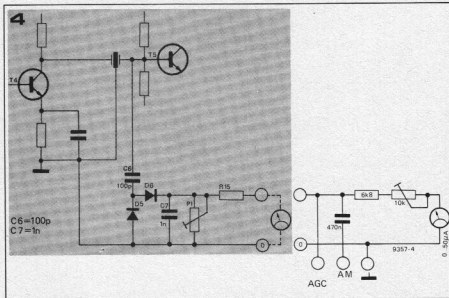
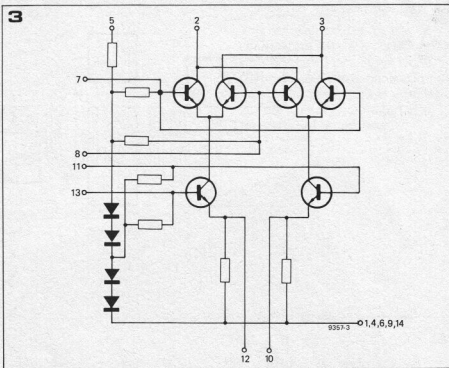
The i.f. outputs of both tuners are fed into pins 7 and 8 of the S042P via the internal capacitors C12 and C13. The internal circuit of the S042P is given in figure 3. As mentioned earlier, this IC incorporates two separate mixers, which allows both front-ends and their associated oscillators to be left in circuit permanently, thus eliminating complicated switching arrangements for high-frequency signals. All that is necessary is a single pole double throw switch S1, which switches the power supply to whichever front-end and oscillator are in use.

The local oscillator for the TV sound, XT01, comprises T1 and T2. The crystal must be of a type intended for operation on the third harmonic of the fundamental frequency, either 27.5 or 39.5 MHz, depending on whether the local oscillator frequency is to be above or below the 33.5 MHz i.f. output of the TV front-end. In either case the difference frequency is 6 MHz. As mentioned earlier, the crystal need not be exactly the specified frequency, and the frequency may be anywhere between 26 to 29 MHz or 38.5 to 40.5 MHz. Potentiometer P1 is used to reduce the supply voltage to XT01 to the minimum value consistent with reliable oscillation. This minimises interference caused by harmonics in the VHF and UHF bands.

The local oscillator circuit for the FM radio is built around T3 and uses a 4.7 MHz fundamental crystal (tolerance  $\pm 30$  kHz). In the S042P the outputs of the TV and FM front-ends are mixed with their respective local oscillators to provide the second i.f. output of 6 MHz to feed into the TV sound board.

To obtain the highest conversion gain (undesirable harmonics permitting!) the output voltages of XT01 and XT02 should both be approximately 500 mV peak-to-peak. For XT01 this level can be set with P1, as mentioned above. The output level of XT02, however, is set with C10. With certain types of crystals it can happen that the oscillator will not start; in this case no reception will be possible in the VHF-FM band. Should this problem arise, C10 can be reduced until the oscillator starts to work. The minimum value for C10 is 56pF.

In this application the S042P mixer does not provide adequate suppression of the input frequencies, so a SFE6MA 6 MHz ceramic filter is connected at the output to remove these components from the 6 MHz i.f. signal. T4 provides additional amplification of the output



signal which improves the sensitivity to around 10 microvolts, measured at the input to the adapter proper (i.e. not counting the gain in the front-end).

### AM Reception and Automatic Gain Control

AM suppression of the circuit may be improved considerably by the application of automatic gain control. The left-hand portion of figure 4 shows part of the existing TV sound circuit, where the output of the second stage is tapped off via C6, rectified (D5, D6) and used to drive the meter. The voltage appearing across C7 is proportional to the amplitude of the incoming carrier, so if the carrier happens to be amplitude modulated this voltage represents the a.f. signal. In any case, where the carrier amplitude varies the voltage across C7 varies in sympathy and may be used to provide AGC. The existing meter circuit must be modified as shown in the right-hand portion of figure 4. A more

sensitive (50 microamp) meter must be substituted for the existing 150 microamp meter, with a 10k potentiometer to adjust sensitivity. The existing meter control P1 should be turned up to maximum. The external connections to the original TV-Sound board are shown in greater detail in figure 7. Furthermore, if the (optional) AM output is required the values of C6 and C7 (on the original TV-sound board) must be changed, C6 (was 100n) becomes 100p and C7 (was 100n) becomes 1n.

Referring back to figure 2, the AGC signal is amplified by T5 and T6 and applied to pins 10 and 12 of the S042P. Referring to figure 3, which is the internal circuit of the S042P mixer, it can be seen that the AGC voltage is applied to the emitters of the two lower transistors, which alters the mixer conversion gain.

### Construction Notes

Construction of the circuit on the p.c.

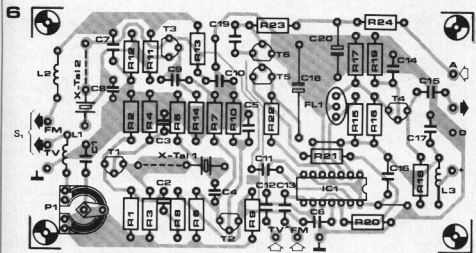
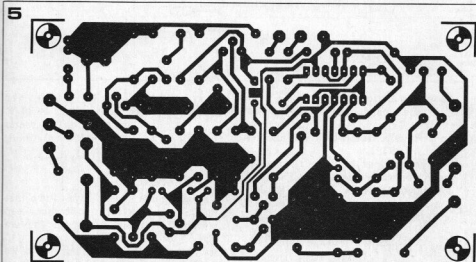
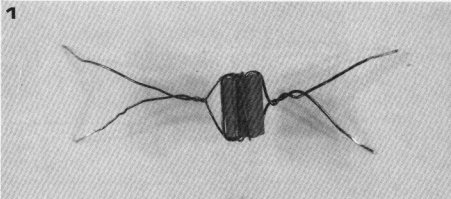
Figure 3. Internal circuit of the Siemens S042P balanced mixer IC.

Figure 4. Modifications to TV sound meter output to obtain AM output and AGC voltage.

Figure 5. Layout of adapter p.c. board. (EPS 9357).

Figure 6. Component layout for figure 5.

Photo 1. A ferrite bead is used as impedance transformer between the TV front-end and the S042P mixer.



#### Parts List

##### Resistors

R1, R2, R6, R7, R11, R24 = 10k  
 R3, R5 = 47 Ω  
 R4, R10, R15, R21 = 1k  
 R8 = 470 Ω  
 R9, R22 = 150 Ω  
 R12, R13, R14 = 4k7  
 R16 = 8k2  
 R17 = 2k2  
 R18 = 220 Ω  
 R19 = 1k5  
 R20 = 330 Ω  
 R23 = 220k  
 P1 = 2k2 (preset)

##### Capacitors

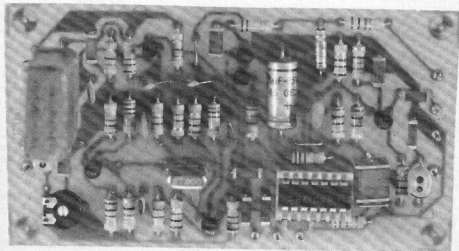
C1, C14 = 47n  
 C2 = 33p  
 C3 = 560p  
 C4 = 220p  
 C5 = 150p  
 C6, C7, C11, C15 = 100n  
 C8 = 180p  
 C9 = 470p  
 C10 = 680p (see text)  
 C12, C13 = 1n  
 C16 = 1 μ  
 C17 = 10n  
 C18 = 100 μ/16 V  
 C19 = 180n  
 C20 = 1 μ 5/3 V

##### Semiconductors

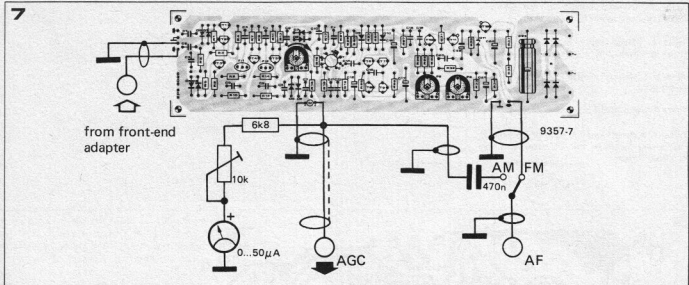
T1 . . . T4 : BF 494  
 T5 : BC 557  
 T6 : BC 547  
 IC : SO 42 P

##### Miscellaneous

L1, L2, L3 : inductor 470 μH  
 X-tal 1 : 26.29 MHz (3rd harmonic, or 38.40.5 MHz (ditto))  
 X-tal 2 : 4700 (±30) kHz (fundamental)  
 F11 : ceramic filter SFE 6 MA  
 S1 : s.p.d.t. switch







board of figure 5 should give little difficulty. Co-ax cable should be used for connection of the front-end i.f. outputs to the p.c. board. It is extremely important to prevent any interference between the various sections of the circuit due to interaction along the supply lines and it is thus necessary to thoroughly decouple the supplies to the front-ends and the p.c. board. For this purpose L1, L2 and L3 are included on the board, and the connections to the front-ends are indicated.

Interconnections between the adapter and the existing TV Sound board need little explanation. The pickup coil is, of course, redundant, and the output of the adapter feeds direct into one of the inputs of the differential input stage. The AGC output from the TV sound feeds into R24 on the adapter board. Note that if the unit is to be used for AM as well as FM reception then the values of C6 and C7 on the TV sound board should be changed to 100p and 1n respectively, as mentioned previously. It may also be necessary to remove C8 (on the TV sound board) to reduce the gain if the sensitivity is too high.

Apart from P1, the function of which has already been explained, the adapter requires no adjustments. On connection of suitable aerials it should be possible

to tune in stations on both the TV and FM radio bands (assuming that the existing TV sound board has been set up correctly, for which see Elektor, February 1975).

The connections between the various units (front-ends, adapter and TV sound) are shown in figure 10. Note that the metal cans of the front-ends must be connected direct to the metal chassis.

#### Power supply

It is quite possible to use the power supply on the original TV sound board to feed the adapter and front-ends as well. This is illustrated in figure 10. However, in this case the original power supply must be 'beefed up' (figure 8): the smoothing capacitor and series regulator transistor are replaced, and  $C_x$  is added. The secondary voltage from the mains transformer (Tr1) should be not less than 12 V and not more than 24 V; if this voltage is more than 18 V a cooling fin should be clipped onto T12.

If either or both of the front-ends have varicap tuning, a further regulated, smoothed and temperature-compensated supply of about 22 V will be needed. A suitable circuit is shown in figure 9; the 'raw' supply to this circuit can be taken from the smoothing elec-

trolytic (C23, figure 8), provided the transformer secondary voltage is 24 V. The original signal strength meter (150  $\mu$ A f.s.d.) can be used as tuning scale.

#### Final notes

Various measurements have shown that not all broadcasting authorities keep within the official limits for the deviation of the FM sound carrier. 'Officially', 75 kHz is the limit — but we have measured up to 120 kHz!

To cope with this without distortion, the hold range of the PLL in the original TV sound circuit must be increased. To this end, R20 can be reduced to 39k; this increases the hold range to 180 kHz, giving an ample safety margin.

The output impedance of most TV front-ends is 60  $\Omega$ , and the gain is often relatively low. Since the input impedance of the mixer is approximately 1k7, an impedance transformer will often give a distinct improvement. This transformer consists of a high-frequency type ferrite bead with a 60  $\Omega$  primary winding (1 turn) and a 1k7 secondary winding (6 turns), see photo 1. The wire diameter should be not less than 0.1 mm (SWG 42).

The output impedance of front-ends for VHF-FM is usually 150  $\Omega$ , and the gain

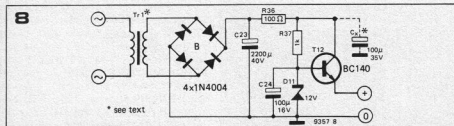


Figure 8. Modifications to the original power supply on the TV sound board, if it is to be used as power supply for the complete receiver.

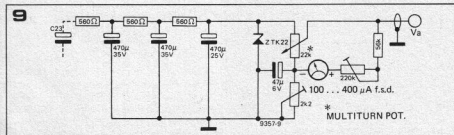
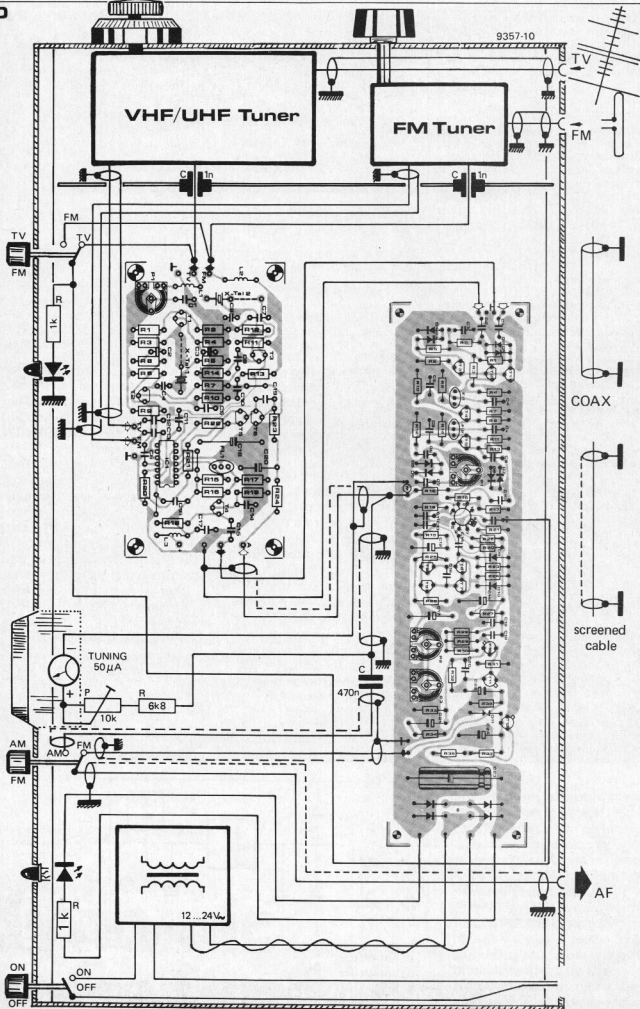


Figure 9. This circuit provides a regulated and temperature-compensated tuning voltage for varicap front-ends.

Figure 10. Point-to-point wiring diagram, showing how the various parts of the receiver are interconnected.

10



is usually higher. For these reasons, an impedance transformer will rarely be necessary here. Should one be required, it can be wound on a ferrite bead as turns; the primary should now be 3 turns and the secondary should be 9 turns.

### Performance

The sensitivity of the complete receiver is so great that it is often possible to obtain a usable TV sound signal when an ordinary TV set fails to produce either sound or picture. The measured performance of the prototype was as follows.

Sensitivity, FM	better than 10 $\mu$ V
Sensitivity, AM	better than 50 $\mu$ V
Signal-to-noise ratio	better than 40 dB
AM suppression with 40 kHz deviation and 50% AM	35 dB
Maximum deviation 75 kHz (R20=220k)	
180 kHz (R20= 39k)	

Table 1:

Modifications to original TV Sound board:

R20 = 39k (was 220k)  
 C6 = 100p (was 100n)  
 C7 = 1n (was 100n)  
 C23 = 2200  $\mu$ /40 V (was 470  $\mu$ )  
 T12 = BC140 (was BC547)

Additions to original TV Sound board:

AM output and AGC (figures 4 and 7):

1 x 6k8 resistor  
 1 x 10k preset potentiometer  
 1 x 470n capacitor  
 power supply (figure 8):  
 C<sub>X</sub> = 100  $\mu$ /35 V.

These values are valid for the combination:  
 adapter + TV-sound board.

In combination with 'normal' TV and FM front-ends the overall sensitivity will be:

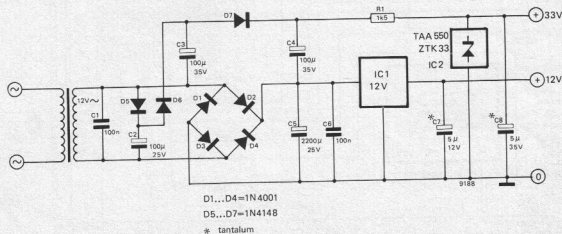
sensitivity, FM approx. 1  $\mu$ V.  
 sensitivity, AM approx. 5  $\mu$ V.  
 For clarity, the modifications and additions to the existing TV-sound circuit are summarised in table 1. M

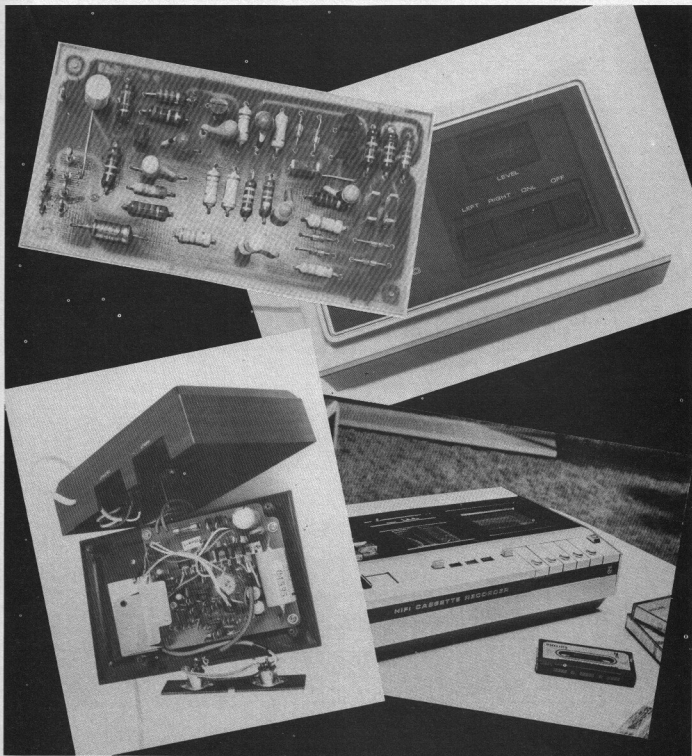
## power supply for varicap tuner

Most tuners with varicap front-ends require two supply voltages. One for the front-end and i.f. amplifier (usually about +12 V) and a tuning voltage for the varicaps (in excess of +30 V for maximum capacitance swing).

This would normally require an additional secondary winding on the mains transformer, but as the current required from the tuning voltage supply is small this difficulty can be overcome using the circuit given here. A transformer with a single 12 V secondary is used. The output is full-wave rectified by D1-D4 and is smoothed by C5 to give about 18 V D.C. An IC voltage regulator IC1 stabilizes the output voltage at 12 V for the front-end and i.f. strips. The choice of IC depends on the current

consumption of the tuner. The varicap tuning voltage is derived using a voltage tripler circuit D5-D7 and C2-C4. The resulting voltage is then stabilized to 33 V by the TAA 550 (IC2), which is a temperature compensated voltage reference. This provides an extremely stable, temperature independent tuning voltage for the varicaps, which can then be applied to the front end via the tuning potentiometer. The only small disadvantage of this circuit is that the voltage reference IC has a warm up time of about 20 seconds, so that the tuning of the receiver can be expected to drift during this period after switch-on. M





# dynamic noise limiter

One of the major problems with tape recorders in general, and cassette recorders in particular, is tape noise. For this reason, noise reduction systems are in demand — and several systems have been launched in past years.

The Philips DNL system described here has several advantages: it is relatively cheap, it can be added to existing equipment without difficulty and it only affects reproduction so that it can be used on existing (conventional) recordings.

The DNL system reduces or eliminates high frequencies (noise) during the quieter passages and pauses of a recording. During loud passages (near maximum modulation) the system is not operative — tape noise is masked by the audio signal in this case. The noise reduction during quiet passages results in an apparent increase in dynamic range.

The block diagram of the circuit is shown in figure 1. The input amplifier stage (A) is used for impedance matching to the tape recorder. From here the signal is fed into two parallel channels. The upper channel consists of a high-pass filter (B), amplifier (D) and variable and fixed attenuators (E) and (G). The lower channel consists of a phase-shifting network (all-pass filter, C) and a preset (or fixed) attenuator (F). The final output is the sum of the outputs of both channels.

The operating principle can be described briefly as follows. The output  $V_1$  of the all-pass network (C) is equal to the original signal, except for having an additional phase-shift. There will be no audible difference between this signal and the original. The output  $V_2$  of the high-pass filter contains the high-frequency portion of the original signal. For all frequencies the signals  $V_1$  and  $V_2$  are in anti-phase so that, if these two signals are summed, the high-frequency portion of the original signal is cancelled out. The net result is a low-pass filter.

For large input signal levels the variable attenuator (E) becomes operative, thereby reducing the contribution of  $V_2$  to the output signal. The high frequency content of  $V_1$  is no longer cancelled out: it is passed without attenuation to the output.

For readers who would like to see a more mathematically exact description (and we suggest that readers who don't like mathematics skip this paragraph): the transfer functions of the high-pass

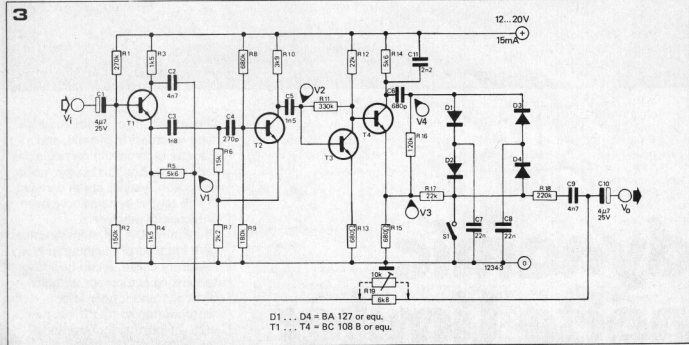
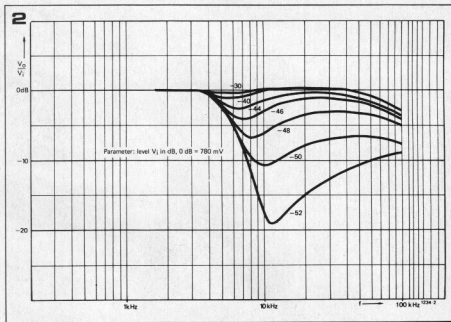
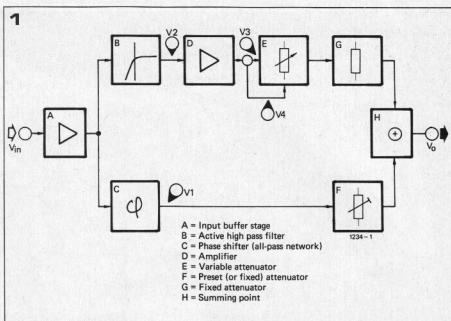


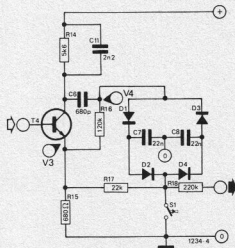
Figure 1. Block diagram of the DNL unit.

Figure 2. Performance of a basic DNL unit. As can be seen from this graph, it works as a low-pass filter as long as the high-frequency component of the signal is at a low level. As soon as the high-frequency component reaches a significant level the DNL becomes inoperative (flat frequency response).

Figure 3. Complete circuit of the DNL (one channel; for stereo two of these units are required).

Figure 4. This part of the circuit is the variable attenuator.

4



and all-pass networks are as follows:

high-pass:

$$H_h(p) = \frac{(pT)^3}{(1 + pT)(p^2T^2 + pT + 1)}$$

i.e. a third order Butterworth response;

$$\text{all-pass: } H_a(p) = \frac{1 - pT}{1 + pT}$$

When its input signal level is high, the variable attenuator will suppress the output from the high-pass filter; the output of the DNL is equal to the output of the all-pass filter in this case: a flat amplitude response. For low input levels, however, the variable attenuator adjusts to a setting where the total attenuation in the amplifier (D) and attenuators (E and G) is equal to the fixed attenuation in F. In this case the total transfer function of the DNL becomes the sum of the two transfer functions:

$$H_T(p) = H_h(p) + H_a(p) = \frac{1}{(1 + pT)(p^2T^2 + pT + 1)}$$

i.e. a third order Butterworth low-pass filter.

Summing it all up briefly: in the absence of high frequency signals of any importance, the DNL circuit will operate as a sharp (18 dB/octave) low-pass filter and thus reduce tape noise; however, if the original signal has a significant high-frequency content the filter action will become progressively less, until at a certain level it will be totally inoperative. The graphs shown in figure 2 illustrate this.

For the actual design, values must be chosen for three independent variables: — the corner frequency of the filter: if this is too high there will be little or no audible noise reduction; if it is too low, noise modulation effects will be audible on program material with mainly low-frequency content (e.g. pianosolo). The value chosen in this design is 5.5 kHz.

- the critical signal level at which the system starts to become inoperative. The choice depends on the nominal signal level at the input to the DNL and on the S/N ratio of the program source. The value chosen is approximately 2 mV, corresponding to -52 dB with respect to a 780 mV nominal level.
- the attack time constant of the variable attenuator. A slow attack will lead to some deterioration in transient response, but a fast attack can give rise to distortion at high frequencies — particularly in the critical region where the system is beginning to become inoperative. The value chosen is approximately 0.1 ms.

### The circuit

The complete circuit is shown in figure 3. Referring to the block diagram (figure 1), the circuit can be analysed as follows:

T1 is the input stage (A in figure 1). The input impedance is approximately 75 k. Simultaneously, T1 with the network C2/R5 works as all-pass filter (C in figure 1). The time constant is approximately  $C2 \cdot R5 \approx 27 \mu s$ .

R19 is the preset (or fixed) attenuator (F in figure 1); a 6k8 fixed resistor can be used for most applications. If a preset potentiometer (10 k) is used instead, this can be adjusted by playing an unmodulated tape and setting R19 for minimum hiss.

The active high-pass filter (B in figure 1) consists of T2, C3, R6, C4, R8/R9/R<sub>in</sub>, T2 and the feedback loop over R7. This is a second order filter; the third element of the total filter is C5 and R10 + R<sub>in</sub>, T3. The time constants are chosen to obtain the required corner frequency (5.5 kHz). The actual component values used differ slightly from the theoretical values, to compensate for a certain amount of mutual loading of the circuits.

Part of the signal amplification (D in figure 1) is already achieved in the active high-pass filter (T2); T3 is the

second half of the amplifier.

The components from T4 up to R18 are the variable attenuator (E in figure 1). This will be discussed in greater detail further on.

The fixed attenuator (G in figure 1) is simply R17 + R18.

The summing point (H in figure 1) is the junction C9 - R19 - C10.

### The variable attenuator

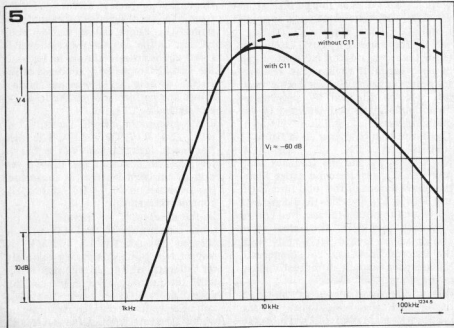
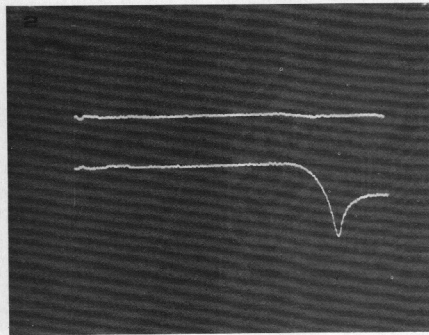
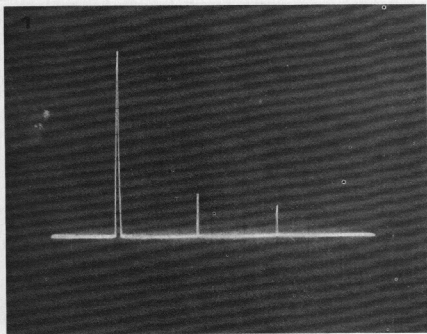
This part of the circuit is shown separately in figure 4.

The input signal is amplified by T4 and passed through a further high-pass filter (C6, R16) to obtain the desired control voltage (V<sub>4</sub>) for the variable attenuator. C11, in conjunction with R14, gives a high frequency roll-off at a slightly higher corner frequency. The result of this is that the attenuator becomes progressively less effective at higher input frequencies as the control voltage decreases (figure 5). Conversely, if the attenuator is less effective, the DNL as a whole becomes more effective towards higher frequencies: a larger high-frequency component will be subtracted from the main signal at the summing point. This effect can be seen by comparison of the characteristics shown in figure 6 with those shown in figure 2: the latter characteristics are those of the circuit without C11, whereas figure 6 shows the performance of the total circuit, including C11.

The attenuator itself consists of D1...D4, R17, C7 and C8. The high-frequency input signal (V<sub>3</sub>) is fed to the junction D1 - D3: this is the control voltage (V<sub>4</sub>).

In the absence of any input signal, the tank capacitors C7 and C8 will be charged through R16-D1 and R17-D4 respectively to approximately the emitter potential of T4. C6 will also charge until the junction C6-R16 reaches this potential.

Let us now first consider the situation where the signal level at the input is so



low that, even after amplification in T4, it cannot produce a sufficiently large control voltage to forward-bias D1 or D3. It will be obvious that, in this case, the input signal ( $V_3$ ) will certainly be insufficient to forward-bias D2 or D4.  $V_3$  is approximately one-eighth of  $V_4$ , and  $V_4$  is itself insufficient to forward-bias the diodes! The cancellation signal is thus passed without any further attenuation: the DNL is at its most active. Next consider the situation where the input signal is at a much higher level — say 500 mV. The peak value of the control voltage will be some 5.8 V in this case, so that C7 and C8 would be charged to more than 5 V above or below their original potential — if that were possible. However, D2 and D4 are connected in series between the two capacitors, so that the voltage difference between them can never be larger than about 1.4 V, i.e. two diode-drops. D2 and D4 are now forward-biased, so that they form an effective short-circuit for audio signals. In this situation, R17 and C7/C8 constitute a low-pass filter with a corner frequency of approximately 300 Hz — giving an attenuation of 20 or more above 5.5 kHz. The DNL as a whole is inoperative: there is practically no cancellation of high frequencies.

It is possible to estimate the effect of the attenuator between the two extreme cases described above by referring to figure 2. The results of some brief calculations, based on these characteristics and the estimated gain or attenuation of the various stages, are summarised in Table 1.

Reading first from left to right: the input voltage to the DNL is given in dB, 0 dB being defined as 780 mV. The input level in mV can thus be calculated, and from this the input voltage to the attenuator ( $V_3$ ) can be estimated. This, in turn, gives the peak value of the control voltage ( $V_4$ ).

Now, reading from right to left:  $V_0/V_{in}$  is given in dB for the various levels of  $V_{in}$ ;  $V_0$  can be calculated from this. The difference between  $V_0$  and  $V_{in}$  is equal to the high frequency cancellation component coming from the variable attenuator; an estimate of the fixed attenuation due to R18 gives the signal level at the D2-D4 junction:  $\alpha V_3$ . Since  $V_3$  is known, the attenuation factor  $\alpha$  can be calculated.

It will now be obvious that the first extreme case outlined above — very low signal level — corresponds to the situation for signal levels of 2 mV or less. The control voltage is 460 mV or less, so that the diodes are blocked and the attenuator is almost inoperative ( $0.9 \leq \alpha < 1$ ). The second extreme case — high signal level — corresponds to signal levels of 25 mV (or more): the diodes are almost in saturation, and the attenuation factor has practically reached the theoretical limit of 0.05 determined by the low-pass network R17, C7/C8. Finally, to pick one intermediate value: at an input level of 3.1 mV the peak value of the control voltage will be approximately 720 mV.

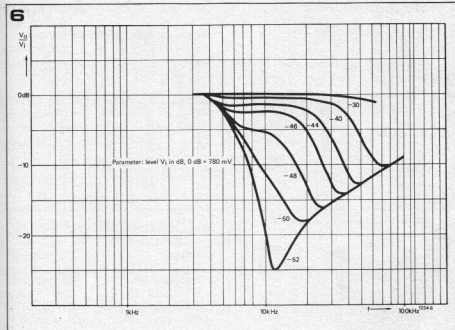


Figure 5. Control voltage ( $V_d$ ) as a function of frequency, at a fixed input level, showing the influence of the capacitor C11.

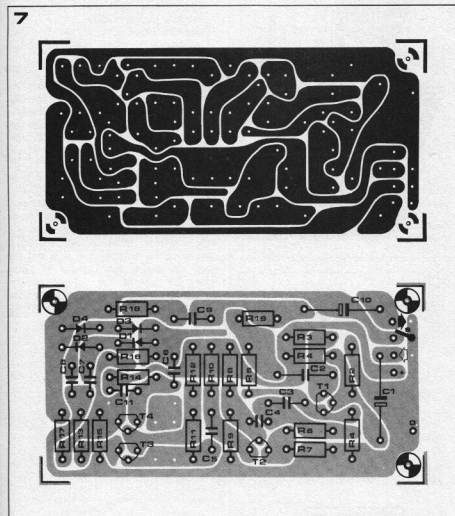
Figure 6. Performance of the DNL unit described here, i.e. with capacitor C11 included.

Figure 7. The p.c. board and component layout (EPS 1234).

Figure 8. A simple power supply, which can be used if the supply cannot be derived from the main equipment.

Photo 1. Harmonic distortion of the DNL. Test signal 5 kHz, 500 mV; harmonics less than -54 dB (0.2%).

Photo 2. Frequency response for an input level of 25 mV (upper trace) and for 2.5 mV (lower trace). The dip is at approximately 11 kHz, and 25 dB down.



#### Parts list for figures 3 and 7

##### Resistors:

- R1 = 270 k
- R2 = 150 k
- R3, R4 = 1k5
- R5, R14 = 5k6
- R6 = 15 k
- R7 = 2k2
- R8 = 680 k
- R9 = 180 k
- R10 = 3k9
- R11 = 330 k
- R12, R17 = 22 k
- R13, R15 = 680  $\Omega$
- R16 = 120 k
- R18 = 220 k
- R19 = 6k8 fixed or 10 k preset (see text)
- P1 = 100 k or 220 k preset (see text)

##### Capacitors:

- C1, C10 = 4 $\mu$ 7/25 V
- C2, C9 = 4n7
- C3 = 1n8
- C4 = 270 p
- C5 = 1n5
- C6 = 680 p
- C7, C8 = 22 n
- C11 = 2n2

##### Semiconductors:

- T1 ... T4 = BC108B or equ.
- D1 ... D4 = BA127 or equ.

##### Miscellaneous:

- S1 = SPST (mono version), or DPST (stereo version).

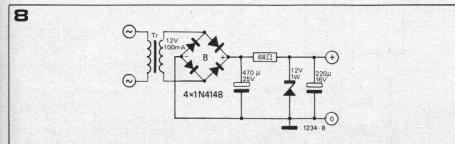




Table 1. An estimate of the variable attenuator action, as derived from the DNL performance shown in figure 2.

Figure 9. Two possible arrangements for the input attenuator. The arrangement of figure 9a reduces the input impedance, whereas the other arrangement increases it.

Figure 10. The DNL can be connected between the cassette recorder and a main amplifier (10a) or it can be included in the cassette recorder itself (10b).

The diodes are then just on the verge of conduction, and the attenuation factor produced to be approximately 0.53.

One final point is perhaps worthy of note. The fact that the control voltage  $V_4$  can be 5.8 V or more does not mean that the voltage across D1 or D3 can reach this value. Nor does it mean that the voltage on C7 or C8 will swing by this much. C7 and C8 are more than 30 times greater than C6, so the effect of a large swing in control voltage will be minor 'charge-pumping' from C8 to C7, followed by the charge flowing back from C7 to C8 through D2 and D4. It is this flow which keeps D2 and D4 in conduction.

The DNL can be switched out of operation entirely by closing S1.

### Construction and alignment

The p.c. board and component layout are shown in figure 7. The power supply can be relatively simple. The required 12...20 V at 15 mA can usually be derived from the main equipment. If this is not possible for some reason, a simple supply as shown in figure 8 will suffice.

For the unit to operate properly, it is essential that the load impedance at the output of the DNL is greater than 20 k $\Omega$ . This should not create any real problems with modern equipment.

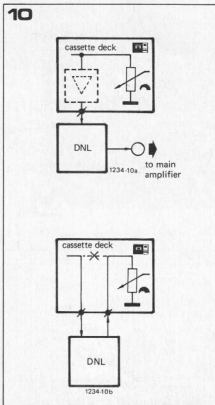
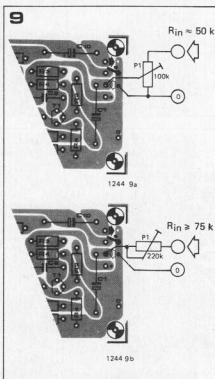
It is even more essential, however, that the input signal to the DNL is at the correct level. As Table 1 shows, the noise level at the input should be 2...3 mV. If the noise is at a lower level the DNL will still work, but it will reduce the low-level, high-frequency portion of the audio signal more than is necessary. On the other hand, if the noise is at too high a level, the DNL will not operate at all!

The S/N ratio of the average cassette recorder will be 46...48 dB. The requisite noise level (2...3 mV) thus corresponds to a nominal signal level of approximately 500 mV; if the recorder output is higher than this, an attenuator will have to be added at the DNL input. A simple solution is to use a 100 k preset potentiometer, as shown in figure 9a; alternatively, a 220 k preset pot can be included in series with the input (figure 9b).

If there is any doubt as to the correct setting of the input level, a simple align-

Table 1

	$V_{in}$ (dB)	$V_3$ (mV)	$V_4$ , peak (mV)	$\alpha$	$\alpha \cdot V_3$ (mV)	$V_{in} - V_0$ (mV)	$V_0$ (mV)	$V_0/V_{in}$ (dB)
	-30	25	500	0.06	28	1.4	24	- 0.5
	-40	7.8	156	0.11	17	0.8	7.0	- 1.0
	-48	3.1	62	0.53	33	1.6	1.5	- 6.5
	-50	2.5	50	0.72	36	1.8	0.7	-11
	-52	2.0	40	0.90	36	1.8	0.2	-19



ment procedure is as follows:

- open switch S1.
- connect a dc voltmeter (10...50 k $\Omega$ /Volt), set at its highest sensitivity, between the D1-D2-C7 junction and the D3-D4-C8 junction; + to C7, - to C8. The meter should read 0 V.
- play an erased tape. The tape noise may cause the meter to show a slightly higher reading.
- set the input level to the DNL, by adjusting P1, until the pointer just starts to move up from 0 V.

The input level is now correctly set, so the meter can be removed. The DNL unit should now operate satisfactorily.

If a preset potentiometer is used instead of R19, this may also need adjustment:

- with S1 open, play an erased tape.
- set R19 for minimum noise at the output.

From the above it will also be obvious that the input signal to the DNL unit must be at a fixed level. This means that it must come straight from the playback preamplifier, before the tone and volume controls. Most cassette recorders have such an output, if this is not the case, the signal can usually be taken from the top of the volume control potentiometer. This is illustrated in figure 10.

# TUP TUN DUG DUS

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP' (Transistor, Universal PNP), 'TUN' (Transistor, Universal NPN), 'DUG' (Diode, Universal Germanium) or 'DUS' (Diode, Universal Silicon). This indicates that a large group of similar devices can be used, provided they meet the minimum specifications listed in tables 1a and 1b.

For further information, see the article 'TUP-TUN-DUG-DUS' in Elektor 1, p. 9.

	type	$U_{ce0}$ max	$I_c$ max	$h_{fe}$ min.	$P_{tot}$ max	$f_T$ min.
TUN	NPN	20 V	100 mA	100	100 mW	100 MHz
TUP	PNP	20 V	100 mA	100	100 mW	100 MHz

Table 1a. Minimum specifications for TUP and TUN.

Table 1b. Minimum specifications for DUS and DUG.

	type	$U_R$ max	$I_F$ max	$I_R$ max	$P_{tot}$ max	$C_D$ max
DUS	Si	25 V	100 mA	1 $\mu$ A	250 mW	5 pF
DUG	Ge	20 V	35 mA	100 $\mu$ A	250 mW	10 pF

Table 2. Various transistor types that meet the TUN specifications.

TUN		
BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP		
BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG
BA 127	BA 318	OA 85
BA 217	BAX 13	OA 91
BA 218	BAY 61	OA 95
BA 221	1N914	AA 116
BA 222	1N4148	
BA 317		

Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification ( $I_{c,max} = 50$  mA).

	NPN	PNP
	BC 107 BC 108 BC 109	BC 177 BC 178 BC 179
$V_{ce0}$ max	45 V 20 V 20 V	45 V 25 V 20 V
$V_{eb0}$ max	6 V 5 V 5 V	5 V 5 V 5 V
$I_c$ max	100 mA 100 mA 100 mA	100 mA 100 mA 50 mA
$P_{tot}$ max	300 mW 300 mW 300 mW	300 mW 300 mW 300 mW
$f_T$ min.	150 MHz 150 MHz 150 MHz	130 MHz 130 MHz 130 MHz
F max	10 dB 10 dB 4 dB	10 dB 10 dB 4 dB

The letters after the type number denote the current gain:

- A:  $\alpha'$  ( $\beta$ ,  $h_{fe}$ ) = 125-260  
 B:  $\alpha'$  = 240-500  
 C:  $\alpha'$  = 450-900.

Table 6. Various equivalents for the BC107, -108, ... families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107	BC 177		
BC 108	BC 178		
BC 109	BC 179		
BC 147	BC 157		$P_{max} = 250$ mW
BC 148	BC 158		
BC 149	BC 159		
BC 207	BC 204		
BC 208	BC 205		
BC 209	BC 206		
BC 237	BC 307		
BC 238	BC 308		
BC 239	BC 309		
BC 317	BC 320		$I_{c,max} = 150$ mA
BC 318	BC 321		
BC 319	BC 322		
BC 347	BC 350		
BC 348	BC 351		
BC 349	BC 352		
BC 407	BC 417		$P_{max} = 250$ mW
BC 408	BC 418		
BC 409	BC 419		
BC 547	BC 557		$P_{max} = 500$ mW
BC 548	BC 558		
BC 549	BC 559		
BC 167	BC 257		169/259
BC 168	BC 258		$I_{c,max} = 50$ mA
BC 169	BC 259		
BC 171	BC 251		251 ... 253
BC 172	BC 252		low noise
BC 173	BC 253		
BC 182	BC 212		$I_{c,max} = 200$ mA
BC 183	BC 213		
BC 184	BC 214		
BC 582	BC 512		$I_{c,max} = 200$ mA
BC 583	BC 513		
BC 584	BC 514		
BC 414	BC 416		low noise
BC 414	BC 416		
BC 414	BC 416		
BC 414	BC 416		low noise
BC 413	BC 415		
BC 413	BC 415		
BC 382			
BC 383			
BC 384			
BC 437			$P_{max} = 220$ mW
BC 438			
BC 439			
BC 467			$P_{max} = 220$ mW
BC 468			
BC 469			
	BC 261 BC 262 BC 263		low noise

# TUP TUN DUG DUS



# integrated voltage regulators

Variations in power supply voltage can have a detrimental effect on the functioning of many electronic circuits. In such cases provision of a stable, ripple-free supply voltage is essential. Until a few years ago voltage regulators were designed almost exclusively using discrete components, but in the past couple of years there has been a proliferation of integrated circuit voltage regulators, so that for many applications it is hardly worth designing a power supply with discrete components. In addition, IC regulators usually offer significant cost reduction. The first part of this article deals with IC regulators in general, and with the universal precision voltage regulator type 723 in detail. Part 2 deals with 'three-legged' fixed-voltage regulators.

The general principles embodied in integrated voltage regulators are the same as those used in circuits built from discrete components (figure 1). The output voltage of the regulator, or a portion of it, is compared to a stable reference voltage (1) in a differential amplifier (2). The error voltage (difference between the reference and the output voltage) is amplified by the differential amplifier and used to control an output stage (3) usually a series pass transistor. This effectively functions as a voltage-controlled variable resistor (shown dotted). Should the output voltage attempt to fall, due to increased load current or for any other reason, then the error voltage seen by the differential amplifier will increase. The output voltage of the differential amplifier therefore rises, turning the series pass transistor harder on and thus tending to increase the output voltage. The circuit is, of course, simply a D.C. power amplifier, which amplifies the reference voltage and provides the necessary output current capability.

Since the circuit is attempting to function as a constant voltage source, under fault conditions such as short-circuits on the output the series transistor would dissipate considerable power and could easily be destroyed. For this reason protection circuits are generally included in IC regulators, which protect the output device by limiting the output current, and also safeguard the entire chip by providing thermal shut-down in the event of excessive power dissipation and overheating.

## Grouping

There are two distinct types of voltage

regulator IC. The universal type, such as the 723, whose output voltage can be varied over a wide range using external components, and the fixed voltage type, which are available with commonly used fixed output voltages such as 5 V for TTL. A commonly used device of this type is the LM 309. Also available are devices that provide both positive and negative output voltages such as  $\pm 10$  or  $\pm 15$  V for operational amplifiers.

In general, the universal type of IC regulator has a relatively small maximum output current, typically between 25 and 150 mA. The output current can easily be increased by the use of external power transistors. On the other hand, the fixed voltage type of regulator is principally intended for use with a minimum of external components, and consequently a substantial output current capability is built into the chip. The smallest of such devices can supply currents of the order of 100 mA, and the largest can supply currents in excess of 1 A.

## The 723 precision voltage regulator

Practically all semiconductor manufacturers who produce IC voltage regulators include the 723 in their range. The pin connections of both the packages in which it is obtainable are given in figure 2, as is the internal circuit. From left to right in the circuit can be recognised the internal voltage stabilisation around D1, the temperature compensated reference voltage around D2, the differential amplifier stage Q11/Q12, the control amplifier Q14 and the output transistor Q15. Q16 is the current limit transistor. A resistor is connected

between the base and emitter of this transistor that carries the load current, and when the voltage drop across this resistor becomes high enough to turn on Q16 then the drive to the output stage is limited.

The zener D3 is only included in the DIL packaged version of the regulator as the metal can version does not have sufficient pins to include it. If D3 is required in a circuit when using the metal can version then it must be added externally. The pin connections to the IC are also shown alongside the circuit diagram. The numbers in brackets refer to the DIL package version.

The absolute maximum ratings of the IC are given in table 1, and table 2 lists the more important specifications of the device. Of particular interest are the high stability of the output voltage and the outstanding ripple rejection (74 dB). This can be further improved to 86 dB, by the inclusion of a capacitor across the reference voltage output.

A replacement for the 723, the Signetics 550 regulator, has similar, and in some cases better, parameters, at a somewhat higher cost. Note however that the reference voltage of the 550 is only 1.63 V.

### Basic circuits using the 723

For equipment requiring supply currents not much in excess of 100 mA (150 mA absolute maximum) no external power transistor is necessary to use the 723 as a positive voltage regulator.

Depending on the required output voltage there are two basic circuits that may be used. The value of the reference voltage lies between 6.8 and 7.5 volts (7.15

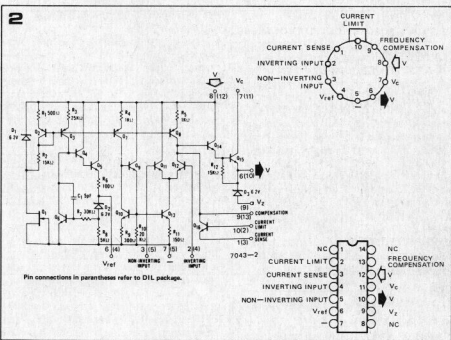
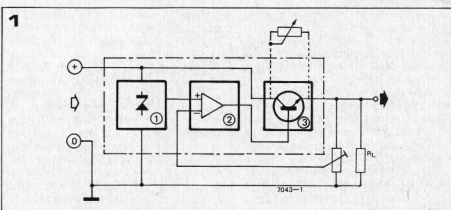


Table 1.

#### ABSOLUTE MAXIMUM RATINGS

$\mu A 723C$

Continuous Voltage from $V^+$ to $V^-$	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from $V_{REF}$	15 mA
Current from $V_z$	25 mA
Internal Power Dissipation	800 mW
Operating Temperature Range	0 to 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	300°C

Figure 1. An integrated voltage regulator comprises a reference voltage source, an error amplifier and an output stage.

Figure 2. Pinout and internal circuit of the 723 regulator IC. The numbers in parentheses are the pin connections of the DIL version.

Table 1. Absolute maximum ratings of the 723 regulator IC.

Table 2. Electrical characteristics of the 723.

Table 2.

#### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ C$ unless otherwise specified) $\mu A 723 C$

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Line Regulation	0.01	0.1	0.1	% $V_{out}$	$V_{in} = 12V$ to $V_{in} = 15V$
	0.1	0.5	0.5	% $V_{out}$	$V_{in} = 12V$ to $V_{in} = 40V$
Load Regulation	0.03	0.2	0.2	% $V_{out}$	$I_L = 1mA$ to $I_L = 50mA$
Ripple Rejection	74			dB	$f = 50 Hz$ to 10 kHz, $C1 = 0$
	86			dB	$f = 50 Hz$ to 10 kHz, $C1 = 5 \mu F$
Short Circuit Current Limit	65			mA	$R_{sc} = 10 \Omega$ , $V_{out} = 0$
Reference Voltage	6.80	7.15	7.50	V	$BW = 100 Hz$ to 10 kHz, $C1 = 0$
Output Noise Voltage	20			$\mu V$ rms	$BW = 100 Hz$ to 10 kHz, $C1 = 5 \mu F$
	2.5			$\mu V$ rms	$I_L = 0$ , $V_{in} = 30V$
Long Term Stability			0.1	%/1000 hrs.	
Standby Current Drain		2.3	4.0	mA	
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation			0.3	% $V_{out}$	
Load Regulation			0.6	% $V_{out}$	
Average Temperature Coefficient of Output Voltage	0.003	0.015		%/°C	$V_{in} = 12V$ to $V_{in} = 15V$ $I_L = 1mA$ to $I_L = 50mA$

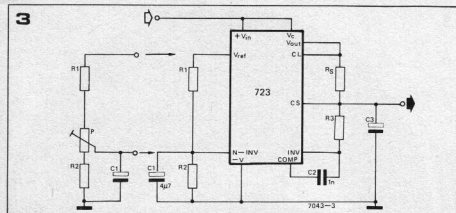


Figure 3. Basic circuit using the 723 regulator for output voltages between +2 and +7 V.

Figure 4. Variation in current limiting characteristics with temperature (current limit nominally 60 mA at 25°C). The limit current reduces at higher temperatures, thus providing a degree of thermal protection.

Figure 5. Basic circuit using the 723 for output voltages between +7 and +37 V.

Figure 6. Use of an external NPN power transistor to increase the output current.

Figure 7. A 5 V 1 A supply using an external PNP power transistor.

Table 3. POSITIVE OUTPUT VOLTAGES.

Output (V)	fixed output voltage		output variable ± 10%		refers to figures
	R1	R2	R1	P	
+3.0	4.12	3.01	1.8	0.5	1, 2
+3.6	3.57	3.65	1.5	0.5	1, 5
+5.0	2.15	4.99	.75	0.5	2, 2
+6.0	1.15	6.04	0.5	0.5	2, 7
+9.0	1.87	7.15	.75	1.0	2, 7
+12	4.87	7.15	2.0	1.0	3, 5
+15	7.87	7.15	3.3	1.0	3, 5
+28	21.0	7.15	5.6	1.0	5, 6
+45	3.57	48.7	2.2	10	39
+75	3.57	78.7	2.2	10	68
+100	3.57	102	2.2	10	91
+250	3.57	255	2.2	10	240

all resistance values in k $\Omega$

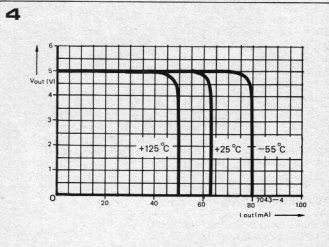
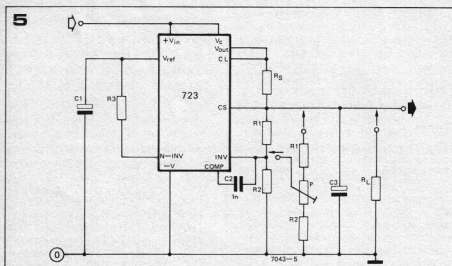


Table 3. Values of potential divider resistors R1 and R2 for various (positive) output voltages.



nominal). For output voltages less than this the circuit of figure 3 must be used. A potential divider, R1/R2 divides down the reference voltage to the value of the required output voltage, and it is then fed into the non-inverting input of the IC. The output voltage is fed back direct into the inverting input. With this circuit output voltages of between +2 and about +7 V can be obtained by suitable choice of R1 and R2. The ratio of R1:R2 can be calculated using the equation:

$$V_{out} = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$$

The nominal value of  $V_{ref}$  (7.15 V) should be used in this calculation. When

choosing the actual values for R1 and R2 it should be remembered that the  $V_{ref}$  output should not be loaded excessively, and it is recommended that R1 and R2 be chosen so that the current through them is about 1 mA. This means that the total value of  $R_1 + R_2$  is about 7 k.

The first four rows of table 3 give the values of R1 and R2 for output voltages between 3 and 6 V (the rest of table 3 will be discussed later). The values thus obtained are odd values not found in any preferred value range. In view of this, and to compensate for component tolerances and variations in  $V_{ref}$  it is recommended that a preset pot be included between R1 and R2, as shown on the left of figure 3. Using the values

for R1, R2 and P given on the right of table 3 the output voltage may be varied by about  $\pm 10\%$ .

In figure 3 capacitor C1 considerably reduces noise on the output caused by the voltage reference diode. The specified value of 4 $\mu$ F is adequate, but larger values can only improve matters. All manufacturers of the 723 recommend the use of tantalum capacitors for C1 and C3. C3 is not essential, but it improves the stability of the circuit and noticeably reduces the hum level. This can easily be verified by observing the output voltage both with and without C3.

R3 affects the temperature stability of the circuit, and for minimum temperature coefficient of the output volt-

age the source impedance seen by the inverting input (essentially R3) should be the same as that seen by the non-inverting input (R1 in parallel with R2). Thus the value of R3 is given by:

$$R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$$

Resistor R<sub>S</sub> is the current sensing resistor that determines at what load current the current limit starts to operate. The output current flows through R<sub>S</sub>, and when sufficient current flows to cause a voltage drop of about 0.7 volts across R<sub>S</sub> then Q16 will turn on, limiting the drive to the output stage. R<sub>S</sub> is thus easily calculated.

$$R_S = \frac{0.7}{I_{lim}} (\Omega, V, A)$$

Figure 4 shows that the onset of current limiting occurs sooner as the device temperature increases, so within certain limits the IC is protected against thermal overload. Nevertheless the device should be provided with an adequate heatsink, particularly when operating near the maximum current or power ratings.

### Output voltage +7 to +37 V

For output voltages in excess of +7 V the circuit of figure 5 should be used. In this case, since the output voltage is in excess of the reference voltage, the reference voltage is applied direct to the non-inverting input, while the output voltage is divided down before applying to the inverting input. The equation for calculating the output voltage is then:

$$V_{out} = V_{ref} \cdot \frac{R_1 + R_2}{R_2}$$

The remainder of table 3, from +9 V onwards gives suitable values for R1 and R2. Here again the values are somewhat odd, so the use of preferred value resistors and a preset potentiometer is recommended. Note that for output voltages in excess of +37 V an external high-voltage transistor must be used as the output device, which will be described later.

### Higher output currents

The output current capability of the

723 can easily be increased by the addition of an external power transistor, which is controlled by the 723 and carries the bulk of the load current.

Figure 6 shows the circuit of a regulator designed to provide 15 V at up to 2 A. Compared with the circuit of figure 5, no additional components are required apart from the 2N3055 power transistor. The value of R<sub>S</sub> is 0.33 Ω, which is suitable for the maximum current of 2 A. Comparing the circuit of figure 6 with the internal circuit of the IC it is apparent that all that has been done is to connect an additional emitter follower with a higher current capacity than the internal transistors in the IC. The maximum output current that can be obtained by this method depends on the gain of the external transistor and the base current drive available from the IC (not forgetting the maximum current and power ratings of the external transistor). By using high gain power Darlington's such as the TIP 140 output currents of up to 10 A can be achieved. For smaller currents (up to 1 A) a BD 241 or similar is sufficient. The external transistor must, of course, be provided with an adequate heatsink.

The output current may also be increased by the addition of an external PNP transistor, as in the circuit of figure 7, which will provide an output of 5 V at up to 1 A. The line and load regulation of this circuit are very good. An input voltage variation of about 3 V will produce an output voltage variation of only 0.5 mV.

Output current variations of between zero and full load (1 A) will cause an output voltage variation of 5 mV max. This demonstrates the excellent stabilising properties of the 723.

The circuit of figure 8, which is a 12 V 1 A regulator, will give similar results. A PNP power transistor (type BD 242) is used here also.

### Negative voltage regulator

The 723 can also be used in situations requiring a negative output voltage. Because the voltages are in the opposite sense to a positive regulator (i.e. negative) the reference voltage must be fed to the inverting input of the regulator, and the output voltage must be fed back

to the non-inverting input, which is the reverse of the positive regulator situation. In the circuit of figure 9, which is a -15 V regulator the reference voltage is halved by R3/R4 and fed to the inverting input. The output voltage is fed back to the non-inverting input via the potential divider R1/P/R2. Note that the power supply for the IC itself is derived from the regulated output, the positive and negative supply pins being connected to +0 and -15 V respectively. The unregulated negative input is applied only to the collector of the external series transistor (BD242).

The output voltage of this circuit is given by

$$V_{out} = \frac{V_{ref}}{2} \cdot \frac{R_1 + R_2}{R_1}$$

providing R3 = R4.

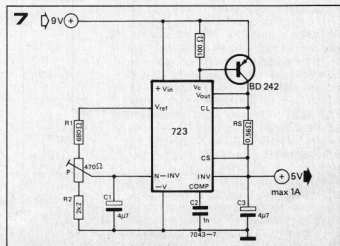
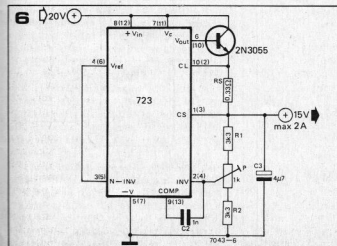
If the potentiometer were not used then rather odd values for R1 and R2 would result, so the use of the nearest preferred values for R1 and R2 is recommended, with a preset potentiometer to provide the final adjustment. For the -15 V regulator shown suitable values would be: R1 = 1k2, R2 = 4k3, P = 500 Ω.

The disadvantage of this circuit is that current limitation by means of R<sub>S</sub> is not possible, as the current limit transistors in the IC are the wrong polarity, so in the case of an overload the external power transistor will fail. Note also the polarity of C1 and C3 (positive terminal to ground) when assembling this circuit.

### High output voltages

In any of the modes described the maximum stabilized output voltage of the 723 is about 37 V (since the maximum input is 40 V). In all these cases, however, one supply pin of the IC is always connected to ground. It is possible to stabilize appreciably higher voltages by operating the IC as a 'floating regulator' (i.e. no direct ground connection to the IC) provided steps are taken to ensure that none of the voltages across the IC exceed the maximum ratings.

In the circuit of figure 10 this is achieved by the use of a zener diode D1 and series resistor R5. This limits the IC supply voltage to 12 V (though the



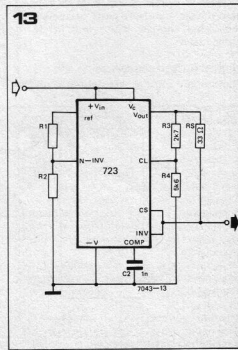
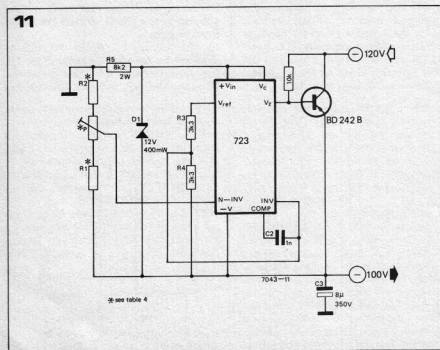
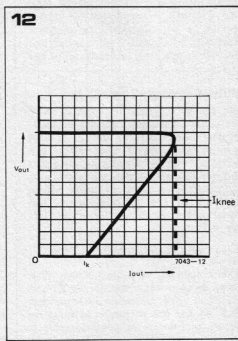
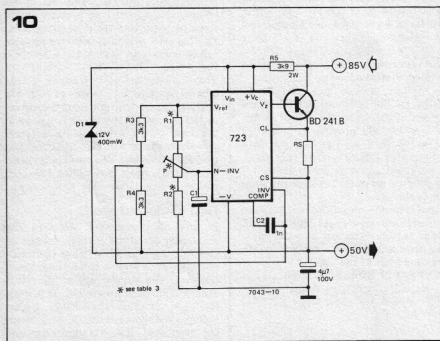
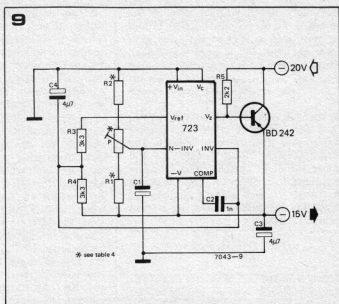
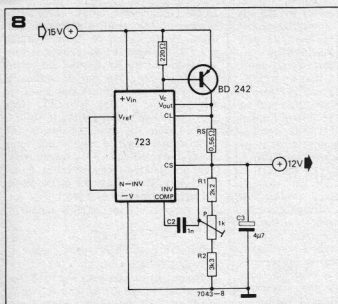


Table 4. NEGATIVE OUTPUT VOLTAGES.

Output (V)	fixed output voltage		output variable $\pm 10\%$			refers to figures
	R1	R2	R1	P	R2	
-6	3.57	2.43	1.2	0.5	.75	9
-9	3.48	5.36	1.2	0.5	2.0	9
-12	3.57	8.45	1.2	0.5	3.3	9
-15	3.65	11.5	1.2	0.5	4.3	9
-28	3.57	24.3	1.2	0.5	10	9
-45	3.57	41.2	2.2	10	33	11
-100	3.57	97.6	2.2	10	91	11
-250	3.57	249	2.2	10	240	11

all resistance values in  $k\Omega$ 

negative supply pin is floating at +5 V with respect to ground). It should be noted that the dissipation in R5 is quite high, and so a 2 W type was chosen in this instance.

The output voltage of this circuit is given by:

$$V_{out} = \frac{V_{ref} \cdot R_2 - R_1}{2 \cdot R_1}$$

provided  $R_3 = R_4$ .

The same principle may also be applied to obtain higher negative output voltages. In this case the circuit of figure 11 applies. Here again the supply voltage across the IC has been limited to 12 V by a zener diode D1 and series resistor R5.

The stabilized output voltage of this circuit is given by:

$$V_{out} = \frac{V_{ref} \cdot R_1 + R_2}{2 \cdot R_1}$$

provided  $R_3 = R_4$ .

12 V is the lowest supply voltage for the IC, but there is no reason why any voltage between 12 and 36 volts should not be used, by suitable choice of zener and series resistor.

### Foldback current limiting

When the current limit is used the voltage regulator becomes a constant current regulator at its limit point. When the maximum current is reached the current remains constant. Any further reduction in the load resistance simply causes a drop in output voltage, until in the short circuit condition there is no voltage drop across the load. The whole, unregulated input voltage is then dropped across the regulator. In this condition the dissipation in the regulator can become excessive, being the unregulated input voltage multiplied by the short circuit current.

A much better system is foldback current limiting, the characteristic of which is shown in figure 12. When the load current reaches the preset maximum it does not remain constant as the load resistance decreases, but actually reduces, until with a short circuit the

Table 4. Values of potential divider resistors R1 and R2 for various negative output voltages.

Figure 8. A 12 V 1 A supply using an external PNP power transistor.

Figure 9. Using the 723 as a negative voltage regulator.

Figure 10. The 723 can be used as a floating regulator to stabilize voltages in excess of +37 V.

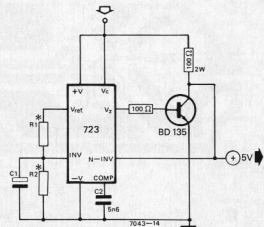
Figure 11. The 723 may also be used as a negative floating regulator.

Figure 12. Foldback current limiting has advantages over a simple current limit. The limit current decreases as the load resistance is reduced, so short-circuit dissipation in the regulator is minimised.

Figure 13. Basic circuit for foldback current limiting.

Figure 14. The 723 used as a shunt regulator.

14



\* see table 3

current is only a small fraction of the full load current. This obviously greatly reduces dissipation in the regulator. When the overload is removed the output voltage returns to its (regulated) value.

The 723 may be used to provide foldback current limiting, and a circuit example is given in figure 13. This circuit is designed for an output voltage of 5 V and a knee current of 50 mA, when the short-circuit current will be about 20 mA. The circuit parameters may be calculated using the following equations:

$$I_{knee} = \frac{V_{out} \cdot R_3 + V_{sense} \cdot (R_3 + R_4)}{R_5 \cdot R_4}$$

$$I_{short\ circuit} = \frac{V_{sense} \cdot R_3 + R_4}{R_5 \cdot R_4}$$

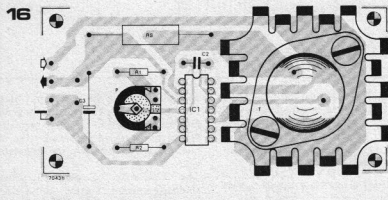
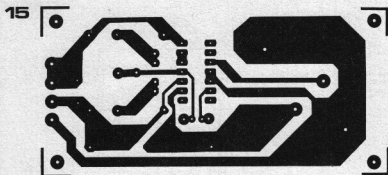
where  $V_{sense}$  is the voltage drop across  $R_5$ .

### Shunt Regulator

In all the examples so far given the regulator (or the external power transistor) has been in series with the load. In the case of a shunt regulator the power transistor is in parallel with the load. If the load current tends to decrease and the regulated output voltage thus tends to rise the power transistor turns on harder and draws more current, and vice versa. The net current drawn by the load/transistor combination is thus always constant.

An example of a shunt regulator is given in figure 14. With the component values given the output voltage variation will be less than 1.5 mV for load variations of 100 mA. No current limit is required with this type of regulator as the short circuit current is limited by the 100  $\Omega$  resistor in series with the unregulated input. The disadvantage of this type of regulator is that maximum power is always drawn from the supply (since the current is constant). Therefore, when the load current is zero the total output power (output current x output voltage) is dissipated in the shunt transistor, which thus requires an adequate heatsink.





### Printed circuit board

The most useful applications of the 723 lie in the range +7 to +36 V, so a printed circuit board layout for these applications is given in figures 15 and 16. The circuit used is that given in figure 6. The component values given for this circuit are for a 15 V output, but component values for other voltages can easily be found using table 3 or the equations previously given.

When building and using this circuit the following points should be noted:

- the unregulated input voltage should be at least 3 V higher than the required output voltage for proper regulation, bearing in mind the absolute maximum of 40 V. Remember, however that the greater the voltage drop across the regulator, the greater the dissipation in the regulator and power transistor.
- R<sub>1</sub>, R<sub>2</sub> and P<sub>1</sub> should be chosen such that the required output voltage should be obtained with P<sub>1</sub> near the middle of its travel, so that positive and negative adjustments of output voltage are possible with P<sub>1</sub> to cater for component tolerances and variations in V<sub>ref</sub>. The current through the potential divider should not exceed 5 mA. Figure 17 illustrates these points.
- R<sub>S</sub> is chosen so that the voltage drop across it is about 0.6 V at the required maximum current

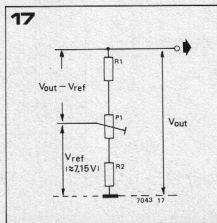
$$i.e. \quad R_S = \frac{0.6}{I_{sc}} (\Omega, V, A)$$

- The maximum output current that can be obtained from this circuit depends on the gain (h<sub>FE</sub>) of the external power transistor. As a rule

Figures 15 and 16. Printed circuit board and component layout for a general purpose +7 to +37 V regulator (EPS 7043b).

Figure 17. R<sub>1</sub>, R<sub>2</sub> and P<sub>1</sub> should be chosen so that the required output voltage is obtained with P<sub>1</sub> near the centre of its travel.

of thumb the maximum current is the product of the transistor gain and the maximum output current (150 mA) of the 723.



# THE MISSING LINK!

Modifications to  
Additions to  
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### BC516/BC517

Some readers have experienced difficulty in obtaining the BC516/517 Darlington transistors used in various Elektor projects. This is due to the fact that these devices are manufactured by Texas Instruments GmbH and must be imported, resulting in delivery delays. It is perfectly permissible to use Darlington pairs made of discrete transistors in these applications, (see figure 1). The main specifications of the BC516 and 517 are listed below.

#### BC516 maximum ratings:

V <sub>cb</sub>	+40 V
I <sub>c</sub>	+400 mA
P <sub>tot</sub>	625 mW
h <sub>FE</sub> (min)	30,000

#### BC517 maximum ratings:

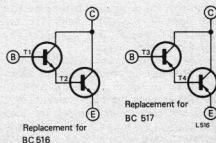
V <sub>cb</sub>	-40 V
I <sub>c</sub>	-400 mA
P <sub>tot</sub>	625 mW
h <sub>FE</sub> (min)	30,000

When choosing transistors for the Darlington pair remember that the second transistor of the pair passes most of the current and dissipates most of the power, and so should meet the rating of the BC516 or 517 in this respect.

The first transistor merely acts as an 'h<sub>FE</sub> multiplier'. Both transistors must meet the voltage rating of the BC516 or 517, and the product of the gains of the two devices should at least equal 30,000.

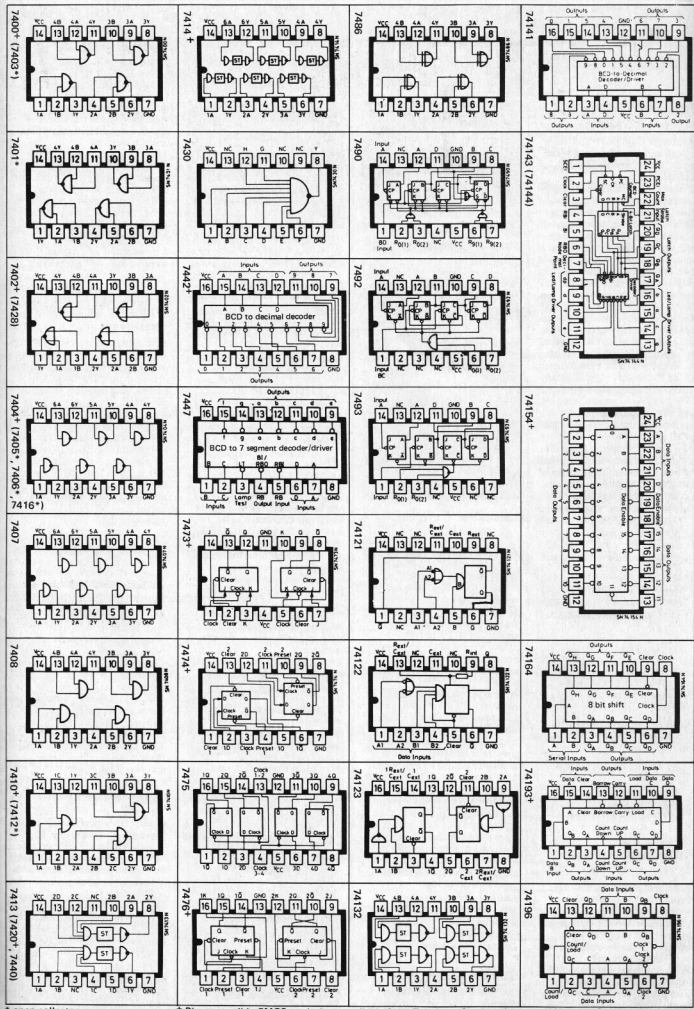
For applications where the maximum dissipation does not exceed 300 mW and the collector-base voltage does not exceed 35 V then the Ferranti ZTX... range of devices may be used. These have the advantage that the E-line package used is very compact.

For T<sub>1</sub> the ZTX107 or ZTX301 to 304 would be suitable; for T<sub>2</sub> the ZTX301 to 304; for T<sub>3</sub> and T<sub>4</sub> the ZTX501 to 504.



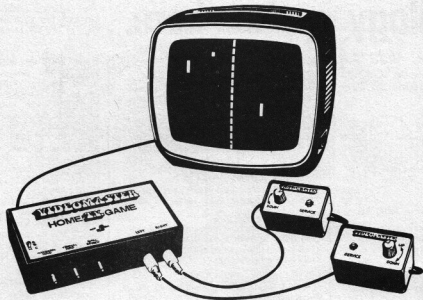
Replacement for BC516

Replacement for BC517



\* open collector

+ Pin-compatible CMOS equivalents available from Teledyne Semiconductor and National Semiconductor



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