up-to-date electronics for lab and leisure

elektor 8

JAN

S		4	11	18	25
M		5	12	19	26
T		6	13	20	27
W		7	14	21	28
T	1	8	15	22	29
F	2	9	16	23	30
S	3	10	17	24	31

FEB

S	1	8	15	22	29
M	2	9	16	23	
T	3	10	17	24	
W	4	11	18	25	
T	5	12	19	26	
F	6	13	20	27	
S	7	14	21	28	

MAR

S		7	14	21	28
M	1	8	15	22	29
T	2	9	16	23	30
W	3	10	17	24	31
T	4	11	18	25	
F	5	12	19	26	
S	6	13	20	27	

APR

S		4	11	18	25
M		5	12	19	26
T		6	13	20	27
W		7	14	21	28
T	1	8	15	22	29
F	2	9	16	23	30
S	3	10	17	24	

MAY

S		2	9	16	23	30
M		3	10	17	24	31
T		4	11	18	25	
W		5	12	19	26	
T		6	13	20	27	
F		7	14	21	28	
S	1	8	15	22	29	

JUN

S		6	13	20	27
M		7	14	21	28
T	1	8	15	22	29
W	2	9	16	23	30
T	3	10	17	24	
F	4	11	18	25	
S	5	12	19	26	

JUL

S		4	11	18	25
M		5	12	19	26
T		6	13	20	27
W		7	14	21	28
T	1	8	15	22	29
F	2	9	16	23	30
S	3	10	17	24	31

AUG

S	1	8	15	22	29
M	2	9	16	23	30
T	3	10	17	24	31
W	4	11	18	25	
T	5	12	19	26	
F	6	13	20	27	
S	7	14	21	28	

SEP

S		5	12	19	26
M		6	13	20	27
T		7	14	21	28
W	1	8	15	22	29
T	2	9	16	23	30
F	3	10	17	24	
S	4	11	18	25	

OCT

S		3	10	17	24	31
M		4	11	18	25	
T		5	12	19	26	
W		6	13	20	27	
T		7	14	21	28	
F	1	8	15	22	29	
S	2	9	16	23	30	

NOV

S		7	14	21	28
M	1	8	15	22	29
T	2	9	16	23	30
W	3	10	17	24	
T	4	11	18	25	
F	5	12	19	26	
S	6	13	20	27	

DEC

S		5	12	19	26
M		6	13	20	27
T		7	14	21	28
W	1	8	15	22	29
T	2	9	16	23	30
F	3	10	17	24	31
S	4	11	18	25	

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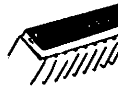

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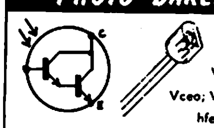

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enables

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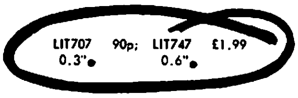
0.3" ● 0.6" ●



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Pins	8	14	16	24	28	36	40	8	10
● Price	13p	15p	15p	26p	30p	39p	44p	31p	35p

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DL721 gives ± 1.9
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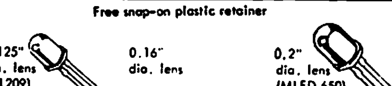
Suitable for Clocks; Instruments; T.V. Channel Indicator
Our Price £4.75 each. ●

L.E.D.'s

Free snap-on plastic retainer



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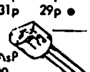
Green	27p	24p	22p ●	33p	30p	27p ●	30p	27p	25p ●
Orange	27p	24p	22p ●	33p	30p	27p ●	30p	27p	25p ●
Yellow	34p	31p	29p ●	35p	32p	29p ●	35p	33p	30p ●



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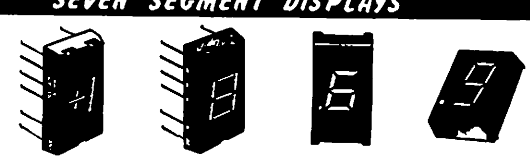
Xciton
Monsanto



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	RED	MAN71	MAN72	MAN73	MAN74	£1.82 ●
	YELLOW	MAN81	MAN82	MAN83	MAN84	£1.82 ●
	ORANGE	MAN3610	MAN3620	MAN3630	MAN3640	£1.82 ●
	GREEN	XAN51	XAN52	-	XAN54	£1.49 ●
	RED	XAN71	XAN72	-	XAN74	£1.49 ●
	YELLOW	XAN81	XAN82	-	XAN84	£1.49 ●
0.4"	GREEN	MAN4510	MAN4520	MAN4530	MAN4540	£2.32 ●
	RED	MAN4710	MAN4720	MAN4730	MAN4740	£2.32 ●
	YELLOW	MAN4810	MAN4820	MAN4830	MAN4840	£2.32 ●
	ORANGE	MAN4610	MAN4620	MAN4630	MAN4640	£2.32 ●
		C.A. L/H Dec. Pt.	C.A. ± 1	C.C. L/H Dec. Pt.	C.C. ± 1	
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austereo control amplifier	HB13	5	1.50	(25)
austereo disc preamp	HB14	5	0.65	(25)
universal frequency reference	HD4	5	1.10	(8)
distortion meter	1437	1	1.65	(8)
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tap sensor	1457	1	0.60	(8)
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minidrum mixer/preamp	1465B	2	0.55	(25)
minidrum noise	1465C	2	1.05	(25)
miniature amplifier	1486	6	0.55	(25)
light dimmer	1487	6	0.45	(8)
beetle	1492	4	2.20	(8)
equa amplifier	1499	1	1.20	(25)
electronic loudspeaker	1527	2	0.50	(25)
mostap	1540	2	1.05	(8)
car power supply	1563	4	1.25	(8)
digital rev counter (control p.c.b. only!)	1590	1	0.55	(8)
car anti-theft alarm	1592	4	1.40	(8)
mos clock 5314 clock circuit	1607A	1	1.15	(8)
mos clock 5314 display board	1607B	1	0.85	(8)
mos clock timebase	1620	4	0.70	(8)
minidrum tap	1621A	2	0.70	(25)
minidrum ruffle circuit	1621B	3	1.10	(25)
automatic bassdrum	1621C	3	0.55	(25)
tap preamp front panels:				
power	1626A	7	1.55	(25)
input	1626B	4	1.55	(25)
volume	1626C	4	1.55	(25)
tone	1626D	4	1.55	(25)
width	1626E	4	1.55	(25)
microdrum	1661	2	0.95	(25)
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clamant clock, time signal	4015-16	7	0.85	(8)
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twin led display	4029-2	2	1.40	(8)
twin decade counter	4029-3	2	1.40	(8)
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NEW:

circuit	number	issue	price	% VAT
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* with solder mask

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Volume 1 — number 8

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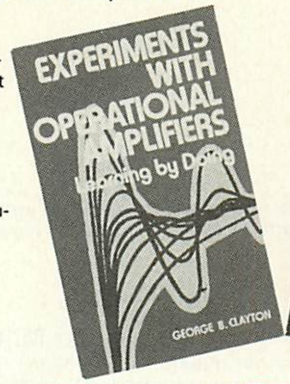

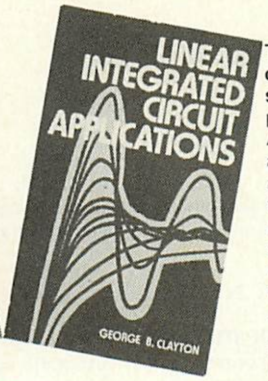

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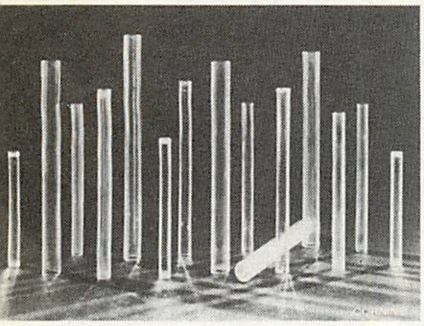
Sapphire arc tube increases efficiency of new HPSV lamps

A single-crystal sapphire material manufactured by Corning for arc tubes in high pressure sodium vapor lamps increases luminous efficacy of such lamps by as much as 5 to 10 percent.
The improved efficiency of the new Corstar sapphire arc tube over conventional polycrystalline arc tubes is a result of the mono-crystalline material's extreme purity and increased transparency.
Thus, high-pressure sodium vapor lamps made with Corstar arc tubes can be designed to produce more lumens per watt from the same energy input, or to produce the same amount of light with less energy.



Characterized by the golden color of the light they produce, high-pressure sodium vapor lamps are coming into increased use for street lighting. Corning's major customer for Corstar arc tubes is currently involved in supplying the lamps for the extensive street relighting program in New York City.
The arc tube is the key component in a high-pressure sodium vapor lamp because it must have the dimensional stability, corrosion resistance and temperature capability to contain a high-temperature discharge of metallic sodium.
The Corstar arc tubes will operate at temperatures in excess of 1200 degrees C, while maintaining superior resistance to the corrosive attack of high-temperature sodium under pressure. Corstar arc tubes have a rated life of over 20,000 hours.

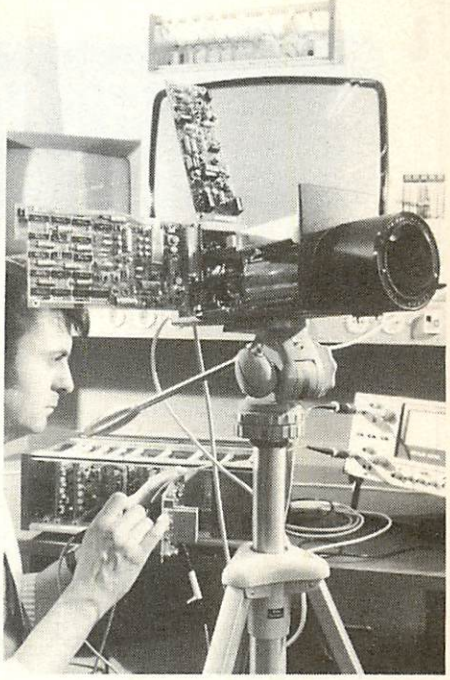
BBC engineers approve 'Thermax' tapes

A small but valuable contribution to the efficiency of the BBC Television service is being made by the Somerset firm, Thermographics Measurements Ltd of Ilchester. This Company's temperature-sensitive tapes are used to take temperature readings in the co-axial feeder cables which connect the transmitters to the aerials in the UHF 625-line system throughout the country.
It is not possible to take satisfactory measurements by inserting thermometers inside the co-axial feeders and, in fact, their presence could upset the operation of the system. What the BBC engineers like particularly about these 'Thermax' tapes is that they are irreversible and, unlike special paints sometimes used for this purpose in the past, they are not subject to change as the exposure time is extended. 'You can go back to a site an hour, a week or a year later and the information you want is there.'
These tapes are also used by BBC staff to make temperature checks on transistors and on other small components and when new types of equipment are introduced.
Available in five temperature ranges between 37°C and 260°C, 'Thermax' tapes indicate temperature changes by a simple colour change from silver-white to black, which is easily observed against the temperature scale marked in red. Through a technical innovation in printing on the tape, a clearer print of the temperature scale has been achieved with the further benefit that it cannot be dissolved or erased.

Thermographics Measurements Ltd., The Square, Ilchester, Yeovil, Somerset

Interplex single-tube colour television camera system

A new single-tube colour camera —Interplex — developed by Siemens, incorporates a tube which gives uniformly high colour rendition of high resolution. The unit consists of a compact camera with a tube and a decoder which converts the colour information into standard PAL television signals.
The Interplex single-tube colour camera uses a new type of dichroic strip filter. In contrast to a normal three-tube camera, the colour distributor used to break down the image arriving from the lens into red, green and blue channels is integrated in the Interplex picture tube. This has made it possible to reduce the size of the camera considerably by dispensing with the accessories for colour coincidence which is so difficult to attain with a three-tube system.
The signal information supplied by the television camera tube in the 4.43 MHz range is converted into standard PAL signals in a decoder with comb filter systems and electronic circuitry. Each frequency spectrum of the black-and-white and colour information is separated by the comb filter and here the spectral lines of the video signals are broken down into colour (chrominance) and luminance information. Additional electronic circuits suppress interference



from repetitive luminance in the chrominance channel (cross-colour suppression), and are also used to suppress interference in the opposite direction (cross luminance suppression). The individual colour signals are processed without loss of information or colour rendition and uniformity, and can be passed on to a receiver as a PAL coded colour signal. The decoder can also be used for horizontal and vertical aperture correction and addition/subtraction of blue, green, red and white colour components (matrixing).
A standardized connection has been established within the Interplex system for the coded colour signal supplied by the tube of the camera (multiplex signal). The single-tube colour camera can be fitted with an antimony trisulphite coated tube (Vidicon with integral filter type XQ 1360) or a silicon tube (Interplex-vidicon type XQ 1365). The silicon tube developed by Siemens is very sensitive to light and has a low intertia and a linear characteristic.
A resolution of approx. 6 MHz can be achieved in red-green-blue-operation. Complete resolution is possible in PAL operation.
The multiplex signal produced by the camera is compatible and can also be shown on a black-and-white set. Several cameras can be operated in sequence using the standardized connection, the decoder and a selector switch. The multiplex signal can be recorded directly on polychromatic video recorders so that the decoder is only required for reproduction. Using the new camera it is also possible to set up colour television units that are no larger than black-and-white television units.

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?eading between the lines

elevision viewers throughout Britain re to be offered a remarkable new ervice – stop-press news flashed on to eir screens at the flick of a switch. A nall adaptor on a standard existing set ill offer the choice of up-to-the-minute ews ranging from, say, what won the .30 race to the current price of gold. lready launched by the BBC (British roadcasting Corporation), the Inde- endent Broadcasting Authority (IBA) ill join in next year.
he BBC's new device, CEEFAX (See acts) has been operating since autumn 974 from the Television Centre, ondon, under editor Colin McIntyre. It as been providing viewers with a video ervice of printed material of up to 00 pages, each page consisting of over 0 lines of electronic type.

ndex

he viewer can punch up an Index page n his screen and then choose which ind of information he wants to have – ews headlines, horse-racing results, ports news, share or commodity prices, eather, road condition report, airport formation or the timetable of the ay's radio and television programmes. e makes his own choice of what he ants and when he wants it – all the formation is stored in CEEFAX's emory and kept up to date by the ditor and his staff in London. When e viewer punches up the page number equired it will appear within 15 sec- nds – less time than it takes to make a elephone connection.
he IBA has developed a similar device hich it has named ORACLE (Optional eception of Announcements by Coded ine Electronics) and this will begin a val service for viewers soon. Both aim t giving the viewer new and instant ccess to useful and necessary facts rom the price of sugar to the starting ime of a play or film. The new services re national but could in time provide ocal neighbourhood information as ell.

lanking Interval

he CEEFAX and ORACLE devices xploit a potential in the television creen which has been known about for early 40 years. There is a section of the ne system which is unused by the ormal television transmission, a group f 8 lines within the 625 line screen hich engineers call the 'field blanking nterval'.
y using two of them it is possible to end out a signal which remains invisible n all receivers except those fitted with special decoding device and with the ddition of a small contraption a normal eceiver can be adapted to decode up to 00 pages of printed material sent out through the ordinary television transmitters.
To provide this material costs the BBC very little. A small staff – only half a dozen – will shortly be assembled and organised into a mini-newsroom, where the various information services will be compiled, 'subbed', typed out at frequent intervals and stored in a small electronic 'memory' from which the viewer will be able to choose whichever sections he wishes. The capital equipment required at the end of the operation should not cost more than £ 50,000 in all – about the cost of equipping a very small local radio station.
When manufacturers decide to mass produce the equipment, the viewer should be able to adapt his receiver for an extra £ 200-£ 300. A full-size colour receiver with a built-in CEEFAX and ORACLE device will cost £ 600-£ 800 and a black-and-white receiver under £ 200.

Prototypes

However, for the moment, the only CEEFAX devices available are specially made jobs which cost about £ 800. The total number of subscribers at present is still well under two figures, a select consumer privilege enjoyed by those involved in the current experiment. But even now there is nothing to prevent anyone from building his own decoder, if he is familiar with basic television engineering.
Some time in early 1975 the IBA's ORACLE system should also begin transmitting and ITN (Independent Television News) is actively thinking up an elaborate set of services which it could provide on behalf of the two London programme companies (Thames Television and London Weekend Television) which will inaugurate the service. ITN sees ORACLE's services as a suitable supplement to its present output and could give ITV viewers a feed of the day's sporting results as well as headlines, newsflashes, weather reports and information about cinemas, theatres, concerts and television programmes.

Sports And City News

Racing results and share prices are obviously the type of detailed information constantly changing throughout an average day for which the new devices are ideally suited. The racing results on a busy day would require over 12 'pages' of transmitted material to bring, say, 300 results. A list of the runners on an average day (160-200) would need another four or five pages.
To provide the full range of services which ITV envisages will require in all 50-100 pages and that means exploiting almost the whole of the 'memory' of the present CEEFAX/ORACLE systems.
One area in which the new devices could prove very useful is the City of London. At present London stockbrokers use the four tape services of Extel, Reuters, AP-Dow Jones and the 'Financial Times'. Reuters supplies a special video service of financial news with 22 channels of information. CEEFAX and ORACLE could provide a similar service very cheaply and conveniently on a single screen instead of the ten which some offices must now have.

Maps And Diagrams

The actual mode of transmission is a digital one and it is possible to sub-

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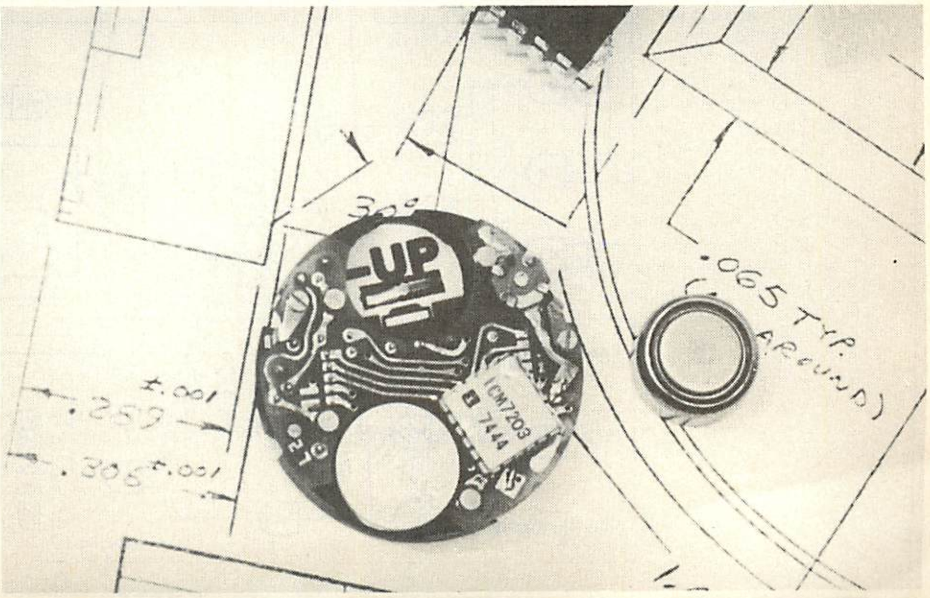
titute small blocks and shapes for the etters of the alphabet and the numerals. Colin McIntyre and his staff can there-ore construct maps and diagrams to ap-ear on the screen, in various colours, as vell as ordinary writing in upper and ower case. With the addition of a com-uter, which is shortly to arrive, the usiness of map-display and diagram resentation will be made much easier nd extremely rapid.
he computer's memory will also ex-end the capacity of CEEFAX to make t possible for a 1000-page 'book', as it vere, to be presented on the screen at a ingle viewer selection, each page of the ook replacing the previous one at the ate of one per minute.
Another major use will be to provide ermanent sub-titles for the deaf. CEEFAX print can be made to appear t the bottom of the normal television icture.
he BBC has worked out that it would ake one man about 40 hours to type ut and store the dialogue of a full-ength play arranged to appear on the creen at the appropriate moments. By witching to CEEFAX deaf people ould receive the printed 'soundtrack' f plays and documentaries without poiling the programme for ordinary iewers whose picture would be quite ormal.
Similarly, viewers can have 'newsflashes' uperimposed on their evening's ordi-ary viewing when major news occurs vithout interfering with the viewing of thers who prefer to watch a whole ulletin at a stated time.

New Intersil 24-hour alpha-numeric readout CMOS watch

ntersil recently introduced two ad-litions to its line of CMOS watch and lock circuits and dropped the prices on wo more.
The ICM7203 is a single-chip LED digi-al wristwatch circuit with alphanumeric apability, providing hours, minutes, lay, date and seconds readout. It is a 24-hour version of Intersil's ICM7200 12-hour circuit and is available immedi-ately.
The ICM7204 is a numeric only version of the 7203. It interfaces with existing 7-segment LED displays. It is a 24-hour ariation of Intersil's ICM7202. Delivery s also immediate.
Pricing for the 7203 has been estab-ished at $ 16.70 at the 100-999 quan-ity level. The 7204 is priced at $ 10.80 at the same level. In a related move, Intersil also dropped the prices of its ICM7200 and ICM7202 to comparable levels, $ 16.70 for the 7200 down from $ 29.20, and $ 10.80 for the 7202 down from $ 22.00.
According to Intersil, no other presently available 24-hour LED watch circuit contains both digit and segment drivers on-chip. Other devices use external tran-sistors for drivers. Intersil LED watch units are totally integrated on one chip, including segment and digit output buffer circuits. This allows OEM watch and clock manufacturers to produce very compact movements without use of multiple-chip assembly techniques.
Both circuits are supplied in 24-pin cer-amic leadless packages, 0.335 inches square, designed to be easily soldered onto PC boards.
According to Intersil, watches made from these circuits are simple to oper-ate, the only LED timepieces offering the utility of a full calendar feature simi-lar to that used in conventional watches.
One button – called the 'command' button – when pushed once displays the time, twice the day-date, and three times the seconds. (At second push, the ICM7204 displays date only, while the ICM7203 displays both day and date.)
The two new circuits also greatly sim-plify watch setting. A second button, which can be recessed in the case to pre-vent accidental activation, cycles the setting modes: one push for date set; two for hour set; three for day set; four for minutes; and five pushes for seconds.
In each set mode, the command button advances the watch display. Hours, for instance, advance by one each time the command button is pressed. Seconds are reset to zero by the command button.
All set modes are independent of each other, allowing hours to be advanced past midnight without affecting day or date – important when travelling be-tween time zones.
Both circuits operate at 32.768 kHz. Two parts, a 32.768 kHz quartz crystal and one trimming capacitor, complete the oscillator circuit. Current required is 4 microamperes, and the oscillator is de-scribed by Intersil as ultra-stable.
The circuits have provisions for light sensors which increase the brightness of the display at high ambient light levels. To conserve battery life, however, only time and day-date can be displayed at low and high brightness. Seconds and set modes are always displayed at low brightness.
The ICM7204 interfaces directly with a multiplexed sevent segment/four-digit-plus-colon common cathode LED dis-play, while the ICM7203 requires a nine segment display.
The circuits are powered by two silver-oxide batteries and typically require 6 milliamperes per segment at 25% duty cycle with seven segments on. With high-efficiency magnified LEDs, this amount of current gives a very bright display, the manufacturer states.
According to Intersil the technology that went into the ICM7200 family was gained directly from their experience developing the ICM7045 single-chip stopwatch microcircuit two years ago. This was the first such device to use ion implanted metal gate CMOS and direct drive of LEDs. It contains 4 modes of user-selected stopwatch functions as well as a full 24-hour clock. In designing it, Intersil had to include a standard mode; a sequential mode to time multi-legged events without restarting the timer at the beginning of each lap; a split mode to clock a complete event while displaying the times of each pro-gressive lap, and an event mode to time a complete event with intermediate interruptions. The circuit building tech-niques included use of computerized cir-cuit simulation to insure worst case operation over full temperature ranges. 'Once we had mastered the problems in-volved with the ICM7045, development of the ICM7200 family of circuits was relatively straightforward.'



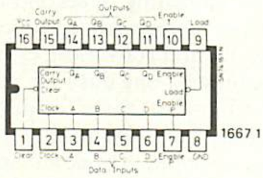
W.G. Paans

calendar

Many mechanical and electro-mechanical clocks and watches a now provided with date indicatio Addition of a calendar to an elec tronic digital clock is a fairly simple matter, and the circuit given here gives the month as wel as the date.

As the calendar is an addition to a digital clock a control signal must be derived from the clock to change the date. This can be derived from the changeover from 23.59 to 00.00 with a 24-hour clock, or if used with a 12-hour clock the changeover from 11.59 to 12.00 may be used. However, since this occurs every 12 hours a ÷ 2 flip-flop must be inserted between clock and calendar to give a pulse once every 24 hours.
Like all the best calendars, this calendar knows whether the last day of the month falls on the 28th (February), the 30th or the 31st. Those who are worried about the 29th of February can add the optional leap-year correction circuit, in which case the calendar will not need to be reset until the year 2100, when a century correction (omission of leap-year) becomes necessary.
The calendar is simply a logical extension of the hours, minutes and seconds counters in the clock, but counting days and months instead. The resetting functions are, of course, considerably mo complicated due to the differing nu ber of days in each month. Since t year begins with the first month, a each month begins with the first day, is not possible to use simple deca counters such as the 7490, which can reset to zero. Instead, presettab counters must be used, so that they c be preset to one at the beginning of t year or month. A suitable choice is t 74163, which is a four-bit bina counter with synchronous preset a clear. Two of these counters make the days and tens of days counter, a as the capacity of the 74163 is 4 b one of these IC's will suffice for t

1



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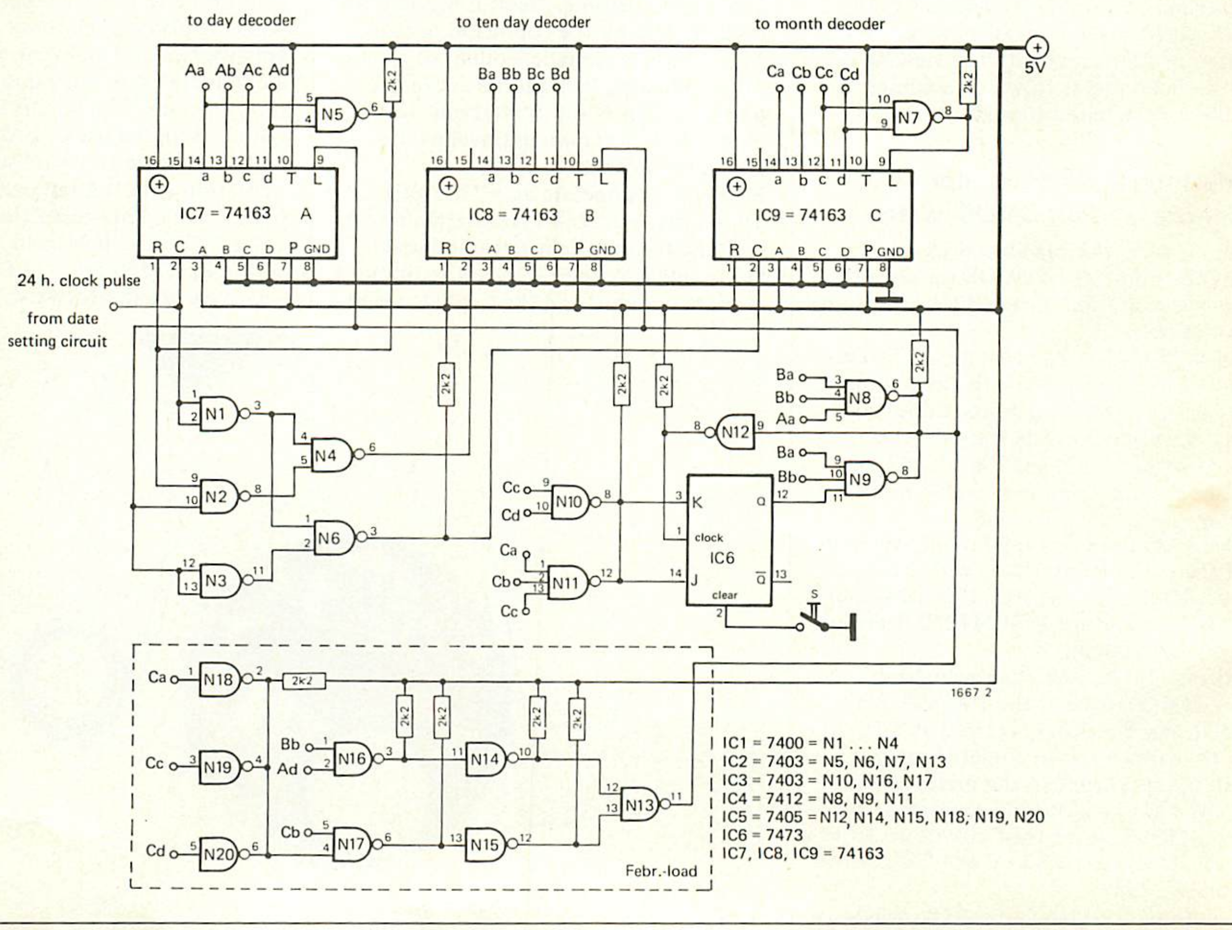

nonths counter. The pin configuration f the 74163 is given in figure 1. Points o watch with this IC are:
) unlike the 7490 it counts on a positive-going edge of the input waveform.
) for resetting purposes a logic '0' is required.
i) counting may only take place when there is a '1' at both the enable inputs P and T.
/) when there is a '0' at the load input the count function is inhibited. The next positive-going transition of the clock input transfers information from the data inputs to the outputs.

Counter Circuit

he circuit of the counter section of the alendar is given in figure 2. IC7 counts ne days, IC8 counts tens of days and C9 counts months. The enable inputs f all three counters are permanently connected to positive supply, as are the clear inputs of IC8 and IC9. The data inputs of the three counters must have the correct presetting data hardwired into them. The day counter is preset to 1 at the beginning of each month, so the A input is connected to positive supply and the B, C and D inputs to ground. The tens of days counter is preset to zero so all the data inputs are grounded. The month counter is preset to 1, like the day counter.

IC7 receives one pulse every 24 hours from the digital clock at pin 2 (clock input). This IC is connected so that it normally counts up to 9 before resetting to zero. When the count reaches 9 (binary 1001) the a and d outputs of the counter are high, so the output goes low, taking the synchronous clear input (pin 1) to '0'. On the tenth clock pulse the counter is reset synchronously to zero. This sequence is of course interrupted when the counter is preset to 1 at the beginning of each month.

While the output of N5 is low this also holds pin 9 of N2 low, so its output is high. The tenth clock pulse which resets IC7 can therefore pass through N1 and N4 to the clock input of IC8. IC8 therefore counts once every ten clock pulses. As stated earlier IC7 and IC8 must be preset at the beginning of each month, the count that they reach before this occurs depending on the number of days in the preceding month. It is evident from table 1 that with two exceptions the number of days in the month alternates between 31 and 30. The exceptions are February, which has 28 days, August, which has 31 days after July's 31 and December/January similarly. It is thus possible to indicate the number of days required in each month with a flip-flop whose state is changed each month, the only corrections necessary being a) additional circuitry to detect when the month is February, and b) circuitry to inhibit the changeover of the flip-flop at the July/August and December/January transitions. The flip-flop is IC6, and the 'February detection circuit' is contained in the dotted box. This part of the circuit operates as follows: Assume that the next transition is from a month with 30 days to one with 31 days (say April/May). The Q output of IC6 will initially be high. When the count of IC7 and IC8 reaches 30, outputs Ba and Bb of IC8 will go high. This means that all three inputs of N9 are now high so the output is low, taking the load inputs of IC7 and IC8 to '0'. On the next clock pulse IC7 and IC8 are thus preset. The output of N9 also holds the input of N3 low. The output of N3 is thus high, so the clock pulse is allowed through N6 to the clock input of IC9. Immediately IC7 and IC8 are preset the output of N9 goes high again. The output of N12 thus goes low. This is connected to the clock input of IC6 so the flip-flop changes state and the Q output goes low.

At the end of the next month, since the Q output of IC6 is low the output of N9 must remain high and the transition cannot take place on day 30. Instead N8 takes over, and on day 31, when outputs Ba and Bb and output Aa are all '1', then the output of N8 goes low and the sequence repeats. Inhibition of the

igure 1. Pin configuration of the 74163 used n this design.

igure 2. Basic circuit of the counting section f the calendar.

igures 3 and 4. Two alternative decoding ircuits for the calendar.

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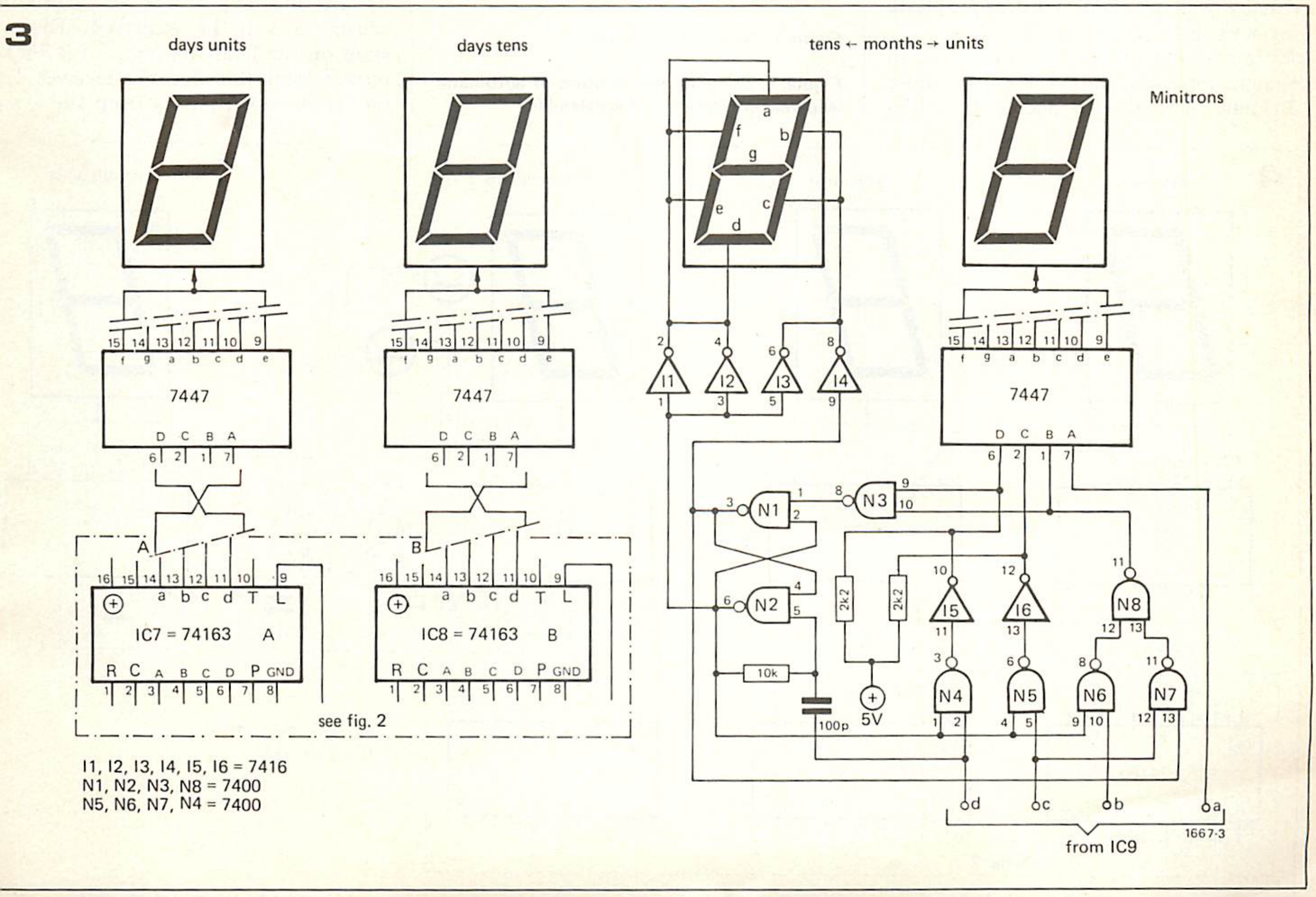

flip-flop changeover during the July/August transition is accomplished by N11. As July is the 7th month (binary 0111) outputs Ca, Cb, and Cc are connected to the inputs of N11. When these are all '1' (during July) the output of N11 is low. This takes the J and K inputs of IC6 low, inhibiting the change of state. N10 performs a similar function during the December/January transition.
The 'February detection circuit' operates as follows: the rather complicated looking array of gates performs the logic function:

$$\text{'February transition'} = Cb \cdot \overline{Ca} \cdot \overline{Cc} \cdot \overline{Cd} \cdot Bb \cdot Ad.$$

Which is to say that the output of N13 goes low when the month is February (binary 0010) and the day is 28 (Ad = 1, Bb = 1).
The only point left to explain in figure 2 is the presetting of the month counter. This is allowed to count up to 12. When the count reaches 12 outputs Cc and Cd are high so the output of N7 holds the load input low. On the next clock pulse the counter is synchronously preset to 1.

Display Decoding

To provide an intelligible display the outputs of the three counters must, of course, be decoded. Two alternative decoding circuits are given, and the choice is up to the constructor. Since the day counters have BCD outputs these are easily decoded, in both figures 3 and 4, using 7447 BCD/seven-segment decoder-drivers. Although the circuits shown use Minitron displays, LED displays may equally well be used (with appropriate segment series resistors).
As the month counter counts to 12 in straight binary decoding is a little more difficult. The month decoding of figure 3 operates as follows:
when the month count is less than 10 the flip-flop comprising N1/N2 is reset and the output of N1 is low. This means that the data from IC9 (connected to inputs a, b, c, d) is allowed through N4/I5, N5/I6 and N6/N8 (data on input a is connected direct to decoder) and is decoded into the months (units) display.
The inputs of I_1, I_2 and I_3 are all connected to the output of N2, which is high, so their outputs are low and the ten month display is '0'. If a leading zero is not required on the ten month display then these inverters may be omitted. When the month count reaches 10 (binary 1010) the output of N3 goes low, setting flip-flop N1/N2. The outputs of I_1, I_2 and I_3 are now high, while the output of I_4 is low, so the ten month display is 1.

Month	Number of days	IC6 Q outputs	IC6 J and K inputs
January	31	0	1
February	28	1	1
March	31	0	1
April	30	1	1
May	31	0	1
June	30	1	1
July	31	0	0
August	31	0	1
September	30	1	1
October	31	0	1
November	30	1	1
December	31	0	0

Table 1. Number of days in each month and the corresponding states of flip-flop IC6.

Figure 5. Date setting circuit.

Figure 6. Showing the addition of automatic leap-year correction to the calendar.

The low output of N2 inhibits the data on the b, c and d inputs from passing through N4, N5 and N6. The high output of N1 allows the data on the c input through N7. During months 10 to 12 therefore inputs C and D of the 7447 are low, the B input receives data from the c output of the counter, while the A input continues to receive 'a' data. During month 10 (binary 1010) the 7447 receives input code 0000 and thus the display is 0. During month 11 (binary 1011) the input of the 7447 is 0001 (display 1) and during month 12 (binary 1100) the input code is 0010 and the display 2. During this period the ten month display is, of course, always 1. At the end of the year, when the month counter is preset back to 1, the d input to the decoder goes low. This transition is differentiated by the 10 k and 100 p on the input of N2, producing a short negative-going pulse that resets the flip-flop.
The month decoding of figure 4 operates on a somewhat different principle. Basically, for counts of less than 10 the months units are decoded by IC2. For counts from 10 to 12 the months units decoding is transferred from IC2 to IC3, while IC2 counts the tens of months. The circuit operates as follows: for month counts below 10 flip-flop N2/N3 is reset, so the output of N2 is low. T1 and T2 are turned off and IC3 is inhibited by a '0' on the blanking input (pin 4). IC2 thus decodes the data from the output of the month counter.
When month 10 is reached the output of N1 goes low, setting the flip-flop and blanking IC2. The display is now driven by T1 and T2, which are turned on causing a 1 to be displayed. The low state on the blanking input of IC3 is removed, and this decoder receives data on its A and B inputs from the a and

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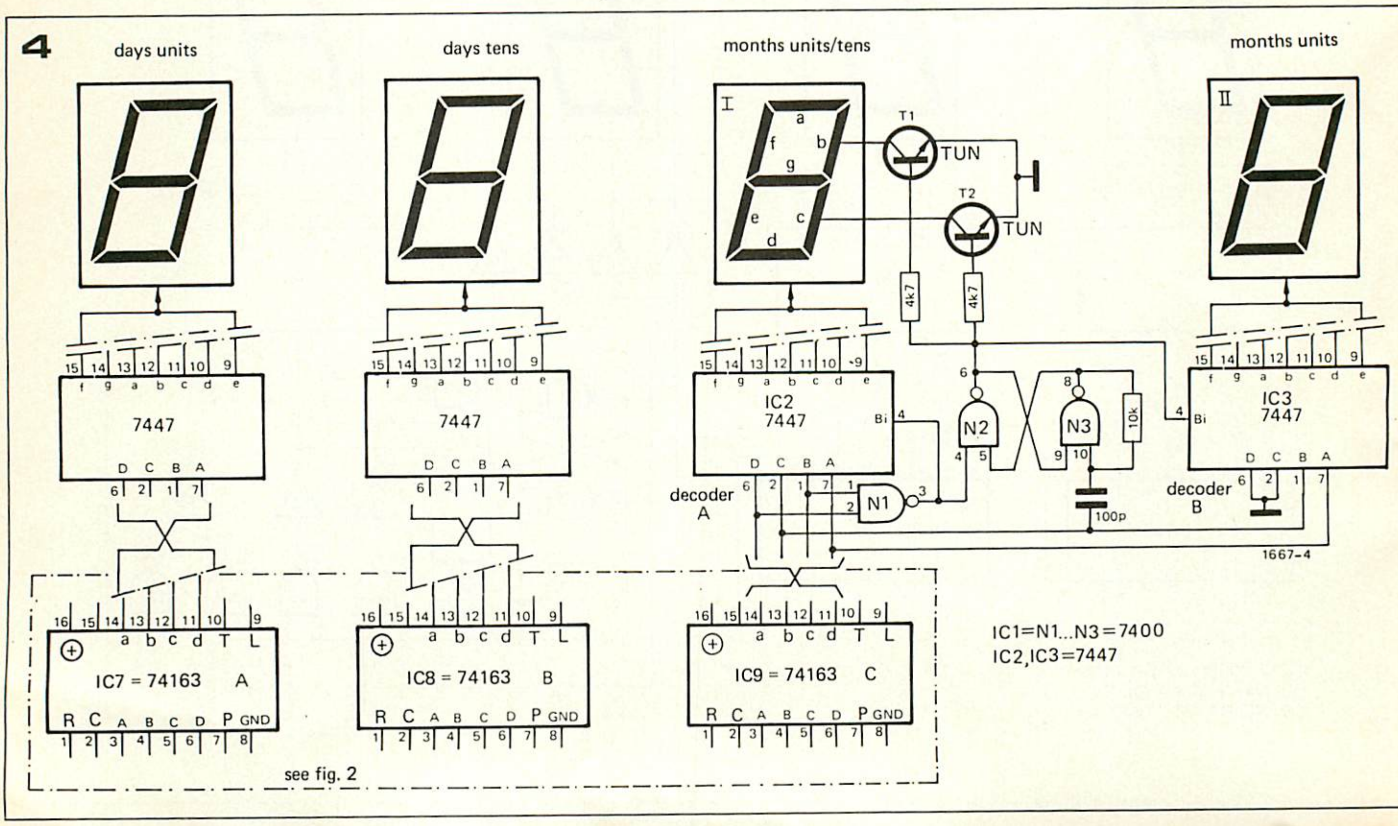

outputs of the counter. Thus for onths 10, 11 and 12 IC3 receives in-ts 0000, 0001 and 0010 respectively. the beginning of the new year the p-flop is reset in a similar fashion to at of figure 3.

ata Setting

is is accomplished by the circuit of ure 5. With S1, S2 and S3 in the pos-on shown the three flip-flops com-sing N4-N9 are reset. The outputs of , N6 and N8 are thus high. One of e inputs of N3 is held low by N5 so its tput is high, and both inputs of N11 e low, so its output is high. Two of e inputs of N10 are high so the 24-ur pulses connected to the other in-t can pass through N10 and N12 to e day counter.

S1 is now changed over flip-p N4/N5 is set blocking the 24-hour ses through N10 and allowing a fast se train from the astable multivi-tor N1/N2 through N3 and N12. This be used for fast setting of the calen- to some value near the required date. S1 is now reset to its original position d S2 is changed over N10 is again cked by a '0' on pin 2. Pin 9 of N11 now high, so the calendar may be vanced slowly to the correct date by gle pulses through N11, produced by ernately setting and resetting flip-p N8/N9 with S3. Flip-flop IC6 must, course, be set to the correct state for e month, according to table 1.

ap Year Correction

e automatic leap-year correction is remely simple, and consists basically a divide-by-four counter that counts e years and gives February an extra y every fourth year. The addition of e leap-year correction to the calendar cuit is shown in figure 6. The counter nsists of two JK flip-flops (IC10). ce a year this counter receives a pulse m output d of the month counter). Normally at least one of the $\overline{Q}$ out-s of IC10 will be low and the base of will be held down via one of the two des connected to these outputs. T1 l thus be turned off. During the rth year both these outputs are high, noving the constraint on the base of . T1 is now turned on and off on ernate days by N21, whose input is nected to output a of IC7. On odd s T1 is off, and on even days T1 is holding pin 12 of N13 low. When 28th of February arrives the 'Febru- detection circuit' will try to operate, since it is an even day T1 is turned and the output of N13 remains high. will not go low until T1 turns off on 29th, and on the next clock pulse day counters are preset.

nclusion

ese circuits should enable the con-uctor to add a calendar to most digi-clocks. The construction and type of plays used are left to the reader's ividual preference, and presumably l be chosen to match the existing ck.

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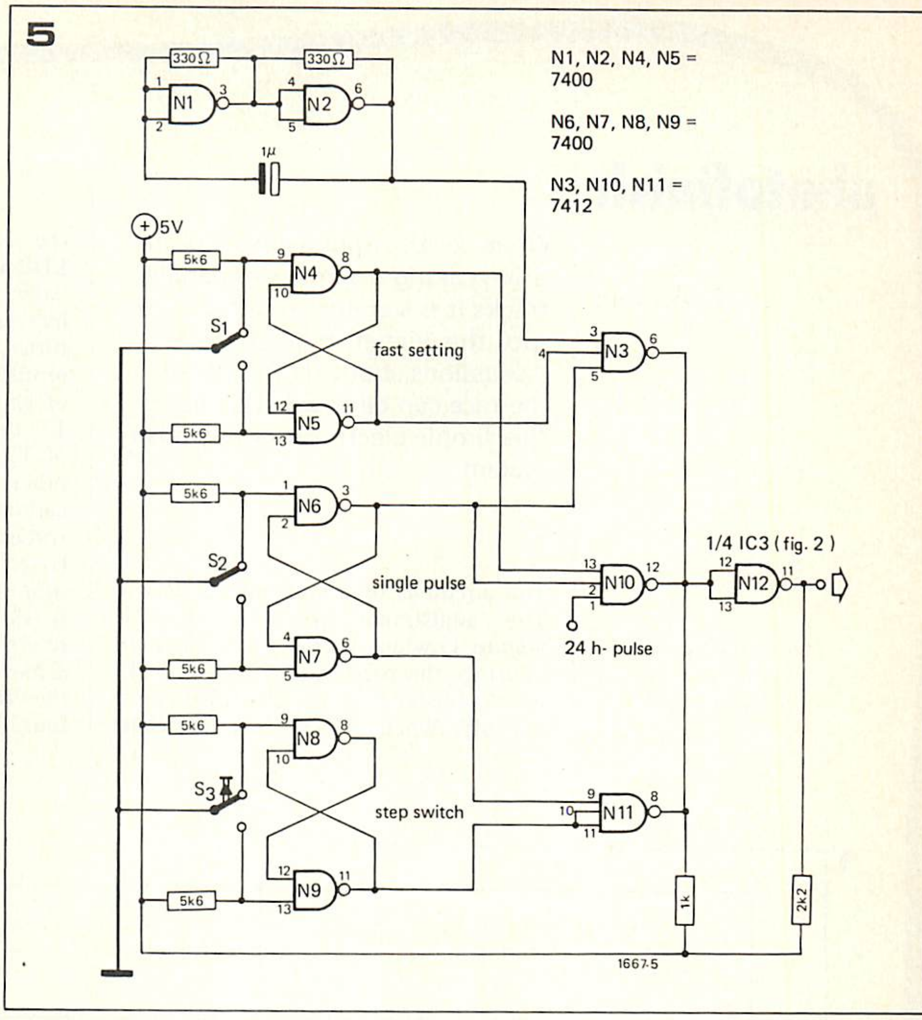

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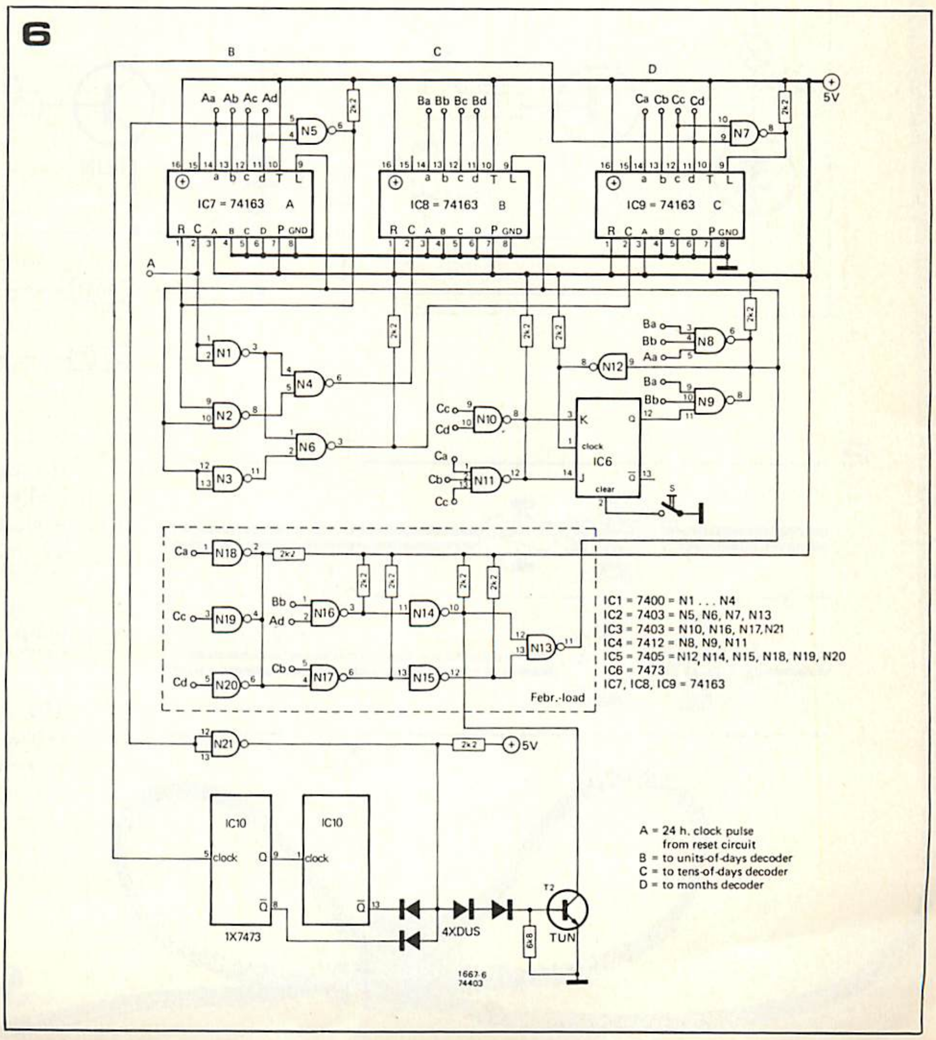

photofinish

F. Ansoms

When several mini racing cars are driven along a number of parallel tracks it is sometimes difficult to spot the winner. Heated discussions about the results of the race can be avoided by using this simple electronic photofinish system.

The circuit is of a quite simple design. The adjustment potentiometer, P1, (figure 1) which together with the LDR controls the base bias of transistor T1 is so adjusted that the transistor is just cut off. When a racing car intercepts the light beam, the resistance of the LDR momentarily increases, so that the base voltage of the transistor also increases, with the result that the latter turns on and lamp L1 lights up. The resulting current causes a voltage drop of about 1 V across resistor R3 so that T3, too, turns on. The collector voltage of T3 is now about 0.3 V, so that the other thyristor cannot fire, since the cathode voltage is higher than the gate voltage. After the final heat, the circuit is reset by briefly interrupting the supply voltage by pushing button S1. If this is often forgotten, automatic resetting after each round can be achieved by fitting a microswitch under the track some distance before the finish line.

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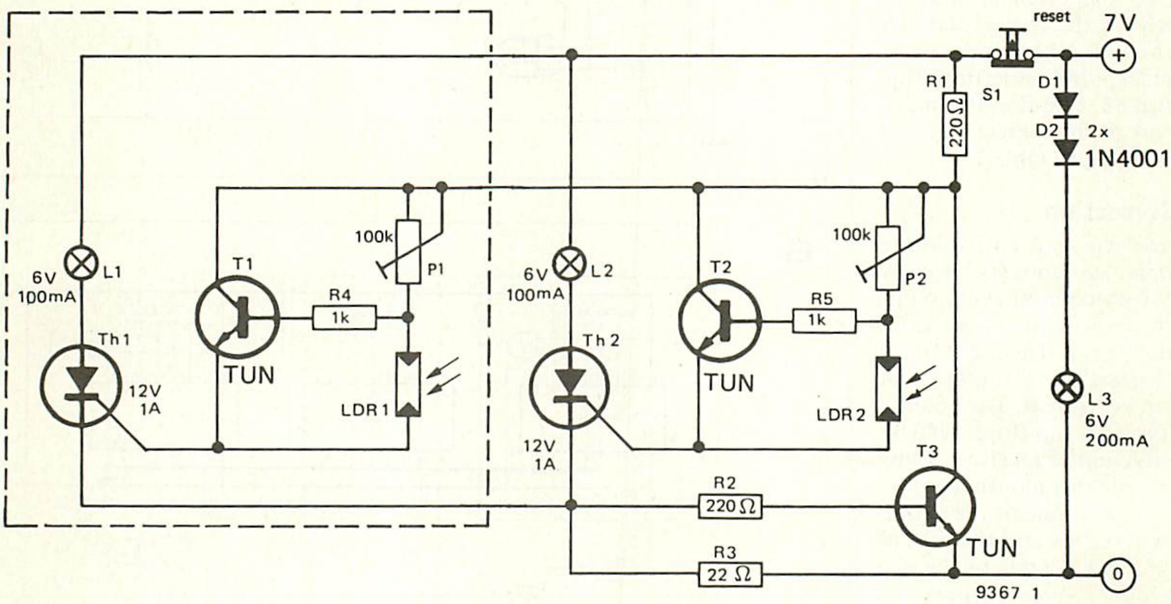

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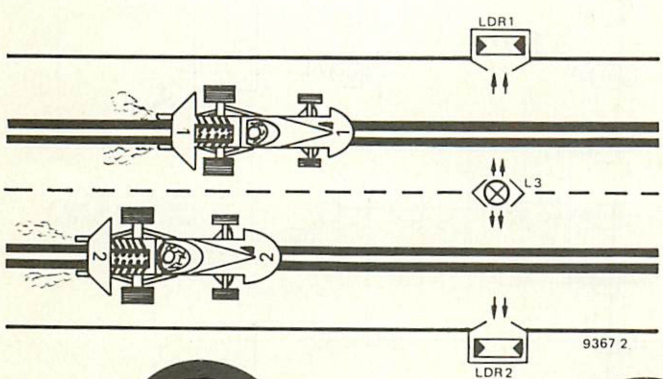

If more than two tracks are used, which makes it more difficult to see who was first, the circuit can easily be extended by parallel connection of the section surrounded by the dashed line. And as a last practical hint: the LDRs and the lamp should be mounted in pieces of PVC tubing. The LDRs are then not influenced by ambient light.
The supply voltage depends on the types of lamp and can be chosen about 1 volt higher than the nominal lamp voltage.

santatronics

l. ter Mijtelen

automatic barrier control for model railway level-crossings

The circuit described here provides control of the 'automatic barrier' type of level crossing (or indeed of the old-fashioned gate type). It gives a realistic simulation of the visual and audible warnings. There is no limit on the train length, and the system will operate when trains are passing in both directions.

igure 1 shows the general principle of peration. In the 'rest' condition the arriers are, of course, open and no ights show. Light dependent resistors LDR1A, 1B, 2A and 2B) are situated y the track some distance on either ide of the crossing, and these normally eceive light from lamps L4 and L5. Vhen a train approaches it will block he light from either LDR1A or 1B, epending on its direction of travel. 'his initiates the following sequence of vents. Firstly amber lights (L1) light or several seconds and a bell sounds. 'hen the amber lamps extinguish and he bell stops, red lights L2 and L3 start o flash alternately and the barriers escend. After the train has passed, (this fact is determined by LDR2A (or 2B) being re-illuminated) then the red lamps are extinguished and the barriers are raised.

Circuit

The most important part of the circuit is the train detection logic given in figures 2 and 3. This ensures that the barriers are lowered as a train approaches, and are not raised again until the train (or trains if there are more than one on the crossing at the same time) have left the crossing. The logic will operate correctly regardless of the length of the train i.e. it makes no difference if the train is either longer or shorter than the distance between LDR1 and LDR2.

The circuit of figure 2 is duplicated for the up and the down line, while figure 3 shows how the two circuits of figure 2 are interconnected. The circuit of figure 2 operates in the following manner: when a train approaches it blocks the light from LDR1, whose resistance thus increases, causing the input of N1 to go high. The output of N1 thus goes low, setting the flip-flop N3/N4 and initiating the gate-closing sequence. Once the flip-flop is set LDR1 has no further effect. When the train

Figure 1. The general layout of lamps, LDRs and barriers.

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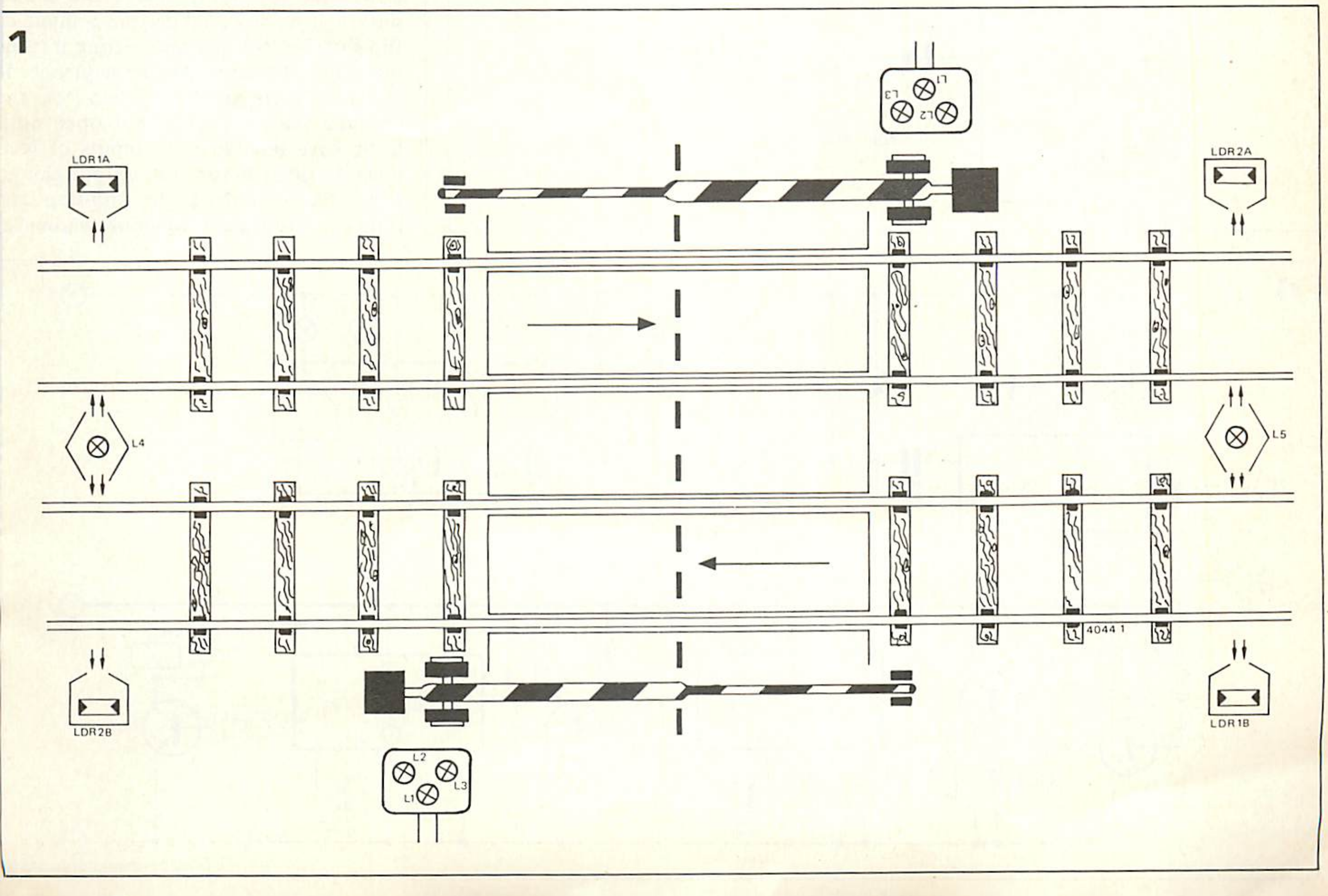


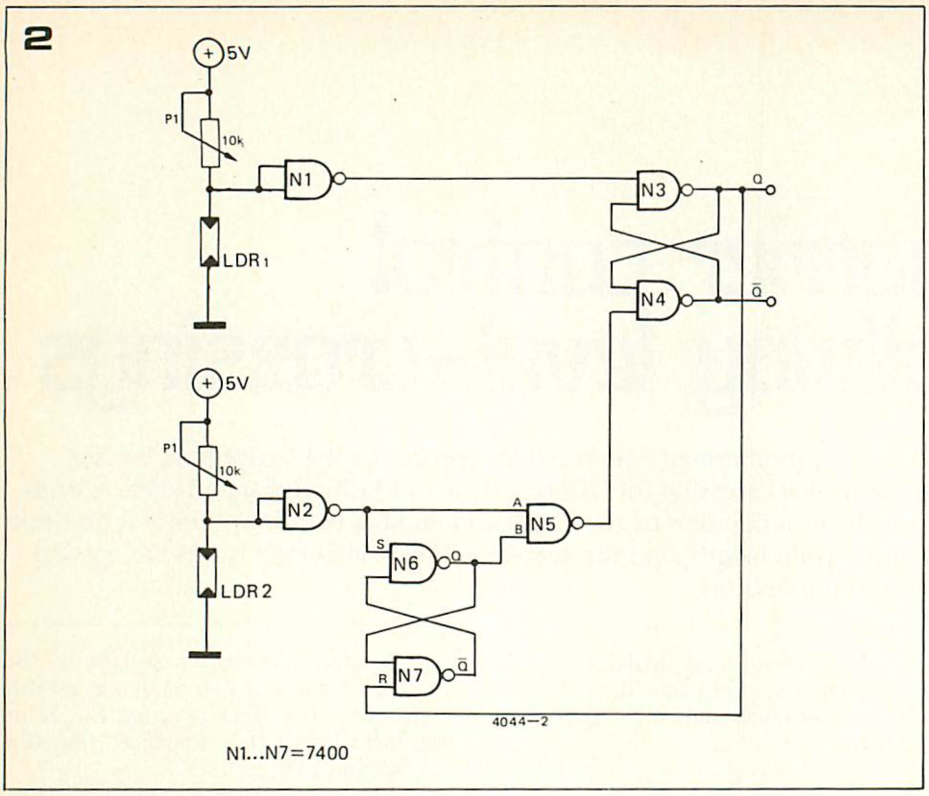
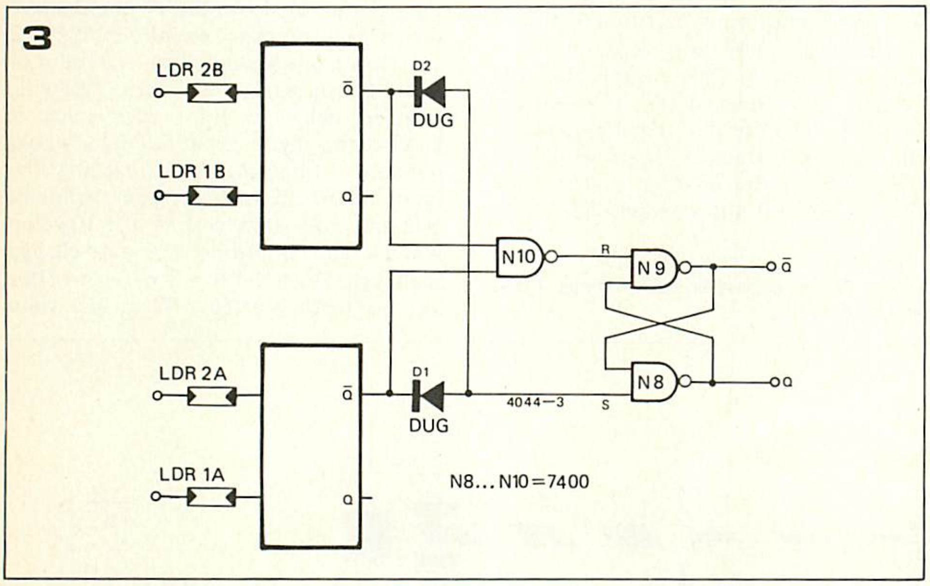


Figure 2. The train detection logic for one line.

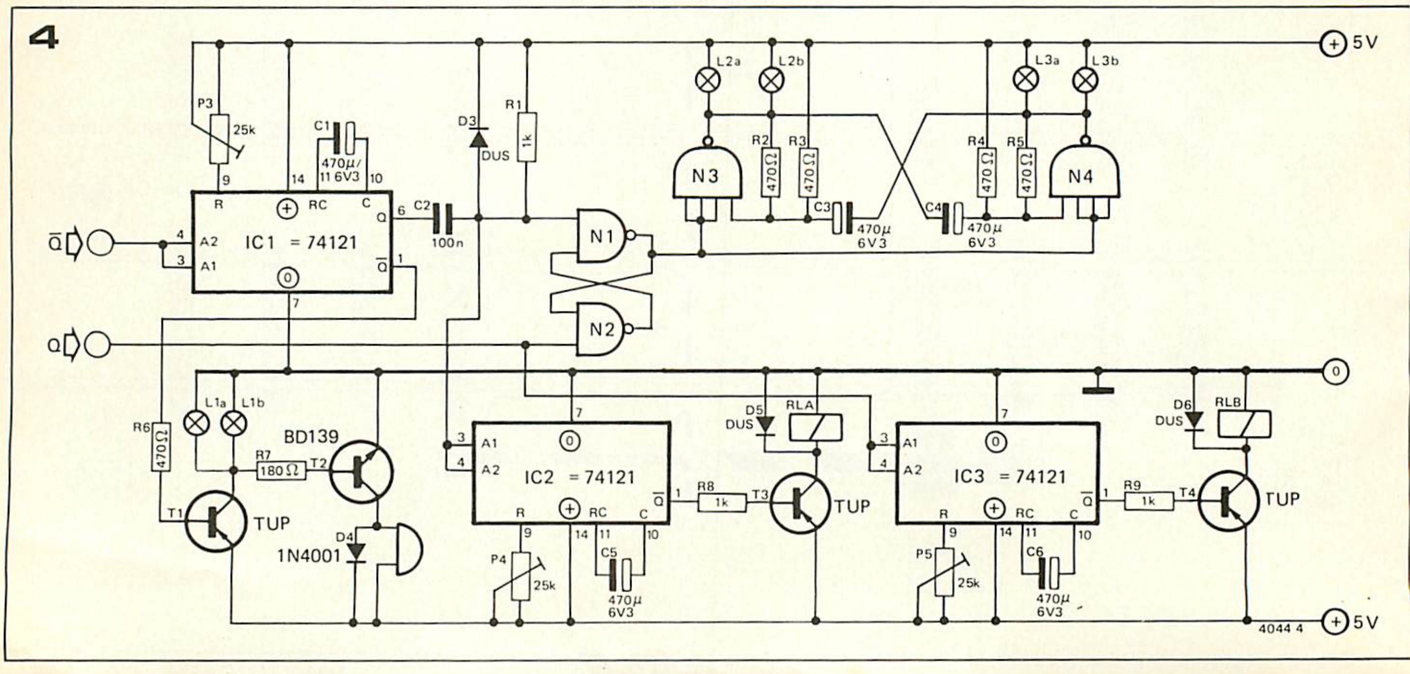
Figure 3. For two-way traffic, as in figure 1 two circuits as in figure 2 must be interconnected.

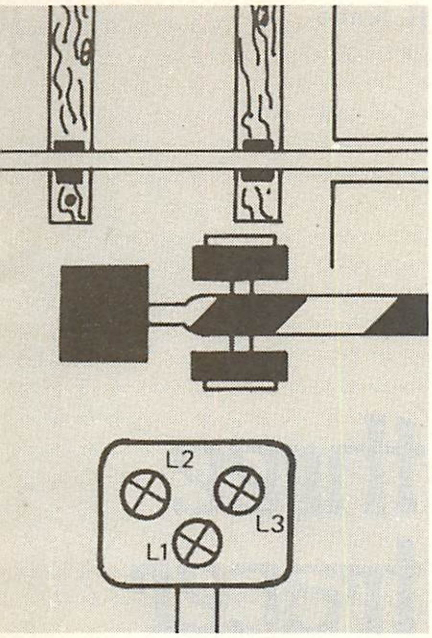
Figure 4. This circuit controls the lights and the opening and closing of the gates.



reaches LDR2 flip-flop N6/N7 is set in a similar manner. The B input of N5 is thus held high by the Q output of this flip-flop. When the end of the train has passed LDR2 is re-illiminated so the input of N2 therefore goes low and the output goes high. Since both inputs of N5 are now high the output goes low resetting flip-flop N3/N4, which in turn resets flip-flop N6/N7.

Since the gates must be activated by a train on either the upline or the down line the circuit of figure 2 must be duplicated. Figure 3 shows how the two circuits are interconnected. D1 and D2 perform an OR function. When a train approaches on either the up line or the down line (or both) one of the $\overline{Q}$ outputs will go low, taking the S input of flip-flop N8/N9 low and setting it, thus initiating the gate closure sequence. If however there are two trains on the crossing the gates must not open until both have left, so both inputs of N10 must be high before the output can go low, thus resetting the flip-flop and initiating the gate opening sequence.





Gate opening and closing sequence

The circuit that controls the lights and opening and closing of the gates is given in figure 4. When a train approaches and the Q output of figure 3 goes low this triggers monostable IC1. While IC1 is in the triggered state T1 and T2 are turned on, the amber lamps (L1) light and the bell rings. When IC1 resets the Q output goes low. This transition is differentiated by C2 and R1, producing a short, negative-going pulse that sets flip-flop N1/N2. Until this flip-flop is set the inputs of the astable comprising N3/N4 are held low by the output of N1, so the outputs of N3 and N4 are high and lamps L2 and L3 are extinguished. When the flip-flop is set the inputs of N3 and N4 are taken high, so the astable starts to oscillate and lamps L2 and L3 flash alternately.

The same negative-going pulse also triggers IC2. While IC2 is triggered T3 is turned on pulling in relay RLA, whose contacts are used to switch the gate motor (or solenoid). The period of IC2 may be adjusted by P4 until it is just long enough to allow the gates to close, thus avoiding unnecessary dissipation in the relay coil.

After the train has passed the Q output of figure 3 goes low, resetting flip-flop N3/N4 so that the lights stop flashing. It also triggers monostable IC3, which activates RLB to open the gates. The period of IC3 may also be adjusted by P5.

Setting up procedure

It is evident that the LDR's must be mounted sufficiently far on either side of the crossing that the train does not arrive before the gates close. The LDR's should be mounted in tubes to screen them, as far as possible, from extraneous light. P1 and P2 should be adjusted so that, whatever the ambient lighting conditions in the room, N1 and N2 will switch reliably when a train passes. P3 is used to adjust the delay between the approach of a train being detected and the closing of the gates i.e. the time for which the bell rings and the amber lamps are lit. ◀

W. Back

turning off thyristors

When thyristors are carrying A.C., they will turn off at every zero-crossing — which can be a nuisance. When carrying D.C., however, they won't turn off at all — which is worse.
This article takes a basic look at how to cope with the latter problem.

There is a growing tendency in electronics for electromechanical switches to be replaced by semiconductor devices. In light current applications transistors are now capable of switching currents which a few years ago would have required the use of relays, whilst in power engineering thyristors can switch loads that would normally require fairly hefty contact breakers, without the associated problems of contact wear due to arcing. A.C. current control with thyristors is fairly simple, but this article takes a basic look at some methods of switching D.C. currents with thyristors.

Switching of A.C. currents with thyristors is relatively easy. As is well known, in its non-conducting state a thyristor will block a potential applied to it in a forward direction (i.e. positive to anode, negative to cathode). However, application of a positive trigger pulse to the gate will cause it to conduct, and it will remain conducting even after the gate input is removed. The only way of returning the thyristor to its blocking state (unless it is a gate turn-off device) is to reduce the current through it below a critical value (the holding current) for a period of time depending on the device in question (the turn-off time).

In A.C. circuits of course, the current through the thyristor attempts to reverse during the negative half-cycle of the waveform, but since a thyristor will not conduct in the reverse direction it turns off at the zero-crossing point of the waveform. No such convenient trick occurs in D.C. circuits.

In D.C. circuits the only two methods of turning off a thyristor are:
- break the circuit so that the current is interrupted.
- momentarily divert the current from the thyristor so that it will turn off.

The first proposition is obviously impractical as breaking the circuit would require a switch or relay capable of switching the current that the thyristor was carrying, which defeats the object of the exercise. The second proposition brings us to the principle of capacitor commutation. If a capacitor is charged and then connected so as to reverse bias the thyristor, then the load current will see the capacitor as a very low impedance into which it will momentarily flow, and the thyristor will turn off.

Figure 1 is the most basic example of such a circuit. When current is flowing in the load R_L then C1 will charge with the polarity shown via R1. When the switch S is closed the capacitor is connected with reverse polarity across the thyristor. The load current sees this as a low impedance and is momentarily diverted into it. The thyristor meanwhile is reverse biassed by the voltage across the capacitor and turns off.

This circuit is clearly not of much practical use, since it also requires a switch, but it does illustrate the principle. A more practical variant of the circuit is illustrated in figure 2. This uses an auxiliary thyristor to switch in the capacitor. R1 is chosen such that after Th1 has turned off and C1 has charged through Th2 with the opposite polarity to its original charge, then the current flowing through Th2 via R1 must be less than the holding current of Th2 so that this thyristor will turn off. This clearly places a lower limit on the value of R1. The lowest value of C1 is also limited by the time it takes to discharge to zero volts on turning on Th2. This must be greater than the turn-off time of Th1 as otherwise C1 will have discharged and begun to recharge in the opposite direction before Th1 can turn off.

The maximum rate at which the circuit may be switched on and off is determined by the time taken to recharge C1 through R1 after Th1 has been turned on again.

Even with the minimum permissible values for C1 and R1 the switching rate is limited to a few hundred Hz in most instances.

A method of increasing the maximum switching rate is to use capacitor turn-off with a ringing choke, and the basic circuit is given in figure 3. If Th2 is initially turned on then C1 will charge through Th2 and R_L, until it has

acquired full supply potential, when Th2 will turn off. If Th1 is now turned on then a parallel resonant circuit consisting of L and C1 is completed, which starts to ring due to the initial charge on C1.
During the first half-cycle current flows through Th1, D and L and reverse charges C1. The diode prevents C1 from attempting to discharge back through L and Th1. Of course, a D.C. current also flows through Th1 into the load. If Th2 is now turned on the reverse-charged C1 is connected across Th1, turning it off. With this method switching rates of up to 1 kHz can be achieved.

Figure 1. Capacitor commutation using a switch to connect the capacitor across the thyristor.

Figure 2. Using an auxiliary thyristor to switch in the commutation capacitor.

Figure 3. Using a ringing choke arrangement to increase the maximum switching rate.

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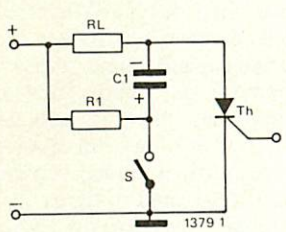

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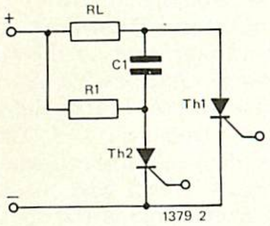

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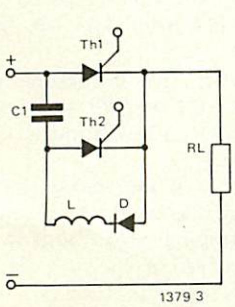

Calculation of commutation capacitor

When the auxiliary thyristor is turned on a negative voltage appears across the main thyristor. This reduces to zero as the load current flows into the capacitor and, provided the main thyristor actually turns off, the voltage on the capacitor will eventually assume full positive supply voltage, at which point the auxiliary thyristor will turn off.
It is evident that the main thyristor must turn off before the voltage on the commutation capacitor assumes a positive value, or it will never turn off. This means that the time taken for the voltage across the capacitor to reach 0 V must be greater than the turn-off time of the main thyristor. Now this time is determined by two factors, the charging current flowing into the capacitor through the load and the capacitance of the capacitor.
Initially current is being driven through the load by a voltage 2 V_b. (supply voltage plus the initial voltage across the capacitor). By the time the voltage across the capacitor has reached zero the current is being driven by the supply voltage V_b.
Initially therefore the current is $\frac{2\,V_b}{R_L}$, and finally it is $\frac{V_b}{R_L}$.
The average current is therefore approximately $\frac{1.5\,V_b}{R_L}$. This is of course a gross approximation as it assumes linear charging, but it is adequate for calculating the commutation capacitor.
Now since $Q = CV = I\Delta t$.
where Q is charge on capacitor.
C is capacitance
V is voltage on capacitor (= V_b).
I is average charging current (= $\frac{1.5\,V_b}{R_L}$).
Δt is charging time (= turn-off time of thyristor).
Then

$$\frac{1.5\,V_b \cdot \Delta t}{R_L} = CV_b.$$

Therefore

$$C = \frac{1.5\,\Delta t}{R_L}$$

This is the minimum value of capacitor to turn off current flowing through a load R_L. In practice the value of C should be slightly larger than this to ensure reliable commutation. The commutated turn-off time of the thyristor (usually designated t_q) can be obtained from the manufacturer's data sheets, and the load R_L is of course known, so C can easily be calculated.

R. Sintic

three tracer

It is possible to display more than one trace on the screen of a single-beam 'scope, using a fast electronic switch. This design will interleave three traces, which may be of analogue or of digital signals. The practical results appear quite acceptable for such a simple set-up.

The circuit

The generator for the switching frequency is a discrete-component shift register which is arranged to 'chase its tail'.
The circuit around T1, T2 and T3 in figure 1 is the actual shift register. A switch (S1) changes the repetition rate from a low value (200 Hz) to a high one, by applying bias to the diodes D1, D2 and D3. The choice of switching frequencies makes it possible to display input frequencies between 20 Hz and 500 kHz.
The pulse-shapers T4, T5 and T6 improve the rise time of the thre

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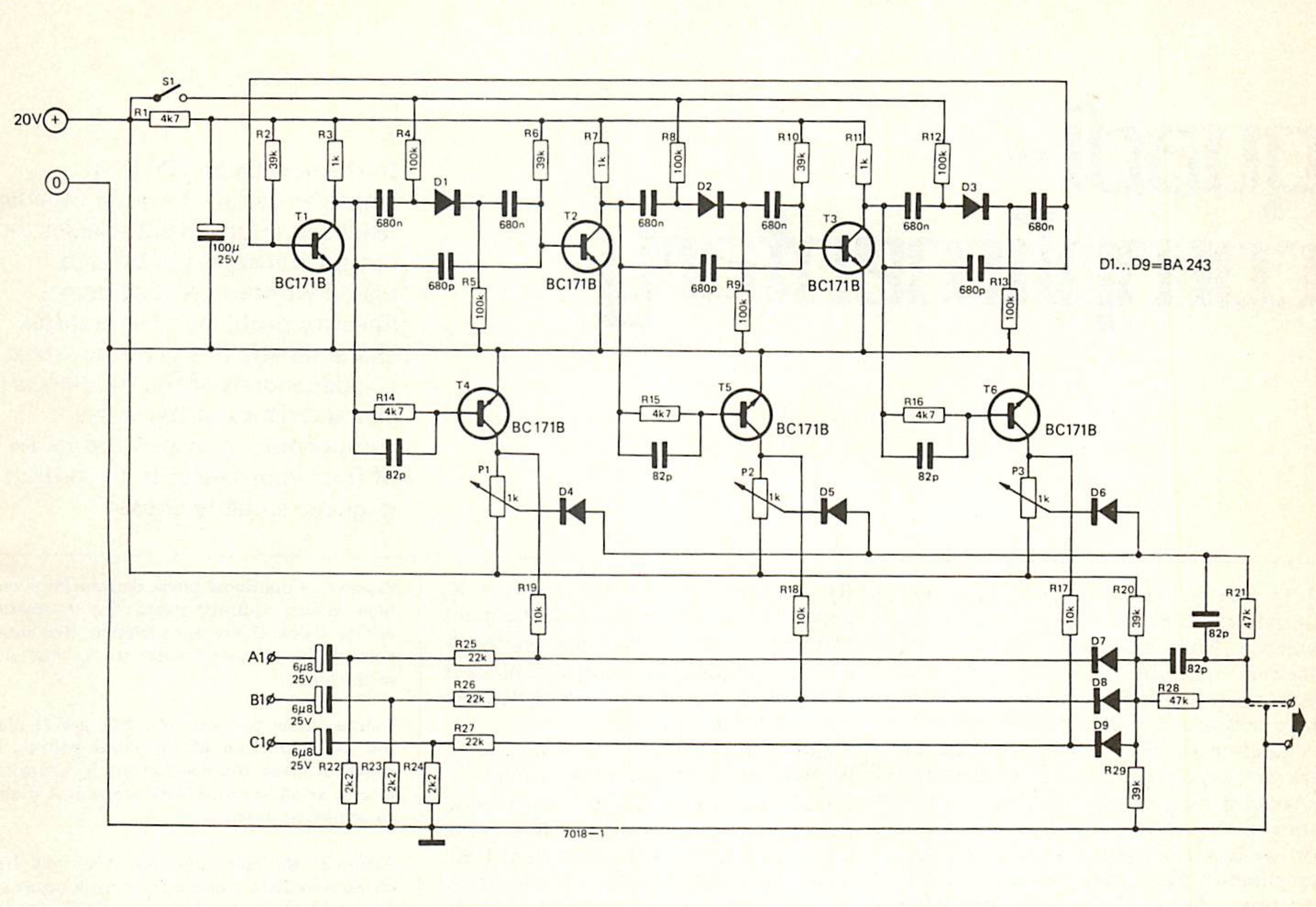

vitching waveforms. The same circuit vitches the DC level of the output acording to the required position of the ıree traces on the screen.

otentiometers P1 to P3 in the collector rcuits of T1 to T3 achieve the DC tting for trace position by varying ıe negative level in the three recıngular signals. As the signals in turn ecome negative, the diodes D4 to D6 ıss them to the output RC network. he signal-switching is done by diodes 7 to D9. They in turn pass the AC omponents of the input signals at A1, 1 and C1 to the output.

o achieve a high input impedance ıd to compensate for the insertion ss of the circuit it is necessary to rovide each input channel with a prenplifier. The gain of each of these prenplifiers can be preset, for calibration ırposes.

reamplifiers with input ttenuators

simple preamplifier of high input imedance can be made using a JFET. urrent-dependent negative feedback is pplied to improve the linearity. Caliration is achieved by presetting the ıtput voltage of each channel.

he input attenuator in each channel frequency-compensated, to enable st rise-time waveforms to be reproıced without distortion. The omponent values given in figure 2 e nearest 'preferred value' aproximations. They are intended for pplications where absolute accuracy is not so important. In other cases it will be necessary to make up the attenuator with close-tolerance precision resistors.

The input blocking capacitor, shown dotted, will only be needed if small AC voltages superimposed on large DC voltages - such as rectifier ripple - are to be observed.

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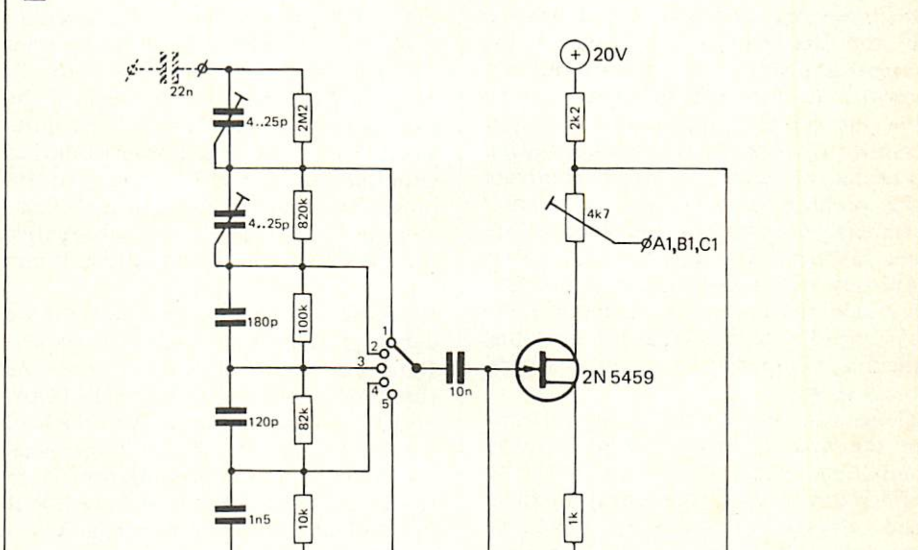

Figure1. Circuit diagram of the three-trace switch. A discrete-component shift register, arranged to 'chase its tail', continuously produces three evenly-spaced sequential pulses.

Figure 2. Preamplifier with input attenuator. Three of these stages are needed; one to drive each of the switch-inputs A1, B1 and C1. (see figure 1).

quadi-complimentary

In the new Quad 100 Watt amplifier design, a special negative feedback arrangement enables the output transistors to be zero biased without creating non-linearity problems. The transfer characteristic of the output stage is independent of the (non-linear) characteristics of the active components, provided the values of four impedances in the output stage are suitably chosen.

Zero bias for power transistors in the output stage of an amplifier is advantageous from the point of view of thermal stability. However, zero bias will result in a 'dead zone', which in turn results is crossover distortion.
A solution to the problem is to bias the output stage into class AB so that the characteristics of the alternate output transistors overlap, resulting in a more or less linear behaviour around the zero crossings of the signal. For success, this strategy relies on the symmetry of the alternate output stage halves. Furthermore, the influence of temperature on the bias setting is of utmost importance. If the base-emitter junctions of the output transistors are part of the bias circuit, the bias will be influenced by the junction temperature of the output transistors. Temperature compensation schemes can never completely eliminate this problem, if only because junction temperature and case temperature are not the same. For this reason, the bias will vary with music program dynamics, resulting in momentary non-linear behaviour. Thermal processes - including thermal compensation - are comparatively slow!
Things can only become more difficult in the new generation of high power amplifiers rated from 100 Watts to 800 Watts (Crown, Phaselinear, Luxman and others). In order to meet the required voltage and current demands, each 'output transistor' has to be composed of several transistors in parallel. Sometimes it may even be necessary to use two transistors in series for each 'parallel transistor'. It will be obvious that it is very difficult to obtain a constant bias when this is influenced by say eight very hot base-emitter junctions. For this reason it is common practice to zero bias all the output transistors.
Figure 1 shows the functional block diagram of a zero bias output stage. Block B has a 'dead zone', i.e. an area around the crossover point where it will deliver little or no output current. Block A supplies current into the load R_L through one of the resistors R, depending on the polarity of the input voltage. If the voltage drop across R exceeds the threshold voltage of block B (V_D) either the NPN or the PNP power transistor is turned on.
Figure 2 shows the characteristics of A, B and the resulting load current I_L versus the input voltage. In a good design the characteristic of B is quite linear as a result of local current feedback by emitter resistors. Generally speaking the driver stage A has an optimal class-AB bias. Provided the mutual conductance of A (the slope $d(I_A)/d(V_{in})$, which is usually inversely proportional to R) is in the same order of magnitude as the slope of B, $d(I_B)/d(V_{in})$, the resulting bend of the load current characteristic will be quite small. So, in the high power amplifiers adopting this current dumping strategy, crossover problems are mild and occur at higher output levels. Overall negative feedback can usually straighten things out.
However, it would be even better if we could get rid of this bend altogether. Referring now to figure 3: Above the threshold voltage $+V_D$ (and below $-V_D$) the contribution of A to the load current is limited. It would be ideal to obtain a zero contribution of A to I_L ($\beta = 0$), because this would mean that the dissipation of the driver stage A is as low as possible. Unfortunately, this would also mean that the voltage drop across the resistor R is limited to $\pm V_D$, making it impossible to turn on the transistors within block B any further. So, we will have to look for a solution which gives the smallest possible value for β.

The Quad amplifier

Figure 4 shows the basic principle of the Quad amplifier, which has been developed by P.J. Walker and M.P. Albinson of the Acoustical Mfg Company.
A is a class-A amplifier with a high open loop gain (A_0). It is capable of delivering an output power of about

Figure 1. Functional block diagram of a ver[y] high power output stage. The transisto[rs] within block B are zero biassed. The inpu[t] voltage V_{in} is taken relative to the 'hot' sid[e] of the load.

Figure 2. The currents I(A), I(B) and I_L plo[t]ted as a function of the input voltage. I[n] order to make the bend in the I_L characte[r]istic as small as possible the slope of A shoul[d] be as high as possible.

Figure 3. By combining the I(A) and I(B) characteristics a straight I_L curve is obtaine[d]. The angle β should be minimal in order t[o] keep the dissipation of A as low as possibl[e].

Figure 4. The basic principle of the ne[w] Quad 100 Watt amplifier. All voltages a[re] relative to the 'hot' side of Z_L.

Watts. This amplifier supplies current nto the load (Z_L) through Z_3. As soon the threshold voltage of either one f the zero biassed power transistors T1 nd T2 is exceeded, the transistor in uestion is turned on and supplies a urrent I_4 through Z_4 into the load. oth Z_1 and Z_2 are large compared to $_3$ and Z_4.

he negative feedback arrangement is uite unconventional. The voltage at the verting input of A with respect to the ot' side of Z_L is the sum of the oltage drop I_4Z_4 across Z_4 and a action $Z_1/(Z_1 + Z_2)$ of the base-emit-r voltage of $T_1 - T_2$. This means that egative feedback is not only derived om the output of the amplifier, as in onventional circuits, but also from the put voltage of the (non-linear) output age. It will be shown that this feed-ack arrangement may lead to a load urrent I_L that is independent of the characteristics of T1 and T2.

Calculations

Referring to figure 4, the current I_L through the load Z_L is calculated as a function of the input voltage V_{in}. All voltages are with respect to the 'hot' side of Z_L.

For amplifier A, with an open loop gain of A_0, the following holds:

$$V_+ = V_{in} \tag{1}$$

$$V_- = I_4Z_4 + \frac{Z_1}{Z_1 + Z_2} \cdot (V_A - I_4Z_4) \tag{2}$$

$$V_A = A_0(V_+ - V_-) \tag{3}$$

(1) and (2) substituted into (3):

$$V_A = A_0V_{in} - A_0V_A \frac{Z_1}{Z_1 + Z_2} - A_0I_4Z_4 \frac{Z_2}{Z_1 + Z_2} \tag{4}$$

Re-arranged:

$$V_A \left(1 + \frac{Z_1}{Z_1 + Z_2} A_0\right) = A_0V_{in} - A_0I_4Z_4 \frac{Z_2}{Z_1 + Z_2} \tag{5}$$

If $A_0 \gg 1$ then:

$$V_A = \frac{Z_1 + Z_2}{Z_1} \cdot V_{in} - \frac{Z_2}{Z_1} \cdot I_4Z_4 \tag{6}$$

so:

$$I_3 = \frac{V_A}{Z_3} = \frac{Z_1 + Z_2}{Z_1Z_3} V_{in} - \frac{Z_2Z_4}{Z_1Z_3} I_4 \tag{7}$$

$$I_L = I_3 + I_4 \tag{8}$$

(7) combined with (8) results in:

$$I_L = V_{in} \frac{Z_1 + Z_2}{Z_1Z_3} + I_4 \left(1 - \frac{Z_2Z_4}{Z_1Z_3}\right) \tag{9}$$

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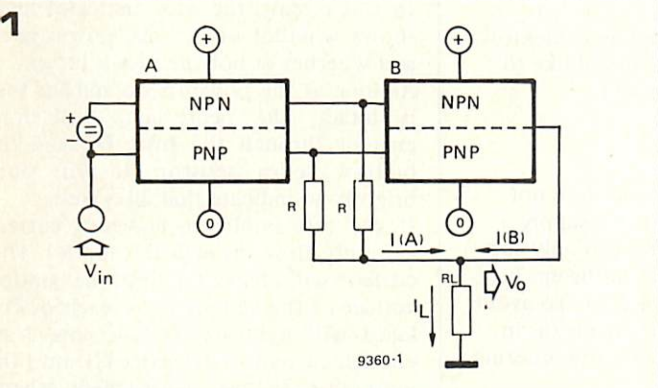

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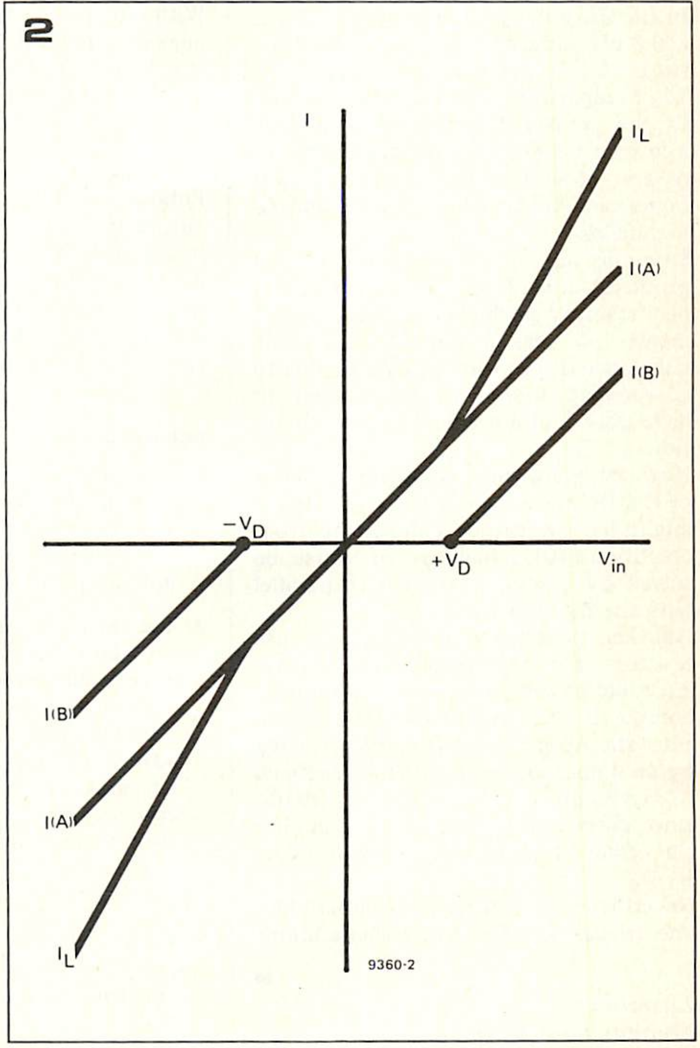

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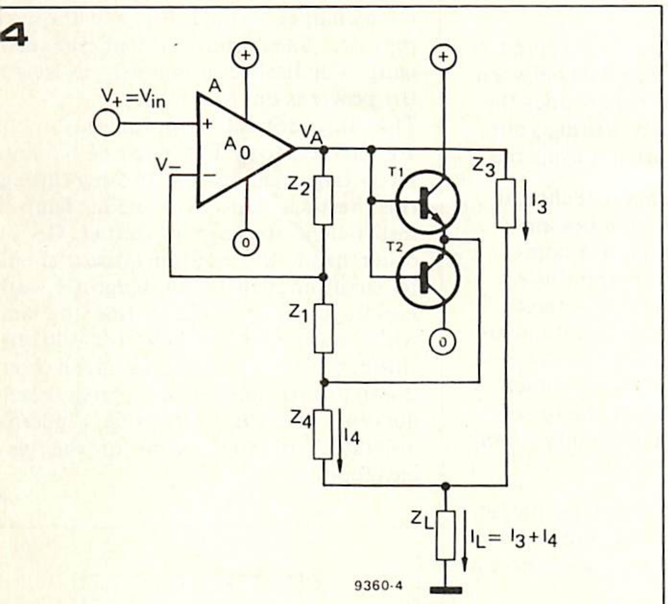

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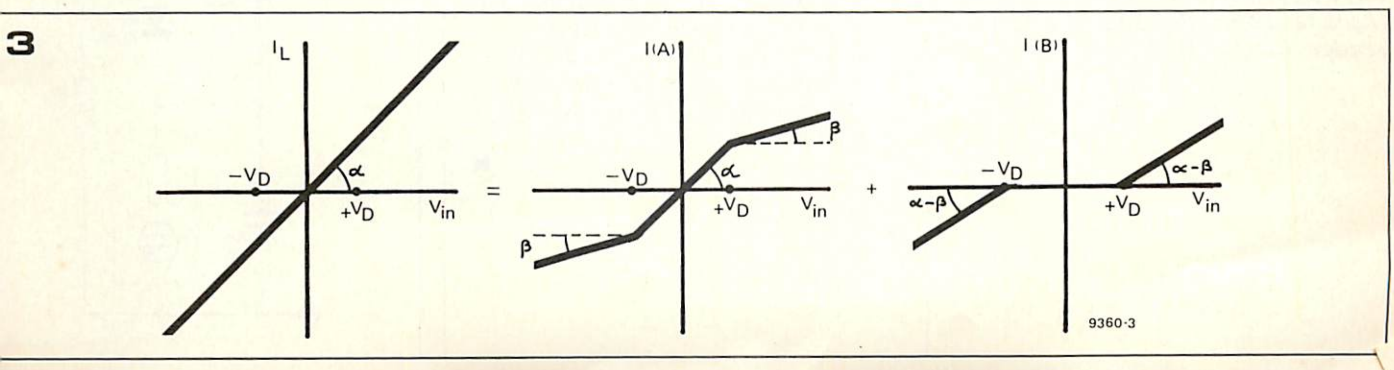


Something wonderful happens when:

$$Z_1Z_3 = Z_2Z_4 \qquad (10)$$

(Just like the Wheatstone-bridge!)

In that case:

$$I_L = V_{in}\frac{Z_1 + Z_2}{Z_1Z_3} =$$

$$= V_{in}\left(\frac{1}{Z_3} + \frac{1}{Z_4}\right) !!!! \qquad (11)$$

In other words: The current through the load is independent of any active parameter. The dead zone of T_1 - T_2 doesn't appear in the load current.
What happens is that this feedback arrangement introduces non-linear feedback in such a way that the relationship between load current and input voltage becomes linear. From formula (6) it follows that the drive voltage V_A to the output stage T_1 - T_2 depends on the value of I_4Z_4.
In the Quad design, the impedance Z_4 is a 0.3 μH inductor; Z_3 is a 100 Ω resistor, Z_1 a 3.3 k resistor and Z_2 a 10 pF capacitor. Condition (10) is met.
In the emitter follower configuration a resistor between the inverting input of A and ground is added. The output impedance of the amplifier is Z_3 and Z_4 in parallel.
Summing up, a lot of typical class-B problems are solved. The design has no bias stability problems, no bias adjustments, no bias at all. A reasonable imbalance in the values of Z_1-Z_4 due to component tolerances in claimed to have only a minor effect on the distortion.
However, we wonder what the influence of the DC-resistance of the Z_4 inductor might be - it causes a departure from condition (10), which can, of course, be solved by placing a resistor in parallel with the Z_2 capacitor.
Another possibility would be to use resistors for the impedances Z_1-Z_4. Z_4 could be say a few tenths of an ohm, composed of non-inductive carbon resistors. Amplifier A could be preceded by an amplifier, and an overall feedback of say 20 dB would result in a virtually zero output impedance and minimise the effect of imbalance in the resistors R_1-R_4.
Nevertheless, referring to formula (11), one can say: Quad erat demonstrandum!

Literature:
'Current dumping amplifier' by P.J. Walker and M.P. Albinson. (Lecture during the 50th A.E.S. Convention, London 1975.)

elektor services to readers

With reference to the column that appeared under this heading in elektor no. 3 (April 1975), we should like to amplify the following points.

eps service

Publication of a p.c. layout does not automatically imply that we supply a board for that design. We can only supply boards which appear in the eps list in the current issue of elektor. To avoid errors please quote board name (as in eps list) and part number when ordering.

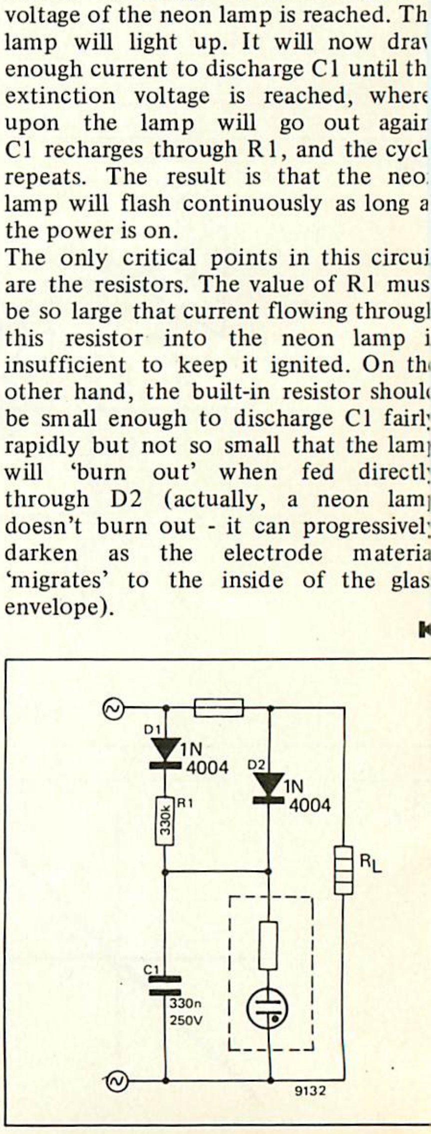
technical queries

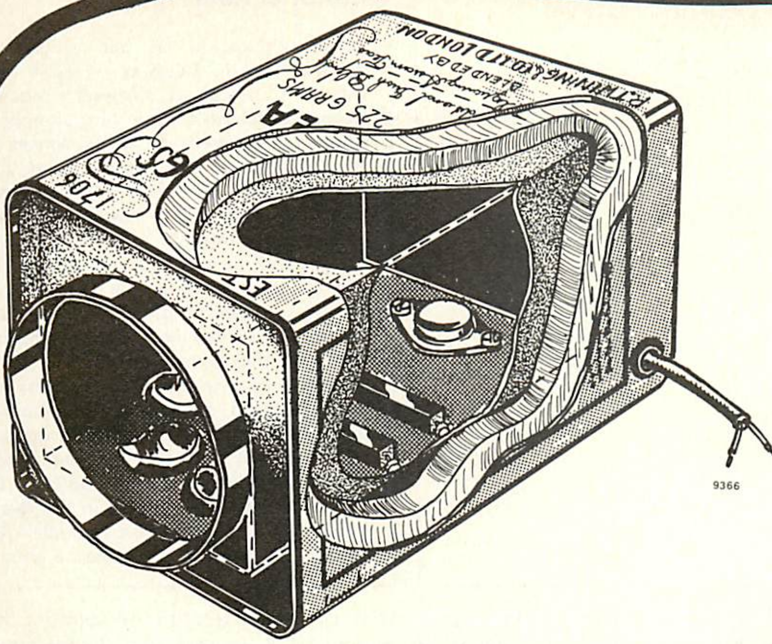
1. Telephone queries can be accepted only on Monday afternoons between 14.00 and 16.30. At other times the editorial staff are busy writing your next magazine and are not available.
2. The service is for genuine technical problems only. Many queries are about sources of supply for components and we can answer these only by asking readers to contact advertisers in the magazine. Remember, most advertisers do not advertise complete stocks, so please contact them before overloading the tq service. If you still have difficulty, then contact us.
3. When writing to the tq service please enclose a stamped, addressed envelope, otherwise we cannot guarantee a reply.
4. When writing to several different departments please enclose separate letters to each department, as otherwise delays may result while your letter is processed by each department in turn.

J.W. van Beek

fuse indicator

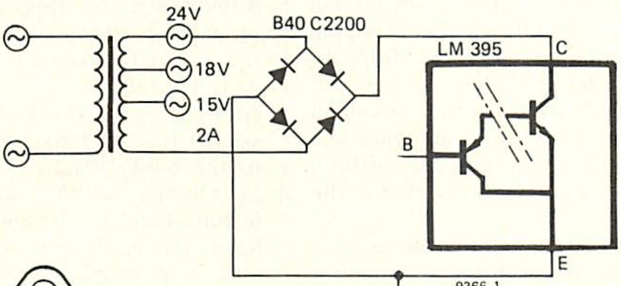
In this circuit, the neon indicator lam[p] shows whether or not the power is o[n] and whether or not the fuse is blown.
As long as the power is on and the fus[e] is intact, the neon lamp will draw current through the fuse, D2 and th[e] built-in series resistor. It will bur[n] brightly to indicate that all is well.
If the fuse is blown, however, curren[t] can only flow through D1 and R1. Thi[s] current will charge C1 until the ignitio[n] voltage of the neon lamp is reached. Th[e] lamp will light up. It will now draw enough current to discharge C1 until th[e] extinction voltage is reached, where[-] upon the lamp will go out agai[n]. C1 recharges through R1, and the cycl[e] repeats. The result is that the neo[n] lamp will flash continuously as long a[s] the power is on.
The only critical points in this circui[t] are the resistors. The value of R1 mus[t] be so large that current flowing throug[h] this resistor into the neon lamp i[s] insufficient to keep it ignited. On th[e] other hand, the built-in resistor shoul[d] be small enough to discharge C1 fairl[y] rapidly but not so small that the lam[p] will 'burn out' when fed directl[y] through D2 (actually, a neon lam[p] doesn't burn out - it can progressivel[y] darken as the electrode materia[l] 'migrates' to the inside of the glas[s] envelope).

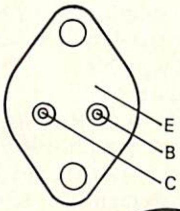


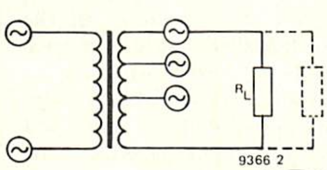


chestnut oven

As the days were once again growing shorter, a designer had a nostalgic dream – about the good old days with the whole family gathered around the open coal fire. Something, he felt sharply, was missing from his thermostatically-controlled centrally-heated home ...
Something that would roast chestnuts ...
The oven is constructed in an old tea- or biscuit-tin, with lid. An inner compartment, made from aluminium or copper sheet, is fitted inside the tin – well insulated and adequately supported by means of a blanket of glass-wool.
A heating element is mounted underneath (or on top of) the floor of the insulated inner compartment. This element may conveniently consist of a few wirewound resistors – but the thermostatically-controlled centrally-heated version would use the dissipation from an LM 395 regulator.







The maximum power required for an oven of 50 cubic inches will be about 50 watts. The circuit for the simple version is given in figure 2. A tapped transformer (to enable the heating power to be adjusted) directly feeds the power-resistors. The transformer must be rated for at least 50 voltamperes (in the example) and the required resistor value follows from $R = \frac{V^2}{50}$, where V is the highest available secondary voltage.
Since 10-watt resistors are readily available, and also to spread the heat production over a larger area, it is recommended that five resistors be used in parallel. The individual resistors should then each of course have five times the value R determined above.
The automated version of the chestnut oven (see figure 1) uses an LM 395 integrated regulator. This device is in fact a voltage stabiliser, provided with a current-limiting circuit and a thermal shut-down. When the device operates into a dead-short it will work as a constant-current sink (at the limit-current of 2 A), dissipating V_{RMS} x 2 A watts – at any rate until the temperature reaches 170°C, the shut-down temperature. The supply voltage determines the 'on' dissipation, while the device determines its own duty cycle as required to maintain 170°C.
There are two ways to destroy an LM 395: one can connect a supply of the wrong polarity, or one can apply a (peak) voltage in excess of 36 volts. The circuit requirements are therefore simple: the transformer secondary voltage must first be passed through a full-wave rectifier (in this case a bridge type), and the applied peak voltage must remain below 36 V under the highest mains supply value that can possibly be encountered. A safe voltage rating for the transformer secondary would be 22 V. At 20% mains overvoltage (what is the chance of that occurring?) the peak voltage would be 37.2 – which means 36 V after the rectifier.
The chestnuts pop after a half- to one hour.

santatronics

Victor Company of Japan, Limited (JVC)

cd-4

Editorial note

After publication of our article on quadrophony ('Quadro 1-2-3-4 . . .', Elektor 1, p. 33) we received a request from JVC/Nivico to give them an opportunity to comment on it. We agreed to this, subject to the proviso that the proponents of the other three systems (SQ, QS and UD-4) were given an equal opportunity.
To this end, we sent copies of this article and of the second article ('Quadro in practice', Elektor 4, p. 646) to all parties concerned, explaining the situation and asking for their comments.
However, to date the only comment we have received for publication comes from JVC – in spite of repeated written and personal requests to the other parties. We now feel that it is only fair to JVC to print their reaction in full, even though we cannot present a parallel discussion of any of the other systems.

Over five years have elapsed since the CD-4 system was announced as a means of achieving quadraphony from a disc record. The worldwide popularization of the CD-4 system is now making rapid progress, thanks to various factors such as the wider variety of software – about 1000 CD-4 albums have been released – improved, more compact cutting equipment, the development of high performance PU cartridges, the high level of integration used in the demodulation circuit, etc. However, there seem to be various misunderstandings of the CD-4 system because of some unfortunate occurrences at the initial stage: played back sound was unsatisfactory because of inferior service to end users during the course of the development, parties with differing interests issued misleading publicity, etc.
For this reason, in this paper, we would like to restate our policy on CD-4 and describe the present state of CD-4 technology to give readers a fuller understanding of the CD-4 system.

The CD-4 system was undertaken to make possible a disc record which would transmit accurately the 4-channel musical information that the people who make the record – musicians, directors and mixing engineers – want the music listeners to hear.
Figure 1 shows a process through which the four separate channel signals can be transmitted using the disc record as the medium.
The 4-channel program source is achieved by collecting sound from the sound field where the live performance is going on, converting these sounds to electrical signals and then composing the 4-channel signals with the mixing console. The various steps in this chain of events are carefully controlled so that the end result satisfies the producers. At this stage, the producer's sole intention is to achieve the desired artistic effect. The end result of this step is a combination of the musical techniques and artistic expression of the performers and the technical abilities of the mixing engineers; it is monitored always paying careful consideration to the listening conditions in which the average user will hear it. The output is the 4-channel master tape (A) which represents the sum total of these peoples' efforts, which they wish to present to the public.
Therefore, it is essential that the recording system transfers all the information to the master tape and that the performance of the mixing console – in the artistic stage described above – is such that the output is loss-free with respect to the input and that the physical properties of the sound such as phase and amplitude of the input signal can be controlled to match the intentions of the producer exactly.
The 4-channel master tape is not the end product which the user buys; a suitable means of duplicating it must be found. This is the CD-4 disc record (B), which has the same channel capacity as tape (A).
The fact that the channel capacity of (A) is equivalent to that of (B), means that the same quality of sound can be played back. In this way the producer's intentions are transmitted exactly as they are to the listener.
While every effort has been made to achieve this (A) = (B) concept in the CD-4 system, another consideration which was not neglected in any way was sufficient compatibility with conventional stereo and mono playback equipment. Therefore:

1. It must guarantee sufficient channel separation when the CD-4 record is played back in stereo and a natural sound image must be obtained.
2. There must be no loss of musical information when the CD-4 record is played back in mono.

If sufficient consideration of these factors is not given when the signals for the 4-channel disc record are being composed, channel separation in stereo playback will deteriorate and phase differences will occur, thus narrowing the sound field and creating out-of-focus sound images resulting in music which is fatiguing to listen to. If this happened, the (A) = (B) concept would not achieve its full potential.
Another basic consideration in the design of the CD-4 system is that the cost to the buyer must be minimized as far as possible, without detriment to the technical and artistic considerations outlined above. Keeping this principle in mind, the composition of the record signals in the CD-4 system were simplified as much as possible.
Manufacturers have taken various steps in the past to lessen the load on the buyer; compensation for distortion and losses, integration of the detector circuit, improvement of styli (especially the SHIBATA stylus) and the development of low-cost PU cartridges for CD-4 using this Shibata stylus.
The will of the developers to achieve the two basic concepts 'discreteness' and 'compatibility' are reflected in the fact that the new system was named CD-4; C for compatibility between the different playback modes and D for the discreteness of the signals, inherent in the

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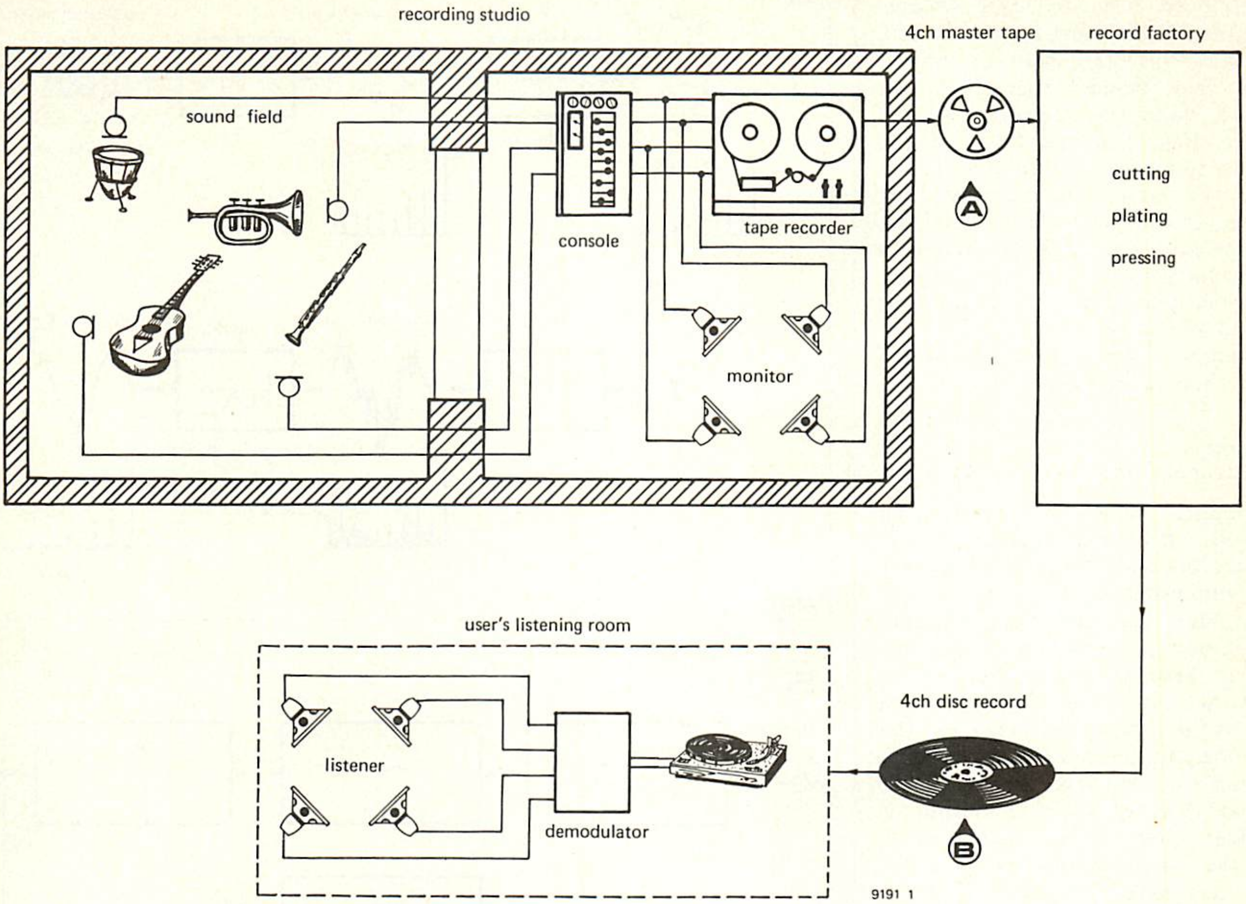

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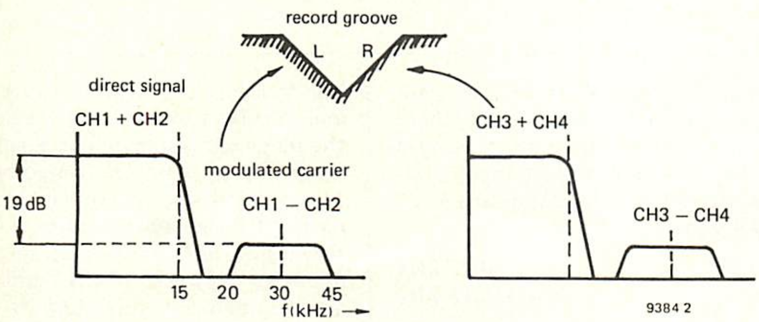

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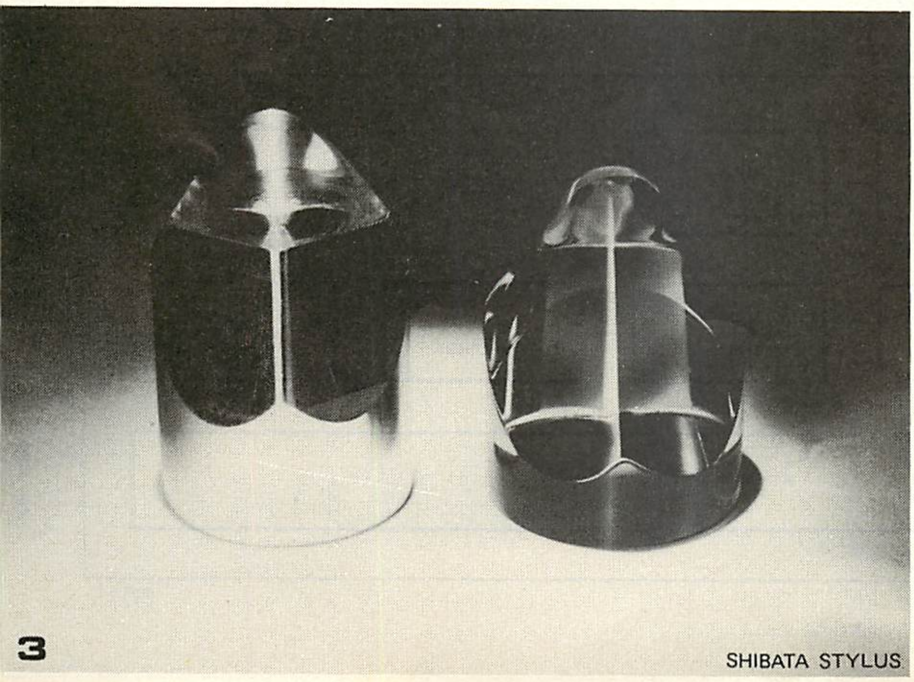

record having equivalent channel capacity.

Details of the CD-4 record

Since the CD-4 record is required to transmit four signals perfectly, it is necessary to double the channel capacity when compared with conventional stereo records.
However, changing the physical shape of the disc record would make it incompatible with stereo and mono records and would greatly increase cost to the user because a new, complicated transducer would be needed. This is the reason why the frequency superimposition technique – 'base band signal' + 'carrier' – was introduced for the CD-4 system.
At this stage, the points under consideration were that the modulation and demodulation of the signal to be superimposed had to be relatively straightforward and the medium to be used for the recording was the standard disc record. Through careful investigation and the comparison of various modulation systems, angular modulation was adopted as being most suitable for the CD-4 system. Before entering into the problems involved in modulation, it is first necessary to devote some time to describing the composite signals.
If full compatibility is to be maintained, the following requirements must be met by the four separate signals, L_F, L_B, R_F and R_B which corresponds to (A).

1. In stereo playback, none of the four signals must be lost. The left signals, L_F and L_B, must be reproduced from the left channel speakers and

the right signals, R_F and R_B, must be reproduced from the right channel speakers. There must be no crosstalk or phase difference between the left and right channel signals, as this would cause the expansion of the sound field and the focus of the sound images to deteriorate. Therefore, the left and right signals must be transmitted discretely, that is independently of each other, and with the same phase.

2. In mono playback, none of the four signals should be lost.

The simplest signal composition which satisfies these requirements is:

	Base band	Carrier band
Left channels	$L_F + L_B$	$L_F - L_B$
Right channels	$R_F + R_B$	$R_F - R_B$

The simplicity inherent in this signal composition guarantees that the cost of the recording and playback equipment will be minimized.

With angular modulation, the variation in amplitude is very small when the carrier is recorded on the disc record, so that this system has advantages with regard to the cutting operation and the record's resistance to wear, if the most appropriate cutting level is determined. Also, as the demodulated output is dependent only on the angular deviation, the playback sensitivity of the pickup cartridge has no influence. The next thing to be decided was the carrier frequency to be used. This had to be determined taking into account the upper limit of the frequencies to be transmitted.

We thought it reasonable to regard 15 kHz as the upper limit of the audio signal because of the frequency response of the human ear. After making this judgement, it became apparent that the frequency of the carrier to be subject to angular modulation would have to be 30 kHz or more.

On the other hand, as the carrier frequency was increased, cutting would become more difficult and there would be increased interference from the base band signals. After considering these practical factors, we determined 30 kHz to be the most appropriate carrier frequency. Therefore, the composition of the CD-4 signal is:

Base band	0-15 kHz
Carrier	30 kHz ±15 kHz

The required bandwidth is up to 45 kHz, but of this, the section between 15 kHz and 20 kHz is necessary for the filter in the playback system which separates the carrier signal from the composite signal. This section should not be regarded as part of the signal bandwidth.

However, this does not mean that frequencies between 15 kHz and 20 kHz are eliminated in recording. If the cut-off characteristic of the filter is good

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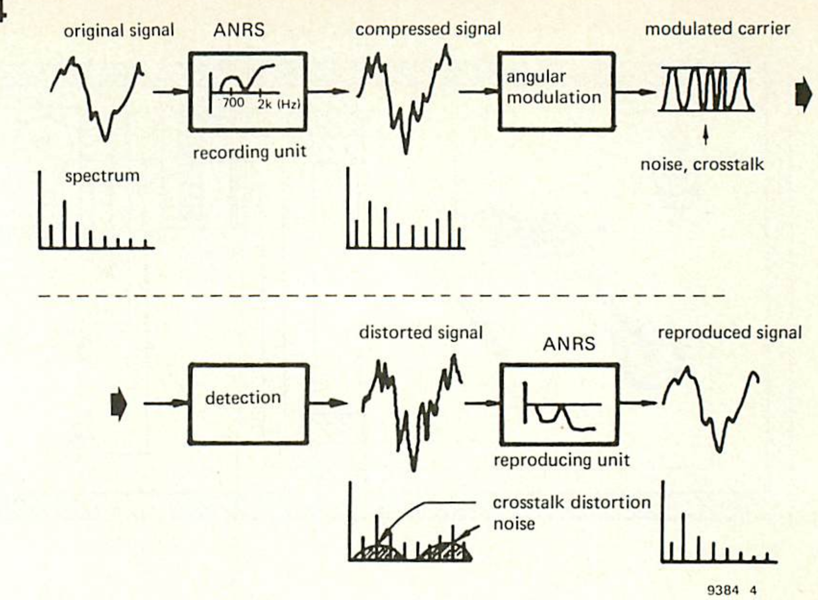

ANRS

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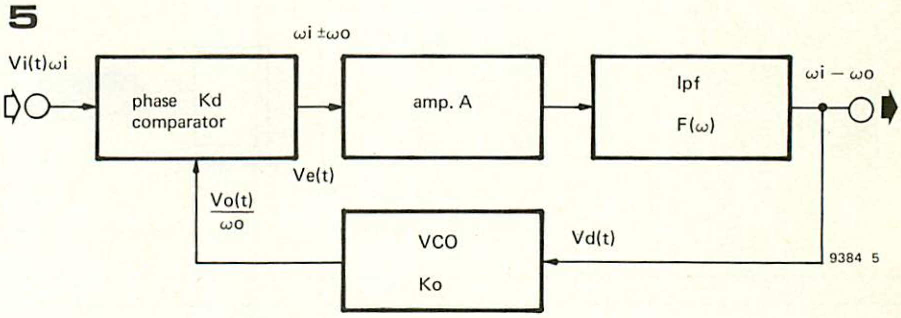

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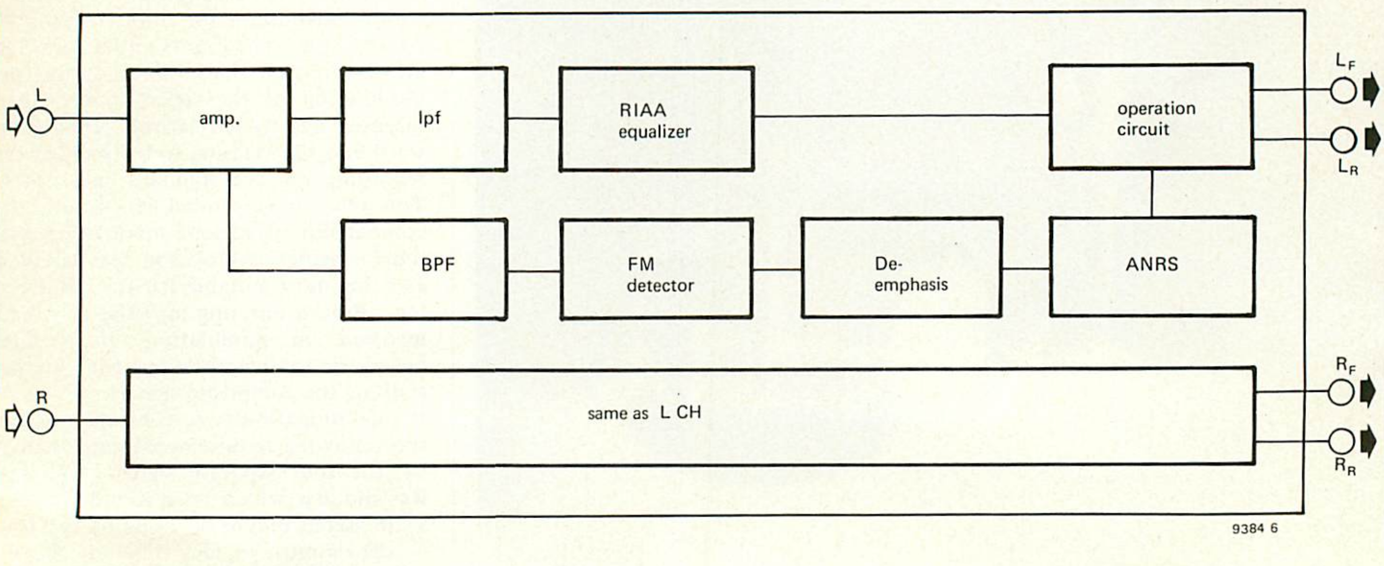

CD-4 DEMODULATOR BLOCK DIAGRAM

enough, components with these frequencies can be utilized.
It was determined that the carrier level should be 19 dB lower than the base band signal. Figure 2 shows the bandwidth structure of the CD-4 record.

CD-4 system technology

CD-4 records which cover a wide bandwidth of 45 kHz require correspondingly broadly based technology. Stating these in the order in which they are required:

1. Required:
   Signal superimposition techniques
   Solutions:
   – the various parameters of the angular modulated signal were established
   – wide range modulator was developed
2. Required:
   Cutting techniques
   Solutions:
   – the use of 1/2 speed cutting mode was adopted
   – the cutting stylus was improved
3. Required:
   Techniques to improve playback sound quality
   a. pickup of superimposed signals
   Solutions:
   – carrier level control recording system
   – Shibata stylus
   b. prevention of tracing distortion
   Solutions:
   – Neutrex I
   – Neutrex II
   c. improvement of S/N and carrier crosstalk distortion
   Solution:
   – ANRS
   d. stabilization of carrier demodulation
   Solution:
   – PLL demodulation
4. Required:
   Related techniques
   a. reduced cost of playback equipment
   Solution:
   – Development of IC
   b. control of phase characteristics of record/playback transducers
   Solution:
   – pulse train measuring method
   c. absolute measurement of record cutting amplitude and crosstalk
   Solution:
   – double-beam interference fringe observation

These techniques are fully described in the literature given in the bibliography at the end of this paper. Here, we would like to select from these techniques those which affect the tone quality and cost.

The pickup cartridge

The pickup cartridge is a very important link in the chain, and is a key item because of its influence on playback sound.
It must cover all frequencies up to 45 kHz; apart from this, it must:

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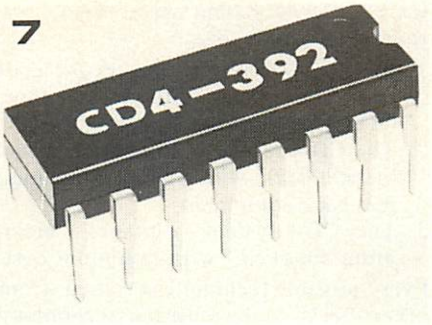

1. not change the playback characteristic from the edge of the record to the center of the record,
2. maintain the same playback characteristic when changes occur in the ambient temperature,
3. not damage the record groove.

Also, as the carrier must be picked up with as little loss as possible, the radius of the stylus tip must be reduced to about 7 microns. This was why the whole subject of stylus design was rethought, resulting in the invention of the Shibata stylus. Figure 3 is an enlarged view of this stylus.
Almost all the problems which we had considered to be the bottleneck imposed by the stylus were solved by increasing the area of contact of the stylus tip and the walls of the record groove. In 1974, a new, bonded Shibata stylus was developed. In this stylus, titanium is bonded to the diamond tip. This stylus has exactly the same performance as the stylus made of diamond alone; the advantage is that only 1/20th the amount of diamond is used in the bonded stylus when compared with the diamond stylus. The result is that low cost Shibata styli are now being mass produced. As well as the Shibata stylus, several other kinds of stylus have been developed with the same increased area of contact with the record groove. By putting these into practical use, the world's leading manufacturers of pickup cartridges have released many cartridges with CD-4 applicability (see 'Market' – Ed.).
The group delay characteristics of the pickup cartridge and cutter head are physical factors which, unless they are understood, make the handling of FM signals correctly impossible. However, they were unknown until the pulse train measurement method was developed. The fact that the group delay characteristics can now be controlled and optimized when this measurement method is used has greatly contributed to the improvement in CD-4 sound.

Neutrex

Apart from those kinds of distortion which can be eliminated by improving the performance of the pickup cartridge, there is a kind of distortion which cannot be eliminated as it is inherent in the system.
For example, tracing distortion resulting from the tracing of the base band interferes with the tracing of the carrier, degrading the sound quality and channel separation however good the performance of the cartridge. To cope with this, Neutrex was developed for use in the CD-4 system.
Neutrex I modifies the shapes of the cutting waveform to be complementary to the tracing distortion waveforms. Neutrex II performs reciprocal modulation of the component of the carrier which would be modulated by the base band signal because of tracing. The optimum combination of these two Neutrex systems effectively suppresses distortion.

ANRS

As well as these kinds of distortion there is also crosstalk distortion and triangular noise which is a result of the superimposition of the angular modulated carrier.
The former occurs because of interference between the two carriers. The frequencies at which this distortion occurs are almost pre-determined and the amount of this distortion is directly related to the amount of crosstalk. The latter increases in frequency ranges where the demodulator output is high. To effectively eliminate these kinds of distortion, ANRS (Automatic Noise Reduction System) was adopted; this functions so as to be frequency selective. Its operation is shown in figure 4.
In this context, the adoption of the angular modulation system for the CD-4 system was helpful. Since the demodulated output depends on the angular deviation alone and not the carrier level, ANRS functions correctly regardless of the pickup cartridge used as long as the cartridge picks up the carrier. As ANRS does not modify the base band signal, it has no effect on compatibility.
Recent progress in pickup cartridge technology has made possible a separation of 25 dB in the carrier band. Because of this and the effects of ANRS technology, crosstalk distortion has ceased to present a problem. With regard to noise, the improvement of the plating process, the record material and cartridge tracing ability and the use of PLL demodulation has made the noise reduction effect of ANRS more stable and more reliable. For all these reasons, the noise characteristics of CD-4 are now very close to those in 2-channel stereo.

PLL

The next subject to be introduced is PLL. This is an abbreviation for Phase Locked Loop, as is widely known. It is a feedback system, as shown in figure 5, which produces an output voltage which corresponds to the momentary frequency of the input signal. In this system, frequency trackability is not degraded by a decrease in the level of the input signal. The PLL circuit used in the demodulator allows the angular modulated carrier to be demodulated while maintaining a good S/N ratio.
By adopting the PLL demodulation system, it has become possible to play

CD-4 records with no instability, even when the record is worn and the cartridge has inferior sensitivity. Furthermore, the PLL has simplified the demodulator circuit by making many L and C elements unnecessary.

Demodulator ICs

As was shown in figure 2, the structure of the signals recorded on the CD-4 record is very simple; the fact that the demodulator can also be greatly simplified can be seen from the block diagram in figure 6.

Demodulator ICs were developed jointly by Signetics Inc. and JVC and independently by QSI Inc. in the U.S.A. following this block diagram. Figure 7 is a photograph of the CD4-392 demodulator IC developed jointly by Signetics and JVC and figure 8 is a photograph of the CD-4 demodulator using this IC. After the results of ICs developed by these companies had been announced, Hitachi completed its development of a demodulator IC; now several manufacturers are developing IC demodulators. The result of integration of the demodulator (including PLL, ANRS and even disc preamp!) into a single IC is that the production cost and size of the CD-4 demodulator component have been greatly reduced. Now, after a great deal of effort, the CD-4 system has become much more easily available to users.

Conclusion

In this paper, the policy and technology of the CD-4 system have been presented. To summarize:

1. In the CD-4 system the record is of the same quality as the master tape; (A) = (B).
2. The CD-4 record is compatible when played back with stereo and mono playback equipment.
3. The CD-4 system combines maximum simplicity with minimum cost.

Every possible technique was used, from other fields of engineering technology wherever and whenever necessary, to satisfy these basic requirements.

As was mentioned at the beginning of this paper, as far as the musicians and record producers are concerned, the 4-channel tape is the result of their art. When software is exchanged between any of the world's record manufacturers, it is done using this master tape. The relationship (A) = (B) shows the goal, perfect fidelity in recording and playback. The development of the CD-4 system and CD-4 records has been a quest for this ideal. The fact that this has been combined with items 2 and 3 in one system is one of the strong points of CD-4.

Summing it up as briefly as possible: CD-4 has one aim. This is a frontal challenge to achieve a perfect disc record system incorporating the recording and playback equipment, which will meet the three requirements stated above. Our basic philosophy, (A) = (B) will, we feel sure, have maximum appeal to both lovers and producers of music.

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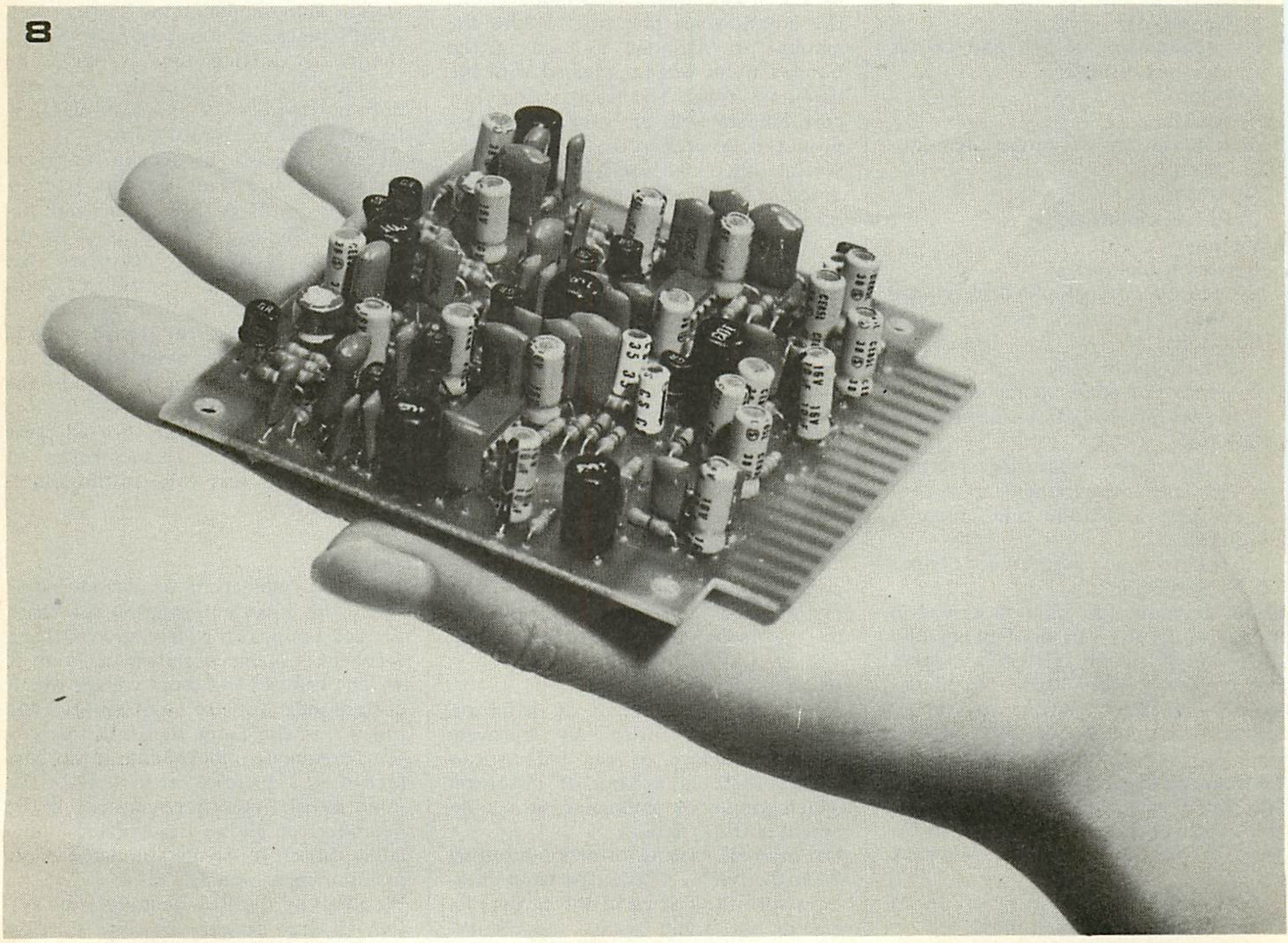

Victor Company of Japan, Limited (JVC)

cd4 - 392

Matrix & audio amplifiers	
THD (V_O = 1.5 V RMS)	: < .05%
Equiv. input noise voltage	: < 2 μV
Gain balance	: < 0.2 dB
Output swing	: > 3 V RMS
Carrier recovery system	
Sensitivity (30 dB quieting 3% deviation)	: < 200 μV
Distortion (± 20% deviation)	: < 0.2%
S/N (V carrier = 20 mV, ± 20% dev)	: > 70 dB
PLL freq. drift with temp	: < 200 ppm/°C

Table 1. Typical CD-4 Demodulator Performance (Vcc = 12 V).

As most quadro-enthusiasts will know, an integrated demodulator for CD-4 has been available in the retail trade for several months now: the CD4-392.
In this article, we are pleased to present all relevant information concerning pinning and specifications. A practical circuit using this IC is included.
We received this article one day before going to press, so we are presenting it as received from JVC — with their original drawings.
—Ed.

At present in Japan 8 record companies are releasing CD-4 discs on 31 labels and 750 albums are available. People throughout Japan are enjoying a wide variety of music from CD-4 records.
In America, 350 CD-4 albums are available on 13 labels including those of the RCA and WEA groups. Recently the A & M label with its excellent reputation in the field of popular music has joined the CD-4 family. We expect that the number of CD-4 releases will grow in the future. Supporting this, CD-4 playback equipment has been greatly improved by the enhancement of the fidelity of pickup cartridges and demodulators. Initially CD-4 playback equipment was designed for incorporation in big console-type stereo systems; now the ground-work for its incorporation in component systems has been completed. The introduction of a low-priced demodulator will make available high performance playback equipment in a price range which will make it more popular. This has been achieved after a year of cooperation between JVC, the inventor of the CD-4 system, and Signetics, one of the world's leaders in linear IC technology.
The CD4-392 single monolithic IC has two basic functions, a carrier recovery system and an audio processing system. This monolothic IC's parameters are sufficient to allow the user flexibility in the design of either high performance or minimum cost demodulators.

Features of the CD4-392 IC chip

The CD4-392 IC chip developed for CD-4 playback offers the following advantages.

1. Versatility and wide range of applications. The CD4-392 IC can be used in a number of design configurations, either low-priced for consumer use or high-priced for professional applications. This IC is designed to be adaptable to newer methods of carrier recovery which may be introduced in the future.
2. Automatic compensation for carrier dropout. CD-4 demodulators using CD4-392 ICs can be designed to compensate automatically for unexpected carrier dropout and for other undesirable input conditions. The carrier level is also automatically adjusted for cartridge output levels from 1 to 7 millivolts.
3. High performance combined with economy. The performance of a typical CD-4 demodulator is shown in table 1.
   Each block on the integrated circuit is designed for lower noise and distortion and wider dynamic range than previous circuits; this was considered essential if the degree of demodulator performance demanded today was to be realized. Inputs and outputs of the circuit blocks are designed to have high and low impedances respectively. Gain, balance and signal level at all block terminals have been established so that external components such as filters and equalizing networks can be simplified. The CD4-392 IC is of the standard 16-pin configuration and two are required for a complete demodulator. The pin configuration is shown in figure 1.

Description of the IC

Figure 2 is a block diagram. The single monolithic chip contains two basic systems, a carrier recovery system and an audio processing system. The carrier recovery system consists of a limiter amplifier, a PLL and a synchronous detector. The PLL includes a phase detector, lock range tracer, VCO (voltage controlled oscillator) and audio amplifier. The audio processing system consists of an automatic noise reduction system (ANRS), its driving amplifier and a matrix circuit. A regulator provides stabilized power for the IC. Lock range characteristics of the PLL are shown in figure 3. These are extremely wide, the DC lock range characteristic being some 20 dB wider than the AC characteristic. Such a wide range is unusual in PLL systems and allows correct synchronization with any input con-

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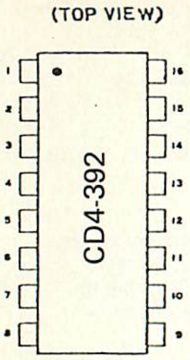
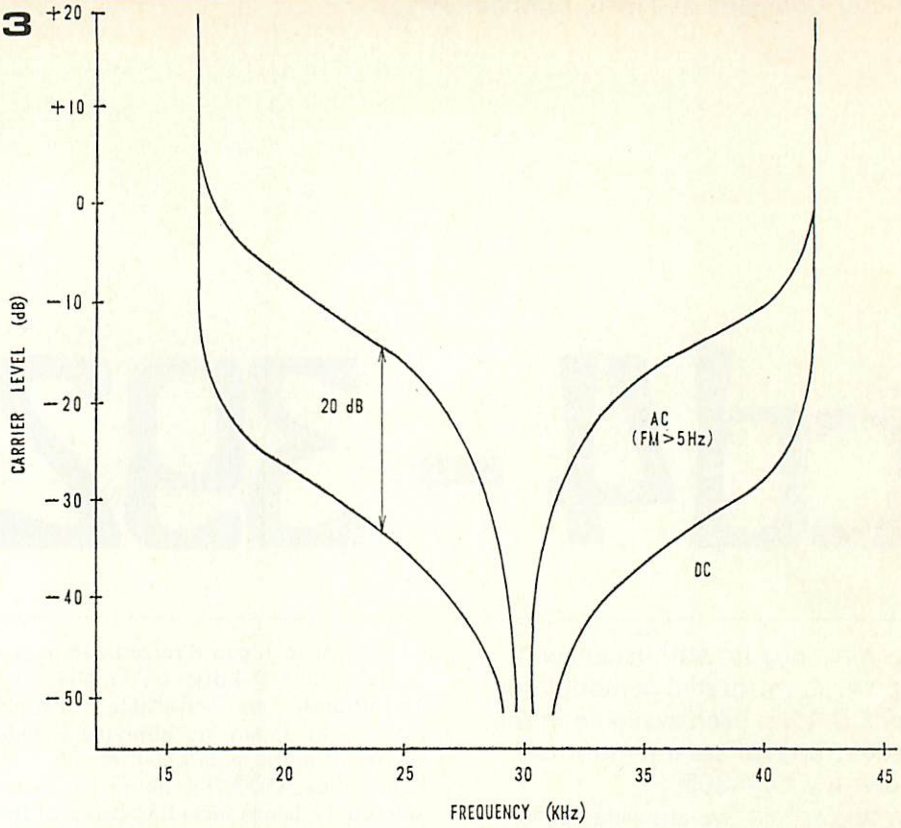


1. ANRS-2 INPUT
2. LOCK RANGE CONTROL
3. LOCK RANGE CONTROL
4. LIMITER INPUT
5. LIMITER OUTPUT
6. +VCC
7. SYNC. DET. OUTPUT
8. VCO CAPACITOR
9. GROUND
10. FRONT OUTPUT
11. MAIN INPUT
12. REAR OUTPUT
13. ANRS CONTROL
14. ANRS-1 INPUT
15. ANRS-2 OUTPUT
16. DEMODULATED OUTPUT

3



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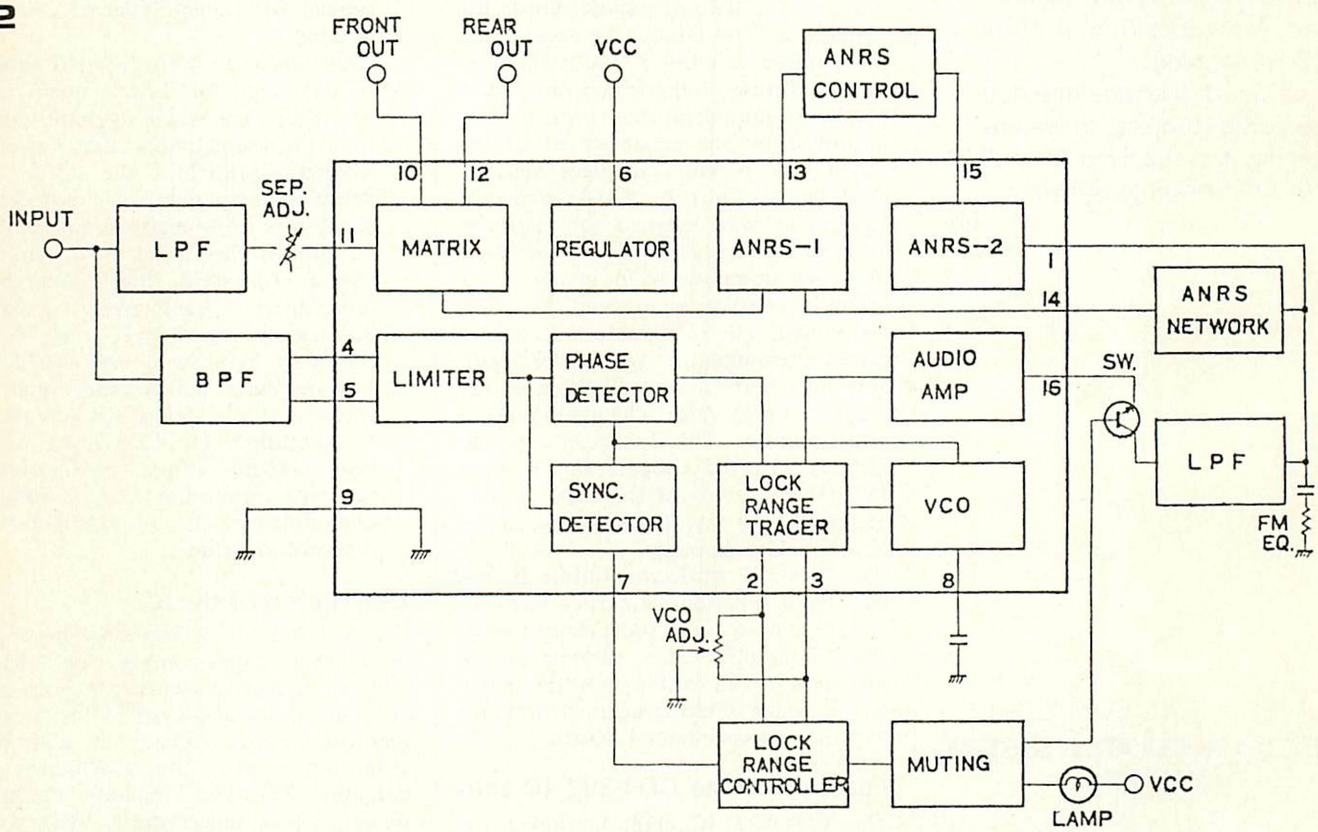

ditions which could occur in practice. Even if a CD-4 disc is inadvertently played back at 45 rpm, the resultant transposed carrier (40.5 kHz) will be within the locking range of the system. Figure 4 shows the quieting curve of the carrier recovery system. There is an S/N of 72 dB from 6 kHz deviation and ANRS improves this ratio by 13 dB for a total S/N of 85 dB, sufficient for professional use.

To prevent interference between the carrier recovery system and audio processing system which are integrated in the single CD4-392 chip, a VCO circuit which oscillates with low current and voltage and which is highly stable was adopted. Figure 5 is a block diagram of this circuit. The VCO consists of a pair of transistors, Q2 and Q3, the emitters of which are common. The transistors switch ON and OFF alternately and repeatedly. The drive circuit connected to a common point between the emitters of these transistors operates in response to a control signal controlling current i_1, thereby driving the transistors. The output is taken from the base potential of transistor Q3. This base potential varies between two values in accordance with the alternating ON and OFF states of the pair of transistors. The charging and discharging currents

Figure 1. Pin configuration of CD4-392 IC.

Figure 2. Block diagram of demodulator using the CD4-392 IC.

Figure 3. AC/DC lock range characteristics of PLL.

Figure 4. Quieting curve of carrier recovery system.

Figure 5. Schematic diagram of voltage controlled oscillator.

which are of the same value are applied to a capacitor connected to the base of transistor Q2. The pair of transistors are switched ON and OFF in response to the charging and discharging of the capacitor via the current mirror circuits connecting the pair of transistors. The control signal controls the oscillation frequency of the linear voltage controlled oscillator.

Circuits external to the IC

The IC has been designed so that a number of approaches to ancillary circuitry can be accommodated.

1. Band-pass and low-pass filtering.
   Either passive LCR or active RC devices can be used.
2. RIAA Equalization
   Normally, the RIAA circuit is divided into two sections, LF boost and HF roll-of, with the feed to the carrier recovery system taken before the HF roll-off. However, as the carrier can be limited by up to 50 dB in this IC, it is possible to take the feed to the carrier recovery system after the RIAA equalizer.
3. ANRS System
   ANRS is an encode-decode noise reduction system and the parameters in playback must match those used in the recording system. Splitting the ANRS into two blocks facilitates a number of approaches to the tailoring of the dynamic characteristics of the ANRS to those desired.
4. Carrier loss compensation
   Carrier loss can result from self-erasure of the HF signal during the cutting process as well as from the

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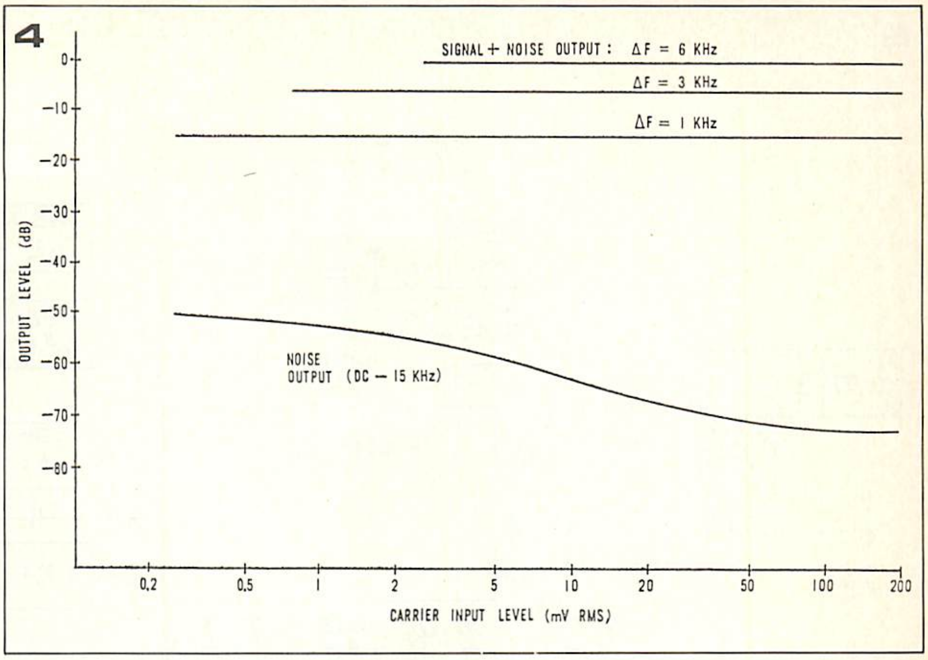

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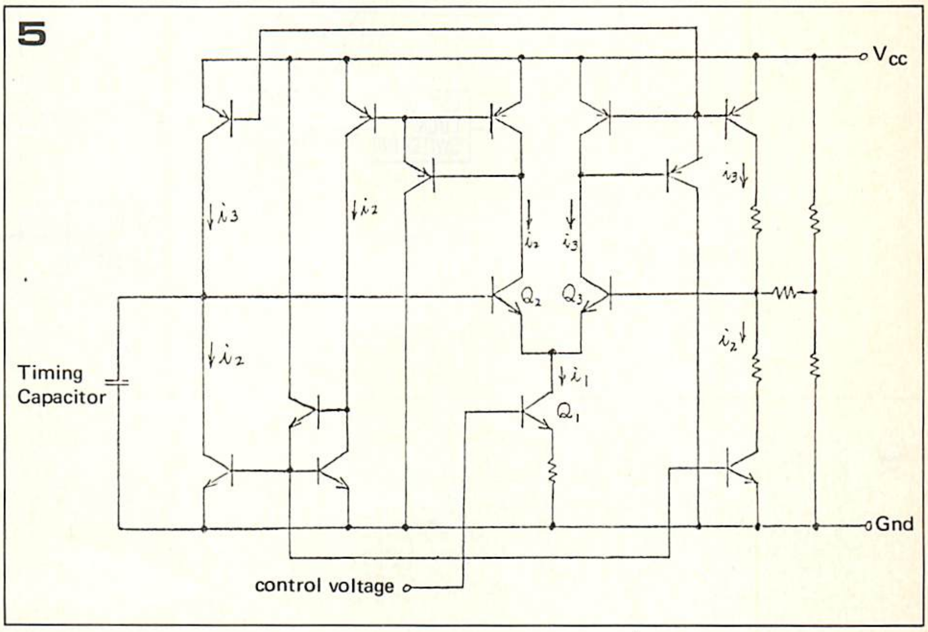

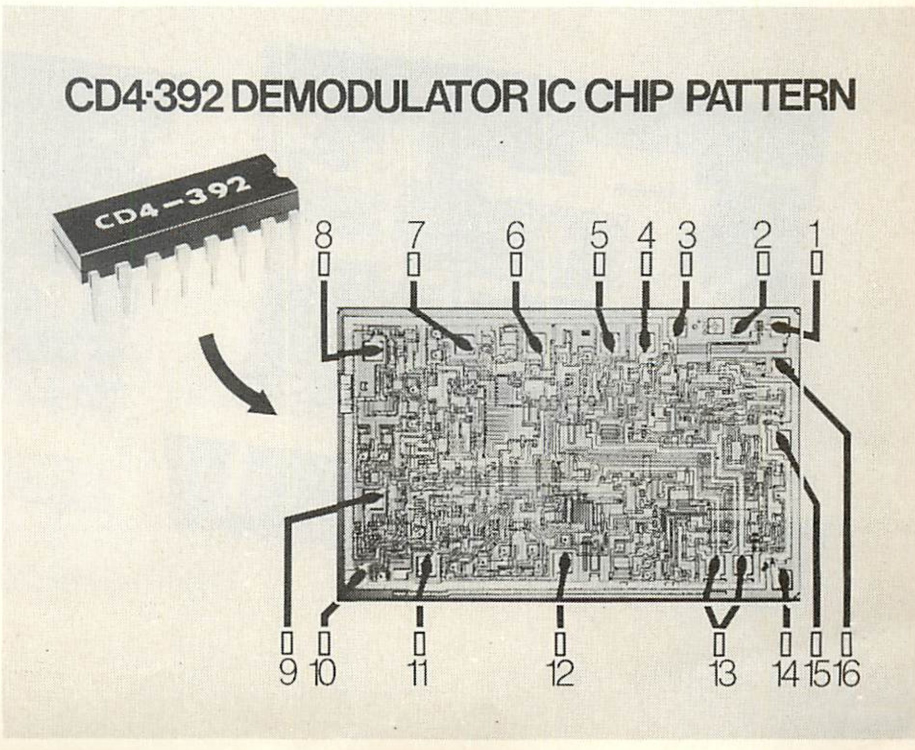

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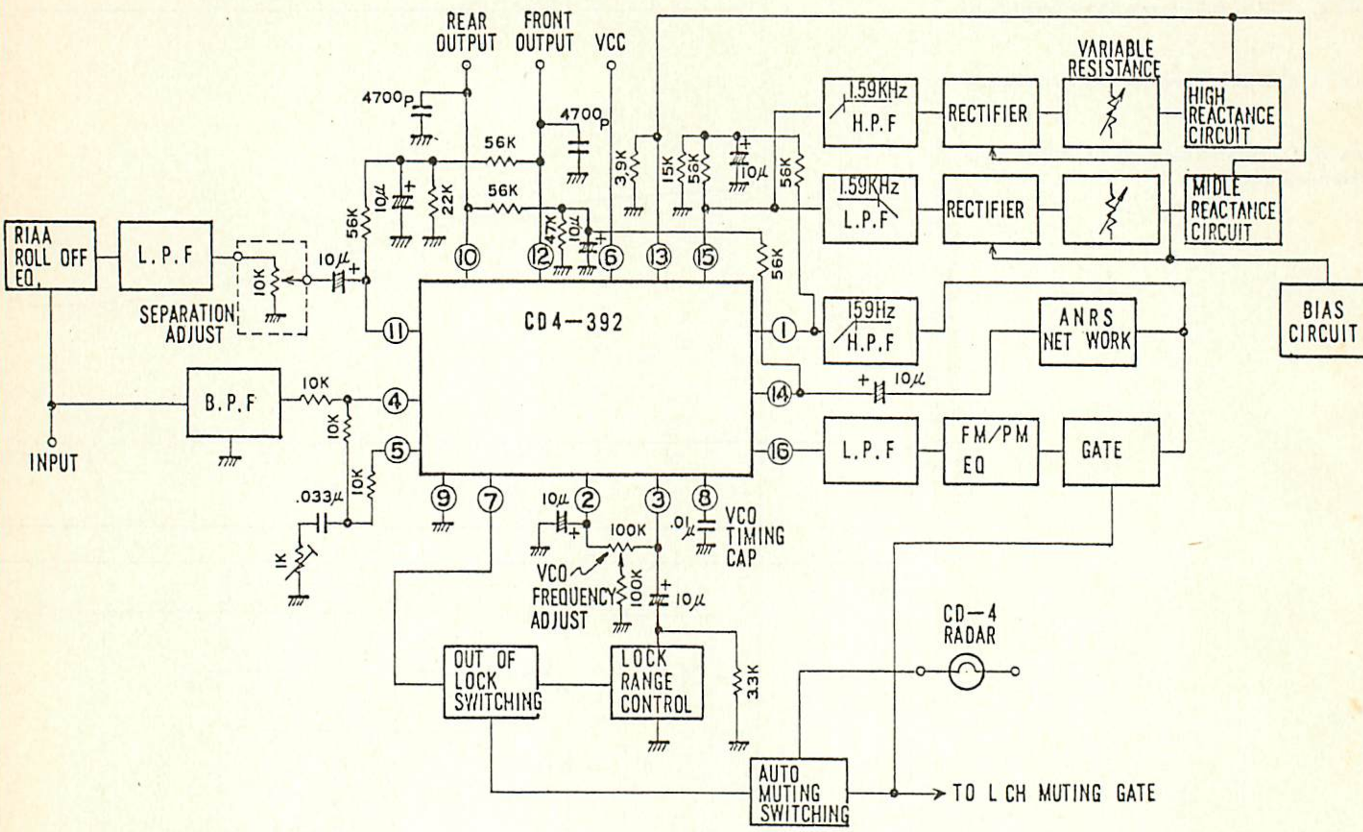
REAR OUTPUT
FRONT OUTPUT
VCC
4700p
4700p
56K
56K
22K
10µ
56K
47K
10µ
3.9K
15K
56K
10µ
56K
1.59KHz H.P.F
1.59KHz L.P.F
RECTIFIER
RECTIFIER
VARIABLE RESISTANCE
HIGH REACTANCE CIRCUIT
MIDLE REACTANCE CIRCUIT
BIAS CIRCUIT
RIAA ROLL OFF EQ.
L.P.F
10K
SEPARATION ADJUST
10µ
CD4-392
159Hz H.P.F
ANRS NET WORK
56K
10µ
B.P.F
10K
10K
10K
INPUT
.033µ
1K
L.P.F
FM/PM EQ
GATE
10µ
100K
.01µ
VCO TIMING CAP
VCO FREQUENCY ADJUST
100K
10µ
3.3K
CD-4 RADAR
OUT OF LOCK SWITCHING
LOCK RANGE CONTROL
AUTO MUTING SWITCHING
TO L CH MUTING GATE

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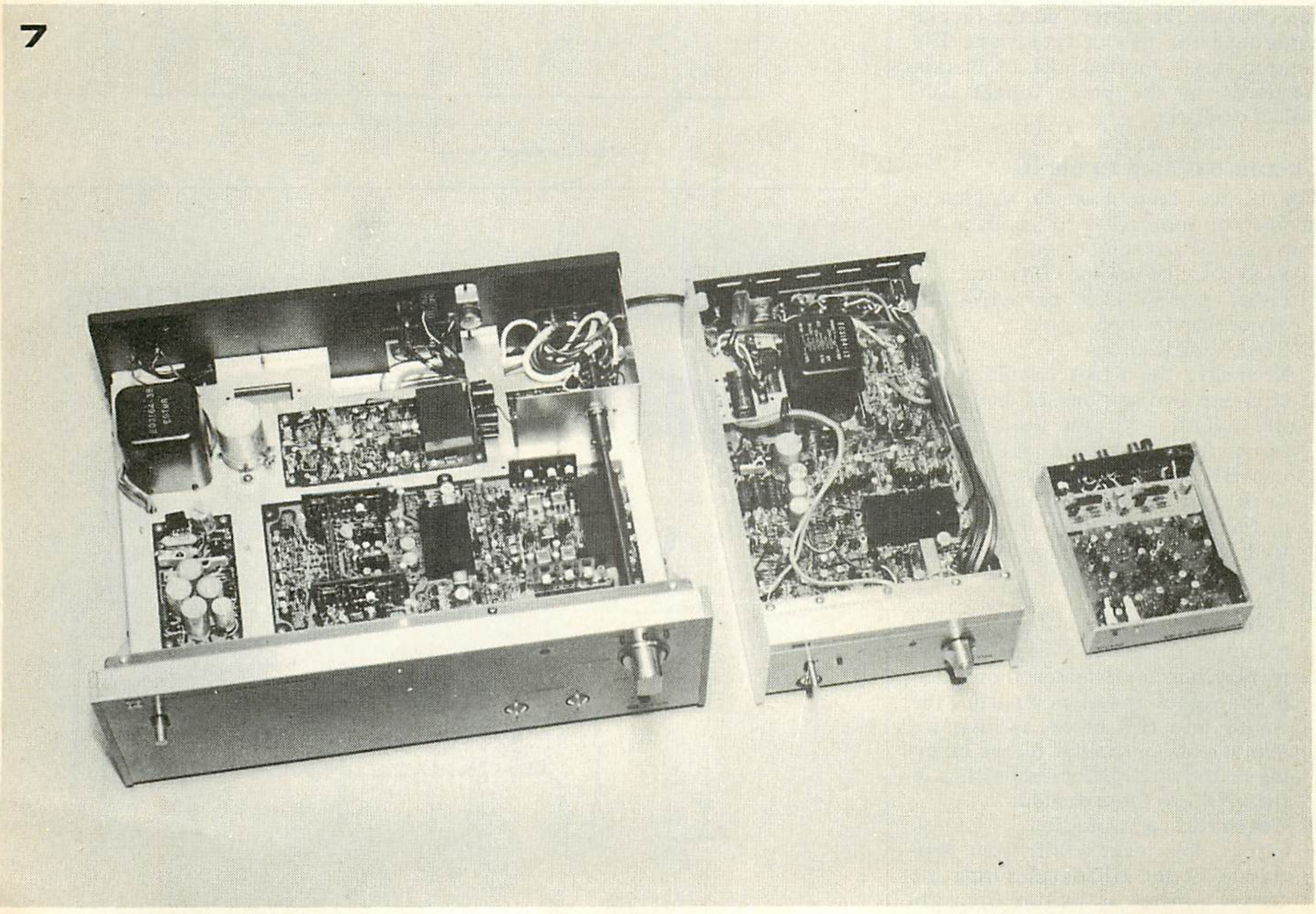


presence of significant harmonic interference from the base band during playback.

The synchronous detector compares the phases of the VCO and the input carrier signal, producing an output signal which accords with the condition of the input signal. This output signal is fed to the lock range controller which controls the PLL so that it is set to the condition most suitable to the input signal, giving a demodulated output which is compensated for carrier loss.

Figure 6 is a block diagram of a standard circuit using the CD4-392.

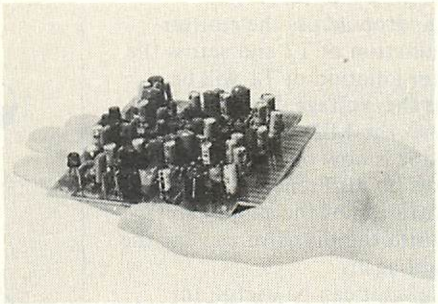
History of the CD-4 demodulator

Figure 7 is a photograph showing the progress made in CD-4 demodulators.

Figure 6. Block diagram of CD4 demodulator.

Figure 7. From left to right: the CD4-1, the 4DD-5 and the TDM-18A.

Figure 8. A complete CD-4 demodulator using the CD4-392 (one channel shown).



The CD4-1 is the first generation demodulator used when the CD-4 system was first released, the 4DD-5 is the second generation demodulator using the PLL IC and the TDM-18A is the third generation demodulator which incorporates the CD4-392 IC.

Figure 8 is a schematic diagram of the standard TDM-19A. The TDM-18A and the TDM-19A represent a significant step forward in the design and evolution of CD-4 playback hardware with their performance characteristics having been substantially improved. ◀

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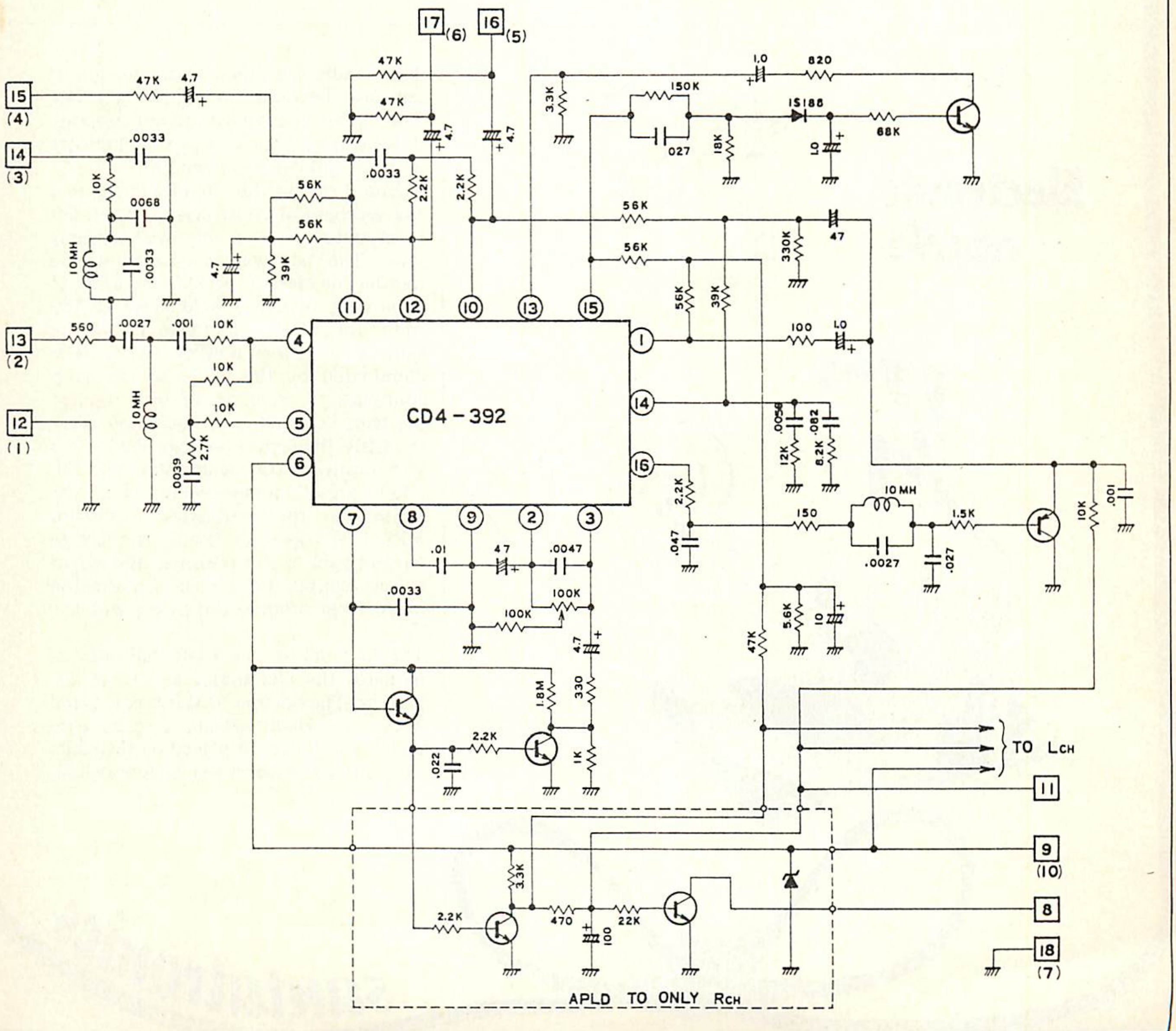
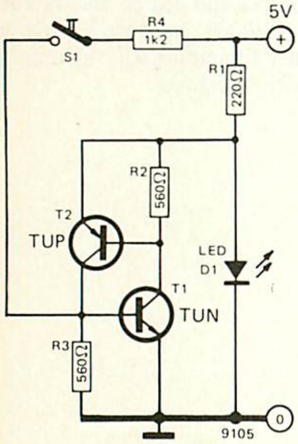
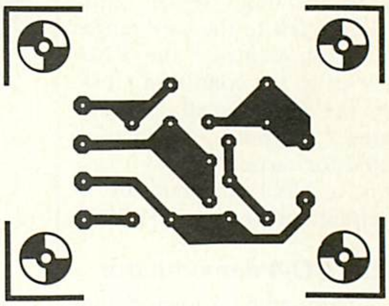


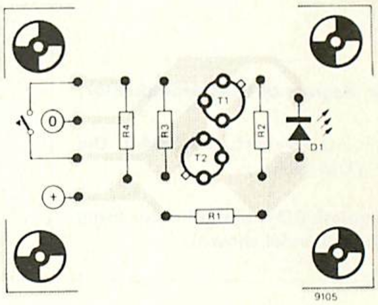
M. Keul

TUT



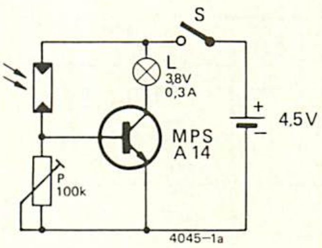
The circuit shows a transistorised universal thyristor, or TUT.
It operates as follows:
When S1 is open, the LED will light when the supply voltage is turned on, because T1 and T2 are both turned off.
If S1 is now closed, T1 receives a base current, so that this transistor turns on and T2 is driven into saturation.
The voltage drop across the emitter-collector junction of T2 and across the base-emitter junction of T1 will be lower than the voltage drop across the LED, so that the LED will extinguish.
The thyristor is now on, and re-opening of S1 makes no difference. Only a very brief interruption of the supply voltage can extinguish the thyristor causing the LED to light again.
This TUT circuit can be useful, for instance, as a mains failure indicator for a digital clock.

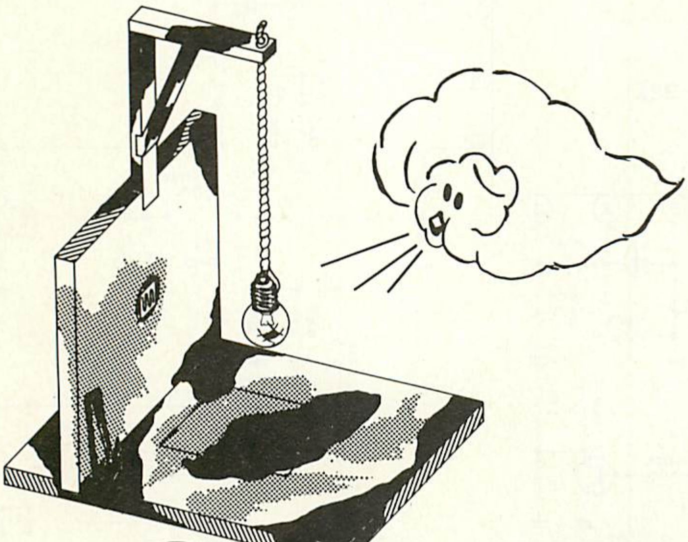




P. Engelmann

Electronic candle





This candle is a simple electronic toy. It can also be used for conjuring tricks. The circuit is designed around an incandescent lamp which can be ignited with a match and can be blown out.
Figure 1 shows the circuit and figure 2 the mechanical construction. The LDR is mounted in the side wall at lamp level. The side wall is covered with a translucent material to hide the LDR. If a burning match is held close to the lamp, the LDR is illuminated and the lamp lights. From now on the LDR is illuminated by the lamp, so the lamp continues to burn. If we blow against the lamp, so that it swings away from the LDR, the lamp is extinguished.
The sensitivity can be adjusted with the 100 k preset potentiometer. For the prototype the darlington transistor MPS A 14 was used. Owing to the high current gain of this transistor the circuit is very simple. Of course, a darlington made from discrete transistors will also do.
The box below the 'LDR-wall' accommodates the electronics as well as the battery. The bottom of this box is fitted with a pin which operates a spring contact when the box is placed on the table. This spring contact is the battery switch.

preamp for counter

In the last issue of Elektor the basic circuit of a frequency counter was described. In this issue a preamplifier to increase the input sensitivity is discussed.

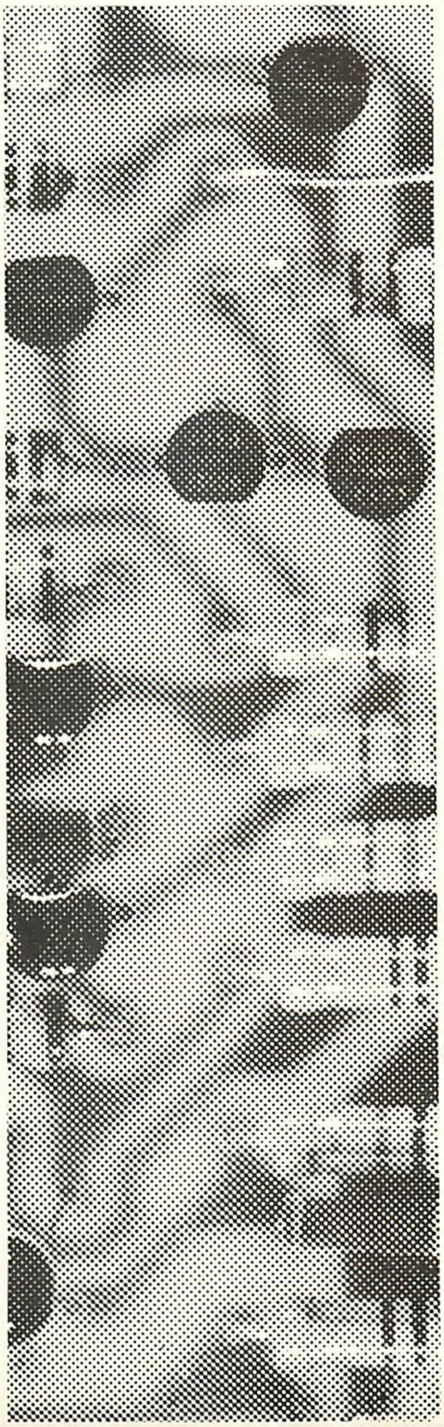
The input sensitivity of the basic frequency meter is inadequate for use in most audio and r.f. circuits where signal levels of at the most a few hundred millivolts are likely to be encountered. It was felt that an input sensitivity of around 10 mV RMS would prove suitable for most applications, and it was with this in mind that the parameters of the preamplifier were determined. The circuit must meet the following specifications:

1. Bandwidth: Greater than the bandwidth of the frequency counter (D.C. - 18 MHz)
2. Gain: 40 dB
3. High input impedance and low input capacitance.

In order to keep the circuit reasonably simple and stable the first criterion was relaxed slightly and the gain rolls off at high frequencies.

The input resistance must be kept high to avoid loading the circuit to which the frequency counter is connected, and the input shunt capacitance must be kept low. In practice an input resistance of 1 MΩ should be adequate for most applications. The input capacitance depends to a large extent on the capacitance of the input leads and the wiring within the instrument.

The complete circuit of the preamplifier is given in figure 1. It consists of three differential stages and an output emitter-follower. The input stage is a differential source-follower. This configuration was chosen because the input FET offers a high input resistance in this mode, and in fact the input resistance of the preamp is almost entirely determined by the 1 M resistor R4. The E420 dual FET has a very low gate-source capacitance and, since both FET's are grown on a single chip, exceptionally good matching and temperature tracking. A further advantage of this type of input stage is that its overload margin is virtually full supply voltage. However the maximum input voltage is clamped to 0.7 V by D1 and D2, whilst R5 limits the current through these diodes. C1 provides some compensation for high-frequency roll-off by shunting R5 at high frequencies. As the preamplifier must operate down to D.C. it is D.C. coupled throughout. However, so that A.C. signals with a large D.C. component superimposed can be measured without the D.C. blocking the amplifier C_X is included in series with the input.



For voltages in excess of 1.5 V p-p, especially from high impedance sources, it is recommended that an input attenuator be used to avoid D1 and D2 loading the signal source when they conduct. D1 and D2 could also be replaced by zeners to increase the maximum input voltage, but if an attenuator is fitted this should not be necessary.

The input stage is followed by two differential stages using bipolar transistors (T2/T3 and T5/T6). The output is taken from the emitter-follower T8. As the frequency counter will not operate correctly with insufficient signal an indication of the output level of the amplifier is desirable. This is provided by T7 and D5. As the signal approaches a level sufficient to drive the counter the signal at the emitter of T7 will also increase and D5 will start to light up. By the time the amplifier is limiting D5 will be glowing quite brightly.

The frequency response of the amplifier is compensated by C3. Up to about 5 MHz an input signal of 50 mV will cause limiting. Above this the gain rolls off until at 18 MHz 100 mV is required for limiting, although 60 mV will produce sufficient output to drive the frequency counter (see figure 2).

When the amplifier is not connected to the frequency counter the output will swing between positive and negative supply (less base-emitter voltage of T8) in the limiting condition. However, as soon as the frequency counter is connected to the output of the preamp the clamping diodes (D2 and D3) in the TTL input circuitry of the counter will limit the maximum negative excursion to about −0.6 V. This output con-

1

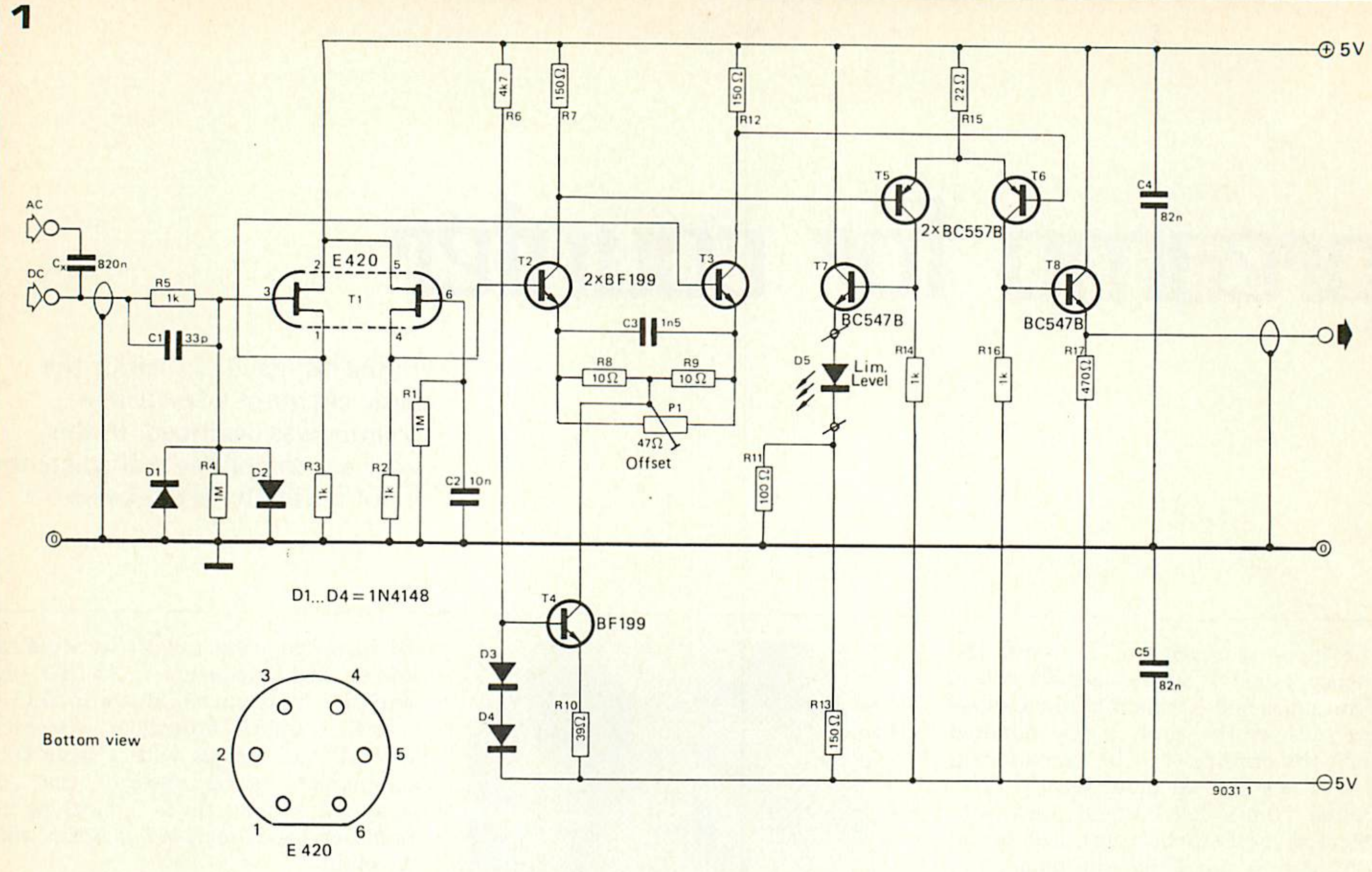


Figure 1. Complete circuit of the input preamplifier.

Figure 2. The frequency response of the preamplifier is flat up to about 5 MHz, and above this frequency it rolls off. The lower curve shows the input voltage required for reliable operation of the counter, whilst the upper curve shows input voltage for full limiting of the amplifier.

Figure 3. Voltage doubler and stabilizer to provide the negative supply required for the preamplifier. This is derived from the existing transformer that provides the +5 V supply for the counter.

Figure 4. Printed circuit board and component layout for the preamplifier.

Photo 1. The completed preamp board.

figuration has the advantage that the logic '0' level is well defined.

Power Supply

The frequency counter requires a single +5 V power supply. The input preamplifier, however, needs a negative supply also. Fortunately, since the current drawn from the negative supply is small it can be derived by a voltage doubler type of arrangement with a simple stabilizer as shown in figure 3. This derives its A.C. input from the existing transformer for the positive supply to the counter.

Construction

Printed circuit boards for the preamplifier and the associated power supply are given in figures 4 and 5 respectively. The only point to note when building the boards is the connec-

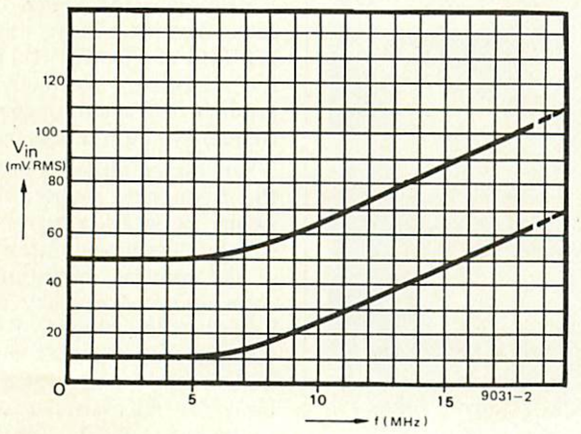
Parts list for figure 1.

resistors:
R1,R4 = 1 M
R2,R3,R5,R14,R16 = 1 k
R6 = 4k7
R7,R12,R13 = 150 Ω
R8,R9 = 10 Ω
R10 = 39 Ω
R11 = 100 Ω
R15 = 22 Ω
R17 = 470 Ω
P1 = 47 Ω, preset

capacitors:
C1 = 33 p
C2 = 10 n
C3 = 1n5
C4,C5 = 82 n

semiconductors:
T1 = E 420
T2,T3,T4 = BF 199
T5,T6 = BC 557 B
T7,T8 = BC 547 B
D1 to D4 = DUS (e.g. 1N4148)
D5 = LED

2



Parts list for figure 3.

R1 = 1 k
C1,C2 = 1000 μ, 16 V
C3 = 220 μ, 10 V
T1 = BC 161
D1,D2 = 1N4002
D3 = zener 5,6 V, 400 mW

tion to the E420 dual-FET as this device may be unfamiliar. The pin configuration of this device is given adjacent to the circuit diagram in figure 1.

Because of the high frequencies involved close attention must be given to the layout of the complete frequency counter. A suitable layout is given in

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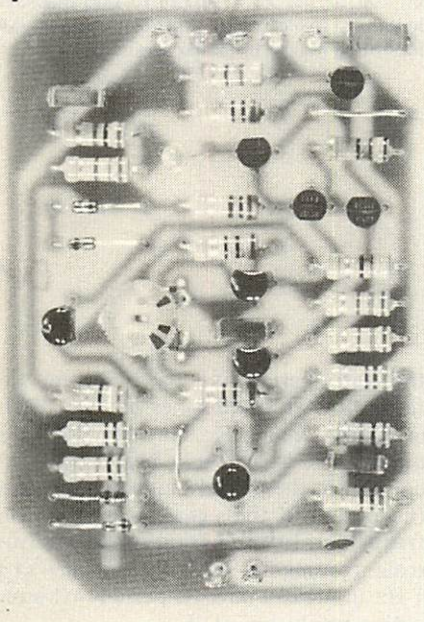
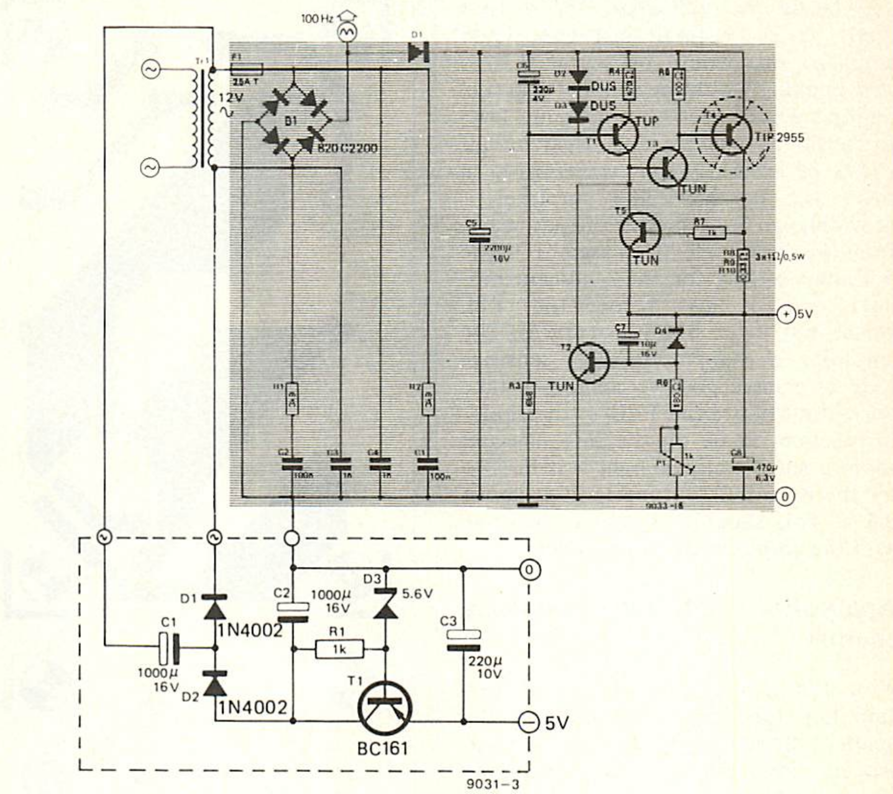


figure 6 and it is recommended that this should be adhered to. In particular it should be noted that all earth connections go directly to chassis and that separate +5 V supply leads are taken from the power supply board to the preamplifier, the control logic and to the display/counter assembly.

The input and output connections to the input preamplifier must be made using screened cable but, in contrast to normal a.f. amplifier practice the braiding of these cables should be earthed at both ends.

3



Preliminary Adjustments

The only adjustment necessary to the input preamplifier is made with the

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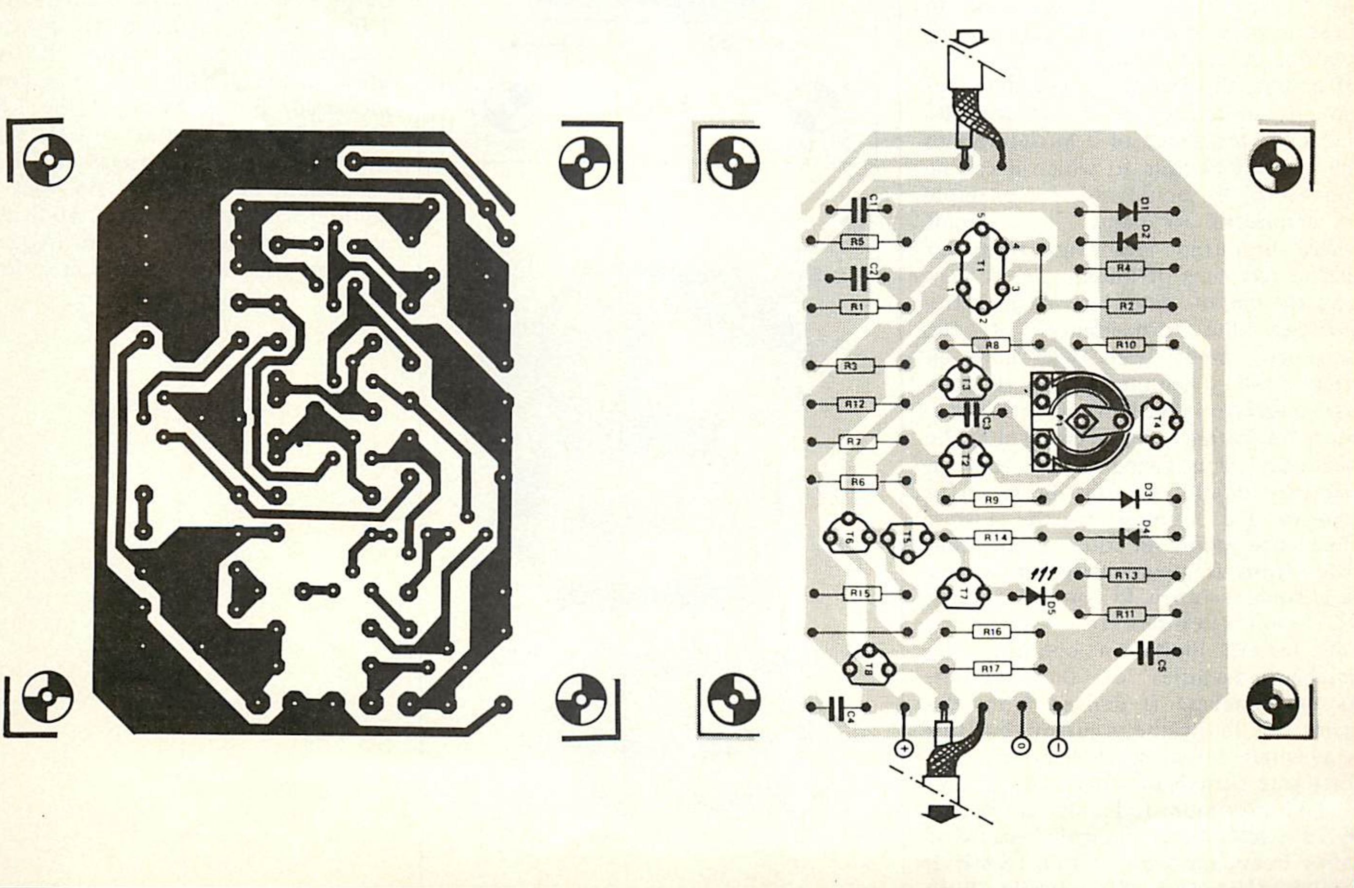
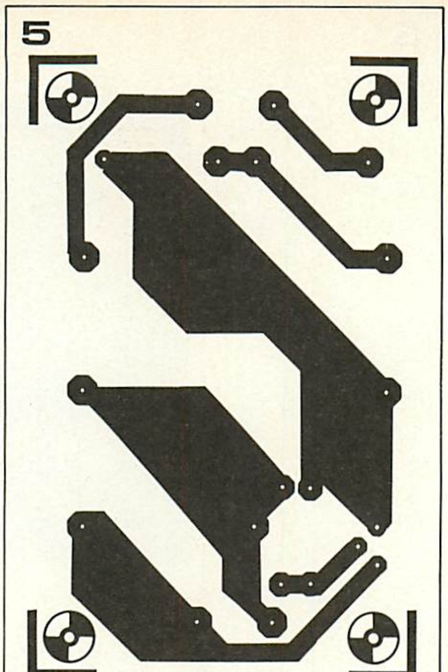


offset control P1. This adjusts the D.C. balance of the second differential stage, and hence the quiescent D.C. output level. In a normal instrumentation amplifier this would be set at 0 V so that clipping would be symmetrical (i.e. limiting would occur at the same level for both the positive and negative half cycles of an A.C. input waveform). In this case, however, the amplifier is providing an asymmetric output waveform (i.e. TTL logic '0' to logic '1'). The optimum setting for the quiescent output level is just below the TTL guaranteed logic '0' level of 0.8 V. The amplifier is then in its most sensitive state as a small positive swing will take the output above the TTL '1' threshold. In practice, to be on the safe side and allow a small noise margin it is best to set the quiescent output level at about 0.5 V. This should, of course, be done with the amplifier input grounded.

Applications of the frequency counter

With the addition of the input preamplifier the uses to which the frequency counter may be put are extended considerably. A few of the applications are:
a.f. circuits – monitoring of oscillator frequency when doing frequency response measurements on amplifiers, filters etc.
r.f. circuits – monitoring output frequency of r.f. oscillators, frequency to which receivers are tuned etc.
PLL circuits – setting up of VCO free-running frequency, particularly useful for stereo decoders.
time measurements – in the period mode the counter can be used to measure time intervals, and may thus be used as a stopwatch.
Of course, the frequency counter does have its limitations. At low frequencies the input resistance of 1 M determines the type of circuits to which it can be connected. It should not, for example be connected to points in a circuit where the output impedance is greater than a few tens of kilohms, as it may load the circuit under test. At high frequencies the capacitance of the (screened) input leads will have an effect, and if connected to the frequency-determining section of an oscillator, for instance, it can easily alter the frequency, thus giving a false reading. Due care should therefore be taken to connect the counter to the lowest impedance point in the circuit, and away from frequency-determining circuits such as tuned LC or RC circuits, RC networks in filters etc.
The second limitation concerns the timebase facilities of the counter. As the timebase is derived from the mains this limits the accuracy, but this is adequate for most applications. The three gate periods of 10 ms, 100 ms and 1 s give maximum full-scale readings of 99.9999 MHz (not attainable because of upper frequency limit of TTL 18 MHz), 9.99999 MHz and 999.999 kHz. With

5



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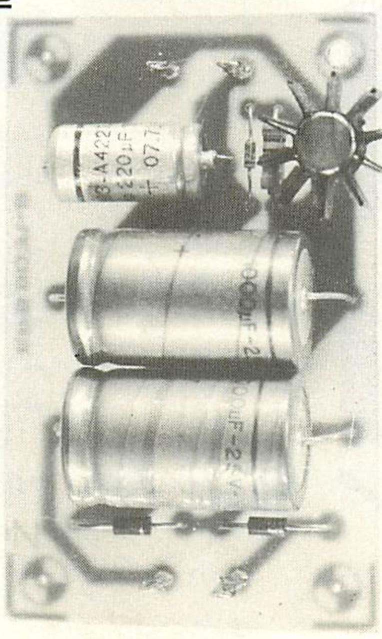


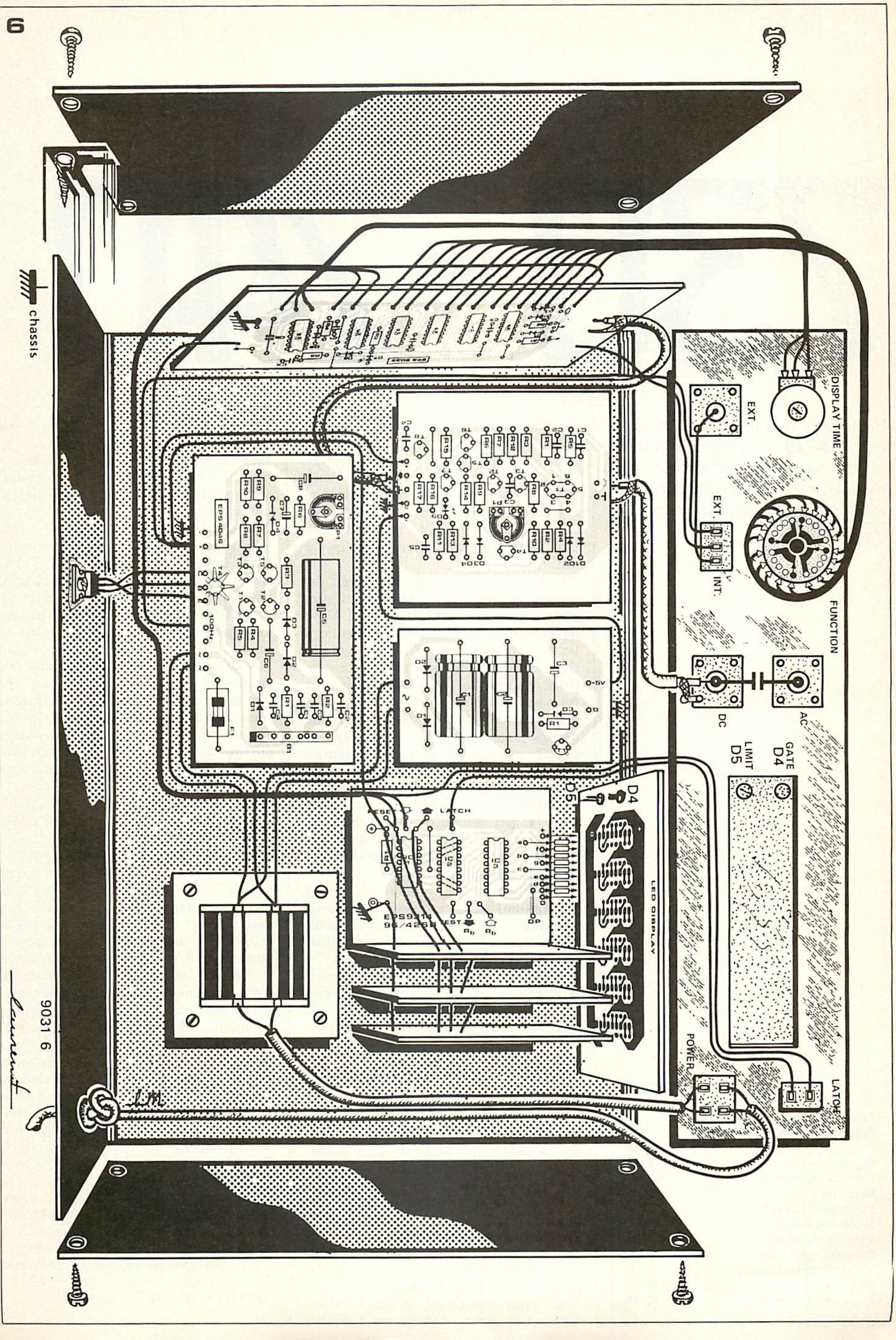
Figure 5. Printed circuit board for the negative supply. As this is the same length as the preamp board the two can easily be mounted side-by-side.

Figure 6. Wiring diagram for the complete frequency counter including the input preamp. It is advisable to adhere strictly to this layout for trouble-free operation.

Photo 2. The –5 V supply can be mounted on top of the +5 V supply to save space. If, however, space is not a problem side-by-side mounting makes for easier servicing.

the gate period set to 1 second the resolution at frequencies below 100 Hz is worse than 1%. At very low frequencies it is probably best to use the counter in the period mode and measure the period of the signal rather than the frequency. In the period mode the full-scale reading is 9,999.99 seconds so a 1 Hz input can have its period measured with a resolution of 1%.
This still leaves a 'hole in the middle' for frequencies between 1 Hz and 100 Hz where the resolution in either the frequency or period mode is worse than 1%. If this is felt to be a problem then the addition of a crystal timebase is worth considering, and a suitable choice is the universal frequency reference published in Elektor No. 5. This has outputs at frequencies from 1 MHz to 1 Hz, and in addition to providing greater accuracy it enables the resolution in the period mode to be greatly increased. For instance, if the 1 MHz output is used to time a 1 Hz signal, then the period can be measured with a resolution of 0.0001% (in fact the counter will just overrange). Addition of a crystal timebase to the frequency counter will be discussed in a future issue.

6


DISPLAY TIME
EXT.
EXT.
INT.
FUNCTION
DC
AC
GATE
D4
LIMIT
D5
LATCH
POWER
LED DISPLAY
D4
D5
LATCH
EPS 4046
EPS 9114
0–5V
chassis
9031 6

730-740

Using only two ICs, the TCA730 and TCA740, a complete stereo control amplifier can be built. An exceptional feature is that the volume, balance, and tone are all DC controlled.

An alternative to the conventional potentiometer control of volume, balance and tone should be more than welcome. The problems connected with running audio signals over potentiometers are well-known: the long cables almost inevitably lead to hum and crosstalk, and 'crackly' potentiometers are notorious . . .
A solution is offered in the circuit described in this article. The Philips integrated circuits TCA730 and TCA740 have built-in 'potentiometers' that can be DC-controlled. The TCA730 contains the electronic volume and balance controls, whereas the TCA740 can be used for bass and treble control.
The necessary control voltages can be derived from a simple voltage-divider circuit incorporating several potentiometers. Since these potentiometers don't have to carry the audio signal, they can be connected to the circuit via virtually any length of cable: the hum pick-up would have to be very severe before it could cause audible modulation of the audio signal.
Another advantage of these ICs is that one (mono) potentiometer can be used to control several audio channels simultaneously, with a minimum of imbalance between the channels.
The circuit described here can be used in combination with almost any preamplifier, and the performance is definitely 'Hi-Fi'.

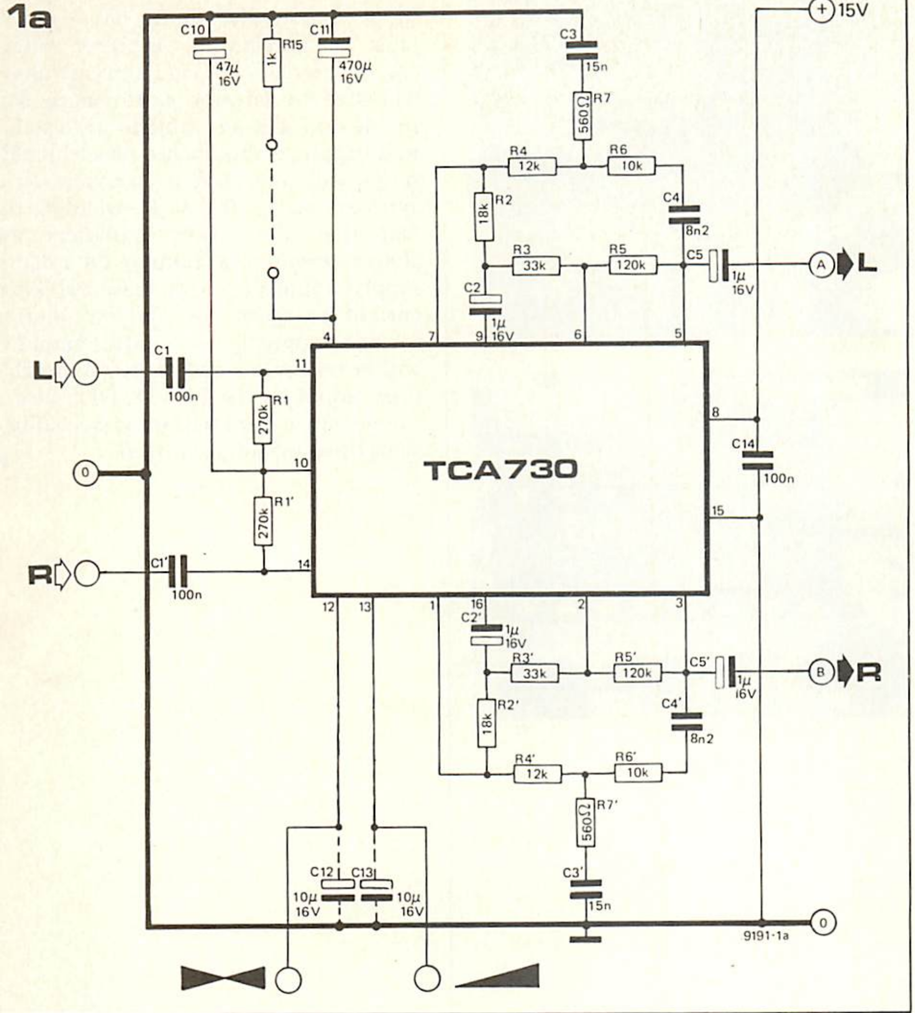
TCA730: volume and balance

The complete stereo control amplifier is shown in figure 1. For convenience, the circuit has been cut in two: figure 1a shows the TCA730 with associated components and figure 1b shows the TCA740. The output of 1a (connections A and B) is connected to the input of 1b.
The first section (TCA730) is the volume and balance control. In the maximum setting of the volume control the gain is x 10: 100 mV in gives 1 V out. This input sensitivity, in combination with the input impedance (250 k), means that the amplifier can be driven direct from practically any receiver, tape recorder or crystal pickup. Microphones or dynamic pickup cartridges will need a separate preamplifier, of course.
The circuit shows the complete stereo version, so that most of the components come in pairs. For instance, R1 (270 k) is the input resistor for the left channel and R1' is its twin in the right channel. The (DC) control voltages for volume and balance control are connected to pins 13 and 12, respectively; both voltages should be linearly adjustable from 1 V to 9 V. Figure 2 gives the circuit of the control potentiometers: four linear potentiometers (10 k) are connected in parallel in a voltage divider circuit that gives the correct control range. Two of these potentiometers are used for volume and balance control. Needless to say, the supply voltage for this control circuit must be well stabilised and smoothed.
If the audio input voltage is 100 mV or less, the volume control has a range from +20 to −70 dB. The balance control range depends in part on the volume setting: when the volume is set at −20 dB or less, the balance control range is +10 to −10 dB, but this range is reduced at higher volume settings. An interesting option is offered at pin 4. If this pin is simply connected to supply common through an electrolytic (C11, 470 μ), the volume control works as normal. However, if a 1 k resistor is connected in parallel with this electrolytic (R15, dotted in figure 1a) a physiological volume control is obtained. It seems unncessary to go into this in any further detail – the effect, also known as 'contour control', is well-known by now. Suffice it to say that in the maximum setting of the volume control (control voltage: 9 V) the frequency response is flat, whereas at a much lower setting (control voltage: 3.2 V) the bass is only 40 dB down and the frequency range from 200 to 7000 Hz is already 70 dB down.

Specifications:

Frequency response (±1 dB):	20-20,000 Hz
Signal-to-noise ratio:	57 dB
Channel separation:	60 dB
Distortion:	0.1%
Input overload level:	1 V
Input impedance:	250 k
Max. output level:	1 V
Output impedance:	4.7 k
Volume control range:	+20 - −70 dB
Max. bass lift/cut:	15 dB
Max. treble lift/cut:	15 dB

1a



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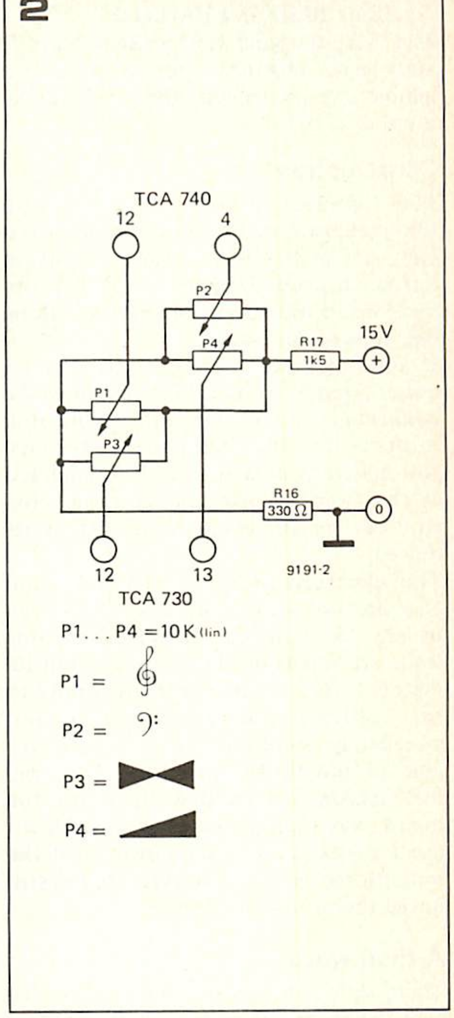


1b

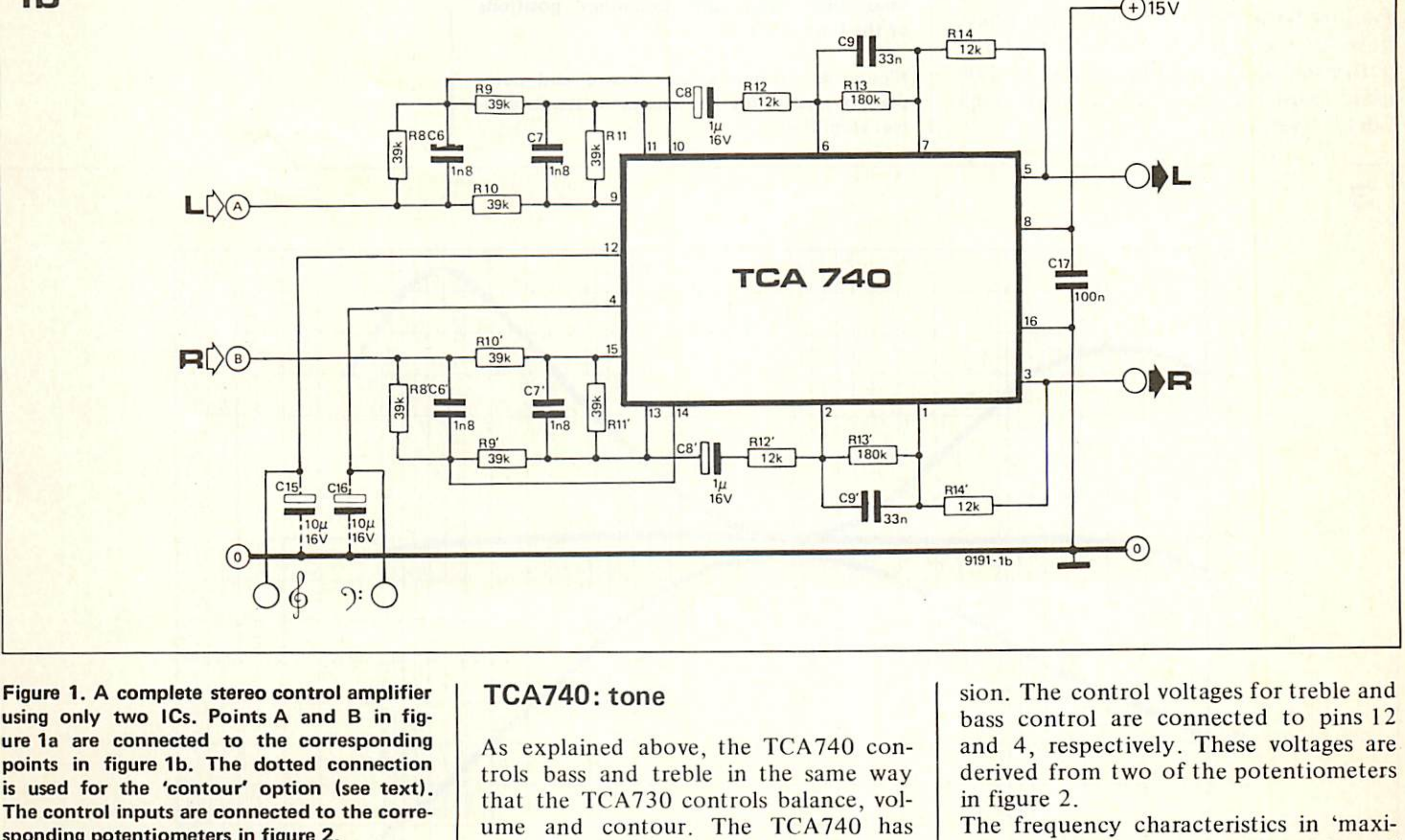


Figure 1. A complete stereo control amplifier using only two ICs. Points A and B in figure 1a are connected to the corresponding points in figure 1b. The dotted connection is used for the 'contour' option (see text). The control inputs are connected to the corresponding potentiometers in figure 2.

Figure 2. The circuit for the control potentiometers (treble, bass, balance and volume respectively). These components are not mounted on the p.c.b.

TCA740: tone

As explained above, the TCA740 controls bass and treble in the same way that the TCA730 controls balance, volume and contour. The TCA740 has unity gain in the 'flat' position of the controls; the maximum signal level at input and output is 1 V.

As with the TCA730, most of the components come in pairs for the stereo version. The control voltages for treble and bass control are connected to pins 12 and 4, respectively. These voltages are derived from two of the potentiometers in figure 2.

The frequency characteristics in 'maximum', 'flat' and 'minimum' positions of the tone controls are plotted in figure 3. Maximum cut and boost is a good 15 dB, both for treble and for bass. The 'flat' response, as measured for our lab-

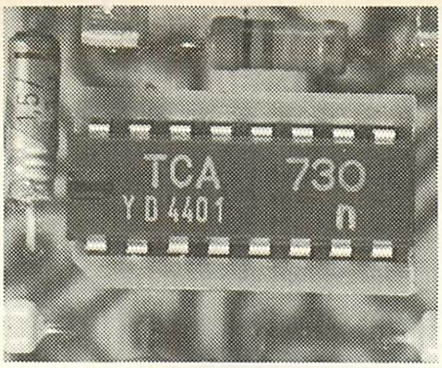
oratory prototype, is definitely flat: −1 dB at 20 Hz and 100 kHz!
The output signal (left channel: pin 5, and right channel: pin 3) can drive almost any power amplifier – the maximum level is 1 V.

Construction

The complete control amplifier, with the exception of the potentiometer circuit shown in figure 2, can be built on one small printed circuit board. All connections to the potentiometers are along one edge of the board.
If physiological volume control is required, pin 4 of the TCA730 must be connected to R15 through a wire link (dotted on the component layout). Alternatively, a switch can be connected at this point so that the 'contour' control can be switched on or off as required.
The electrolytics C12, C13, C15 and C16 are not strictly necessary, and can usually be omitted. However, if long leads are run from the control potentiometers to the boards, or if the supply to the control potentiometers is not adequately smoothed, it can be advisable to add these capacitors. The original reason for putting them on the board was that it makes it possible to use a digital control unit instead of the potentiometers . . . however, that is still in the pre-prototype stage!

A final word

There should be no further need to discuss the technical merits of this control amplifier; the specifications tell the story. For those who are perhaps not so familiar with the technical terminology, however, we can safely state that the performance of this amplifier should be quite satisfactory as part of most high fidelity systems.



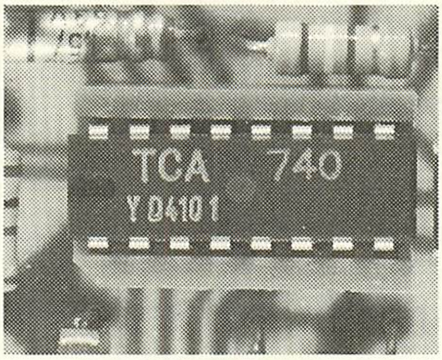
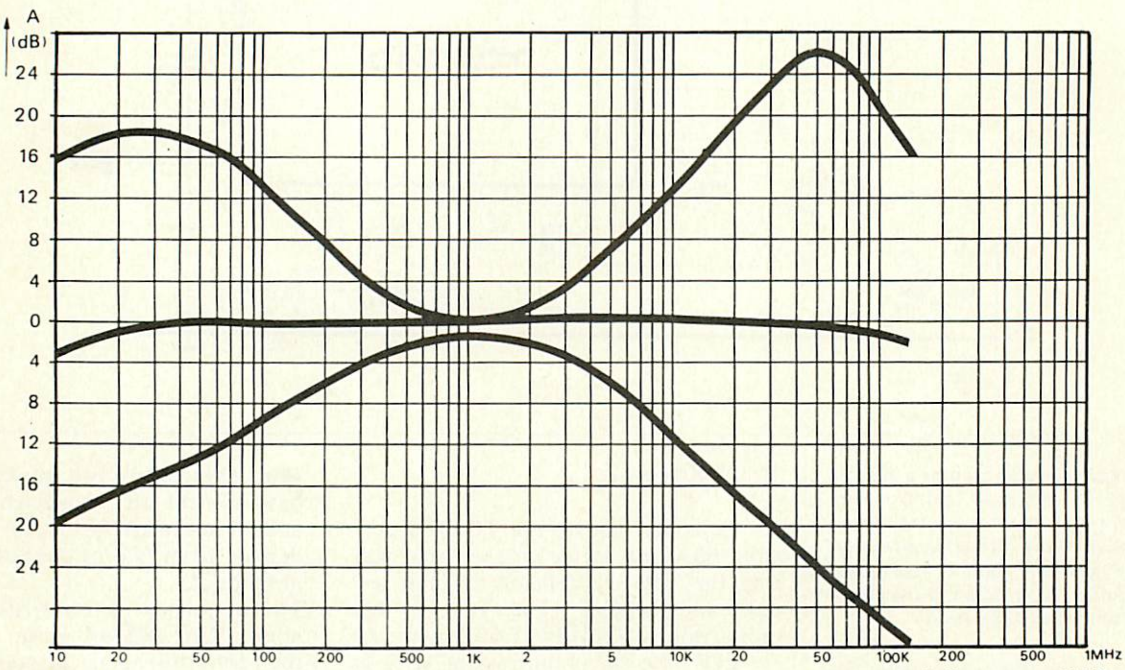


Figure 3. Frequency response curves in the 'maximum', 'flat' and 'minimum' positions of the tone controls.

Figure 4. Printed circuit board and component layout for the complete stereo control amplifier.

A final word on the power supply: th supply voltage given in the circuit (15 V must be adhered to. A higher voltag can destroy the ICs, and a lower voltag will lead to inferior performance. Fo this reason it is advisable to use a stabil ised supply; it should also be adequatel smoothed. The current consumption i approximately 60 mA. Considering th fact that the power amplifiers wil almost certainly be running on a highe supply voltage and will have sufficien current to spare, the simplest solutio for the supply to the control amplifie will be to use a stabiliser IC. A suitabl type would be the LM131. Of course, simple zener stabilisation with adequat smoothing would do instead.

3



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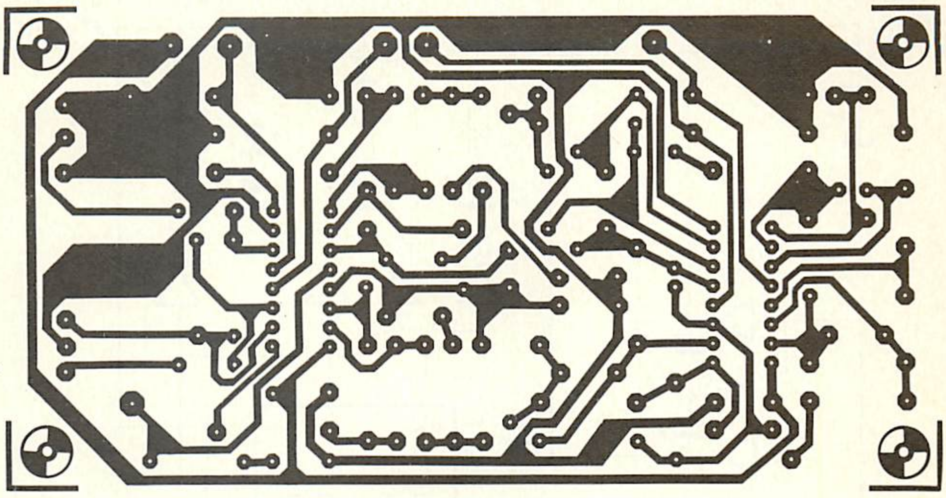
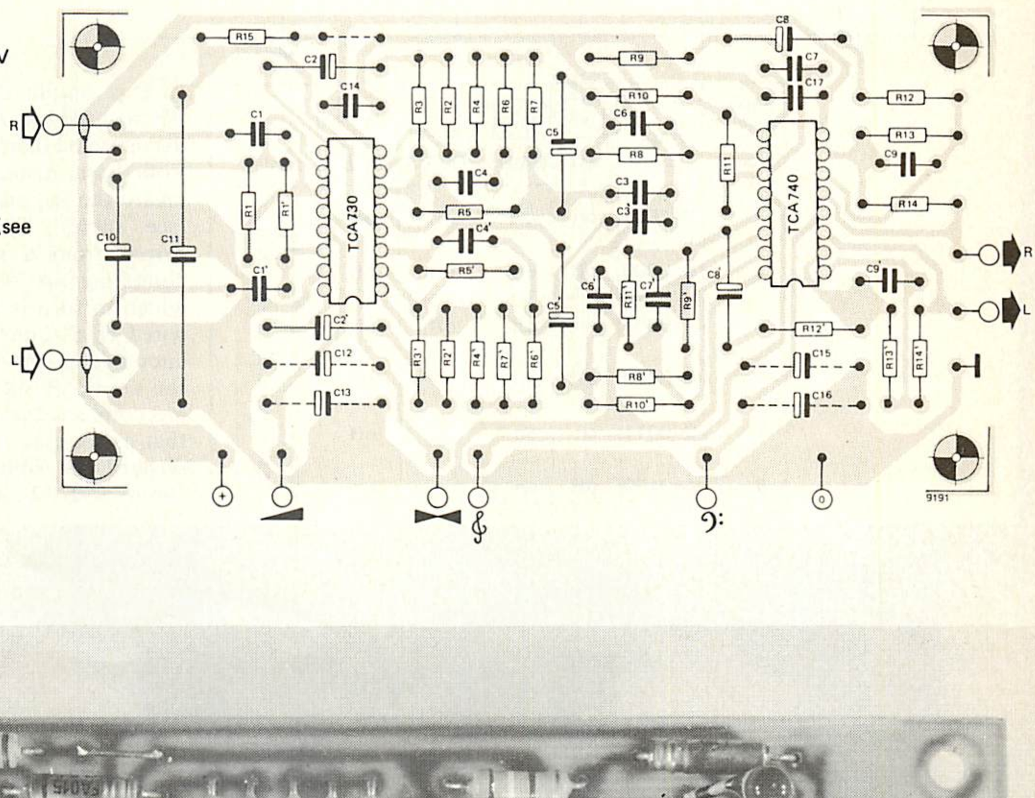


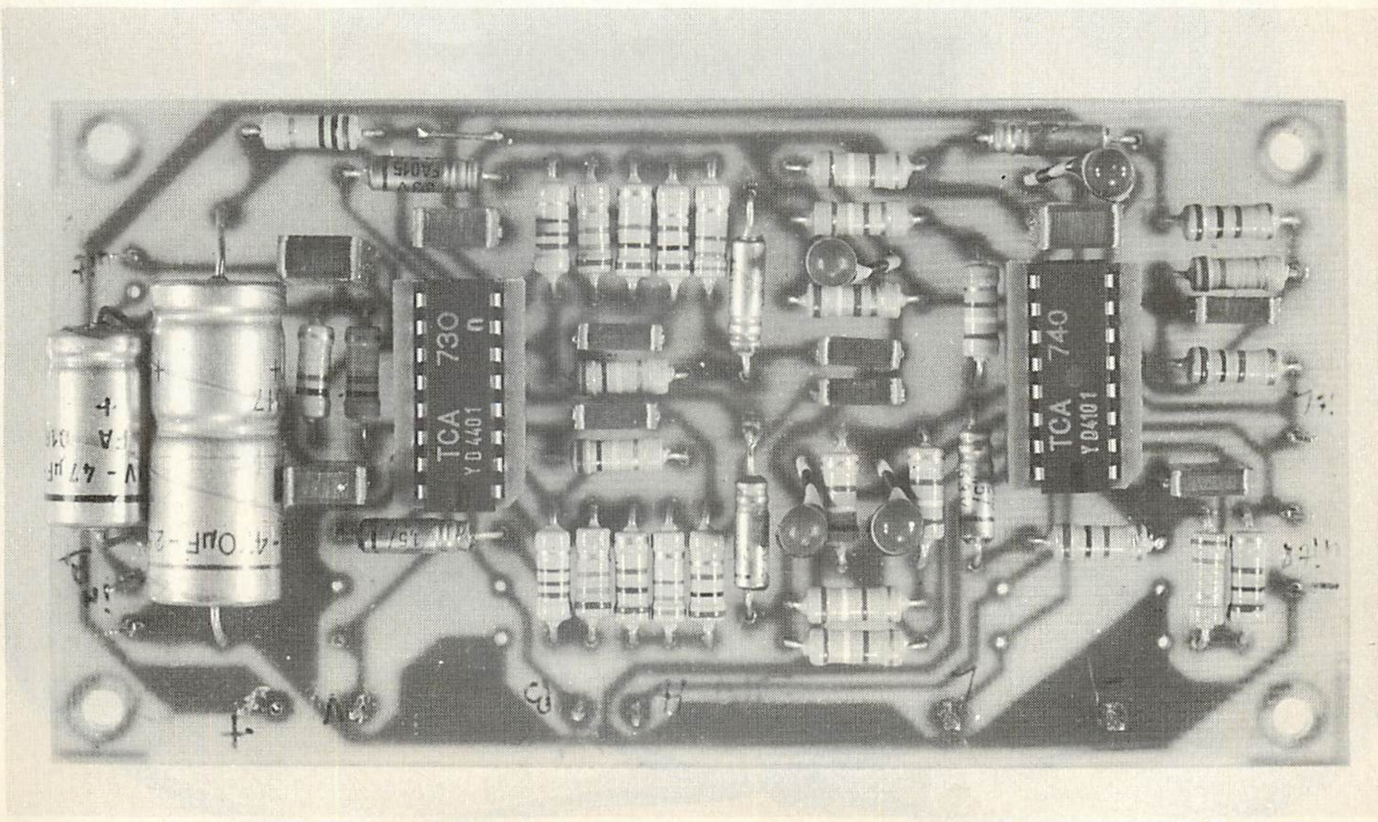
Parts list

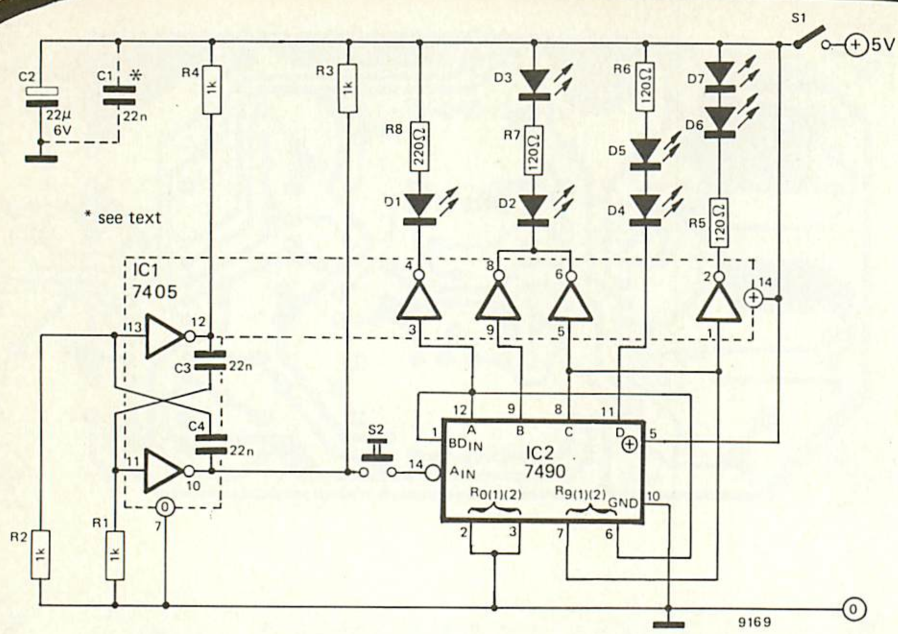
Resistors:
R1,R1' = 270 k
R2,R2' = 18 k
R3,R3' = 33 k
R4,R4',R12,R12',R14,R14' = 12 k
R5,R5' = 120 k
R6,R6' = 10 k
R7,R7' = 560 Ω
R8,R8',R9,R9',R10,R10',R11,R11' = 39 k
R13,R13' = 180 k
R15 = 1 k
R16 = 330 Ω
R17 = 1k5
P1,P2,P3,P4 = 10 k, lin

Capacitors:
C1,C1',C14,C17 = 100 n
C2,C2',C5,C5',C8,C8' = 1 μ/16 V
C3,C3' = 15 n
C4,C4' = 8n2
C6,C6',C7,C7' = 1n8
C9,C9' = 33 n
C10 = 47 μ/16 V
C11 = 470 μ/16 V
C12,C13,C15,C16 = 10 μ/16 V (see text)

Semiconductors:
IC1 = TCA730
IC2 = TCA740







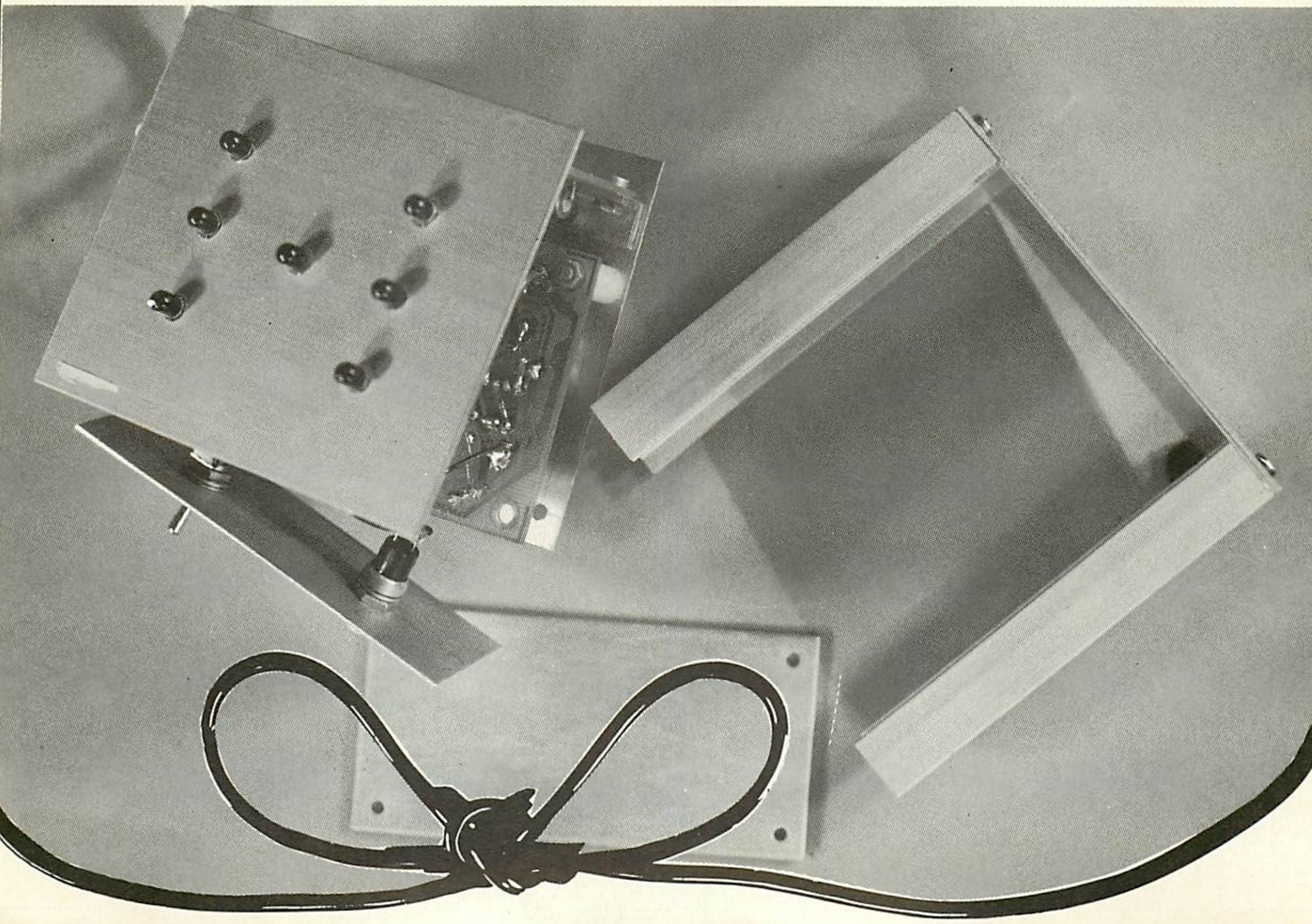
M.G. Fishel

die

Table. throw	7490 count	D1	D4,D5	D2,D3	D6,D7	display
1	9=1001	on	off	off	off	
2	0=0000	off	on	off	off	
3	1=0001	on	on	off	off	
4	2=0010	off	on	on	off	
5	3=0011	on	on	on	off	
6	4=0100	off	on	on	on	

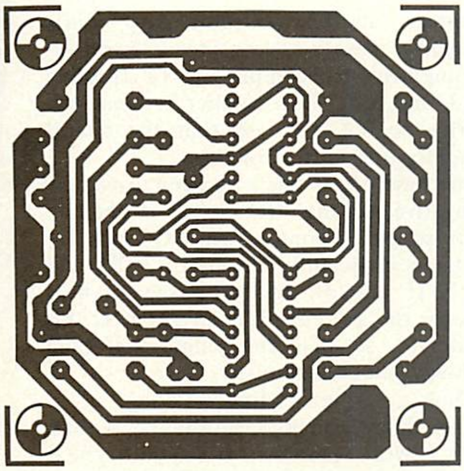
In this simple electronic die only two ICs are used for the oscillator, 6-counter, decoder and display-drivers.

Four basic display patterns are used to create the six displays required for a die (see table). The LEDs D1 - D7 are driven from a simple decoder circuit consisting of 4 inverters (2/3 IC1), which in turn is driven by a 7490 (IC2) wired as 6-counter. A slightly different circuit from the usual is used to achieve the count of six: the A and C outputs are connected to the reset-9 inputs, so that as soon as a count of five (0101) is reached the 7490 is reset to 9. It now counts 9-0-1-2-3-4-9-0-..., a total of six



counts per cycle.
The 7405 contains 6 inverters, of which only four are used for the decoding circuit. The remaining two can therefore be used to construct a simple multivibrator for driving the counter. The multivibrator is free-running; it can be connected to the counter via push-button S2 for each throw of the die.
The LEDs (D1 - D7) are arranged on the printed circuit board in the correct pattern. They can be mounted either on the component side or on the copper side; this second alternative will probably prove the most practical when mounting the die in a small box.

Capacitor C1 (dotted in the circuit) is not mounted on the p.c.b., because it did not prove essential in practice. However, a good power supply (preferably stabilized) is advisable. If batteries are used C1 should be mounted on the board in place of C2, the leads from the battery must be short, and a larger electrolytic (220 μ - 470 μ) must be mounted across the supply connections to the board.



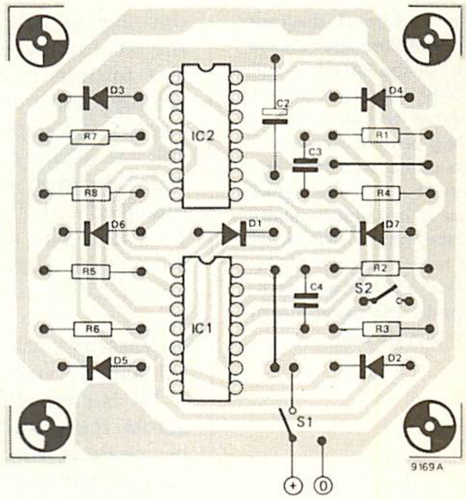
Parts list:

Resistors:
R1 - R4 = 1 k
R5 - R7 = 120 Ω
R8 = 220 Ω

Capacitors:
C1*,C3,C4 = 22 n
C2* = 22 μ/6 V

Semiconductors:
IC1 = 7405
IC2 = 7490
D1 - D7 = LED

* = see text



T. Meyrick

door-chime driver

The bell-wiring-system in many blocks of flats consists of a set of pushes in the communal entrance hallway, a centrally-located (and inaccessible) transformer and a cheap-and-nasty trembler bell in each flat. One's own front door is then usually fitted with a kind of king-size bicycle-bell that requires considerable force to be applied to the push. Since the whole set-up is a minimum-price job, the available current is invariably too low to operate a full-length door-chime, particularly when the flat concerned is located on a higher floor. It is also not normally possible to connect a bell-push on the flat-door into the system. The circuit described here is the result of one engineer's taking up the gauntlet . . .

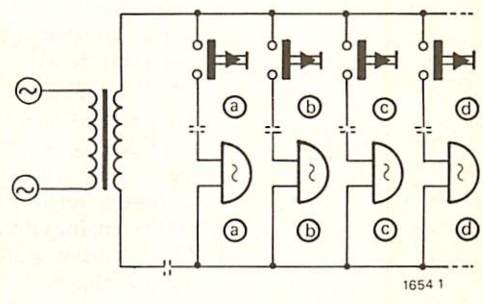


Figure 1, The original situation. The transformer and the bell-pushes (a, b, c, d . . .) are installed in the communal entrance hall.

The existing bell-system is typically wired as in figure 1. The transformer and the bell-pushes are installed in the main hall (or at the street-door), with only the ringing-lines and the common return being brought upstairs. In particular the 'hot side' of the transformer secondary is therefore inaccessible, except at the actual pushes. The solution is obvious: shunt a rectifier diode across the bell-push contacts, so that

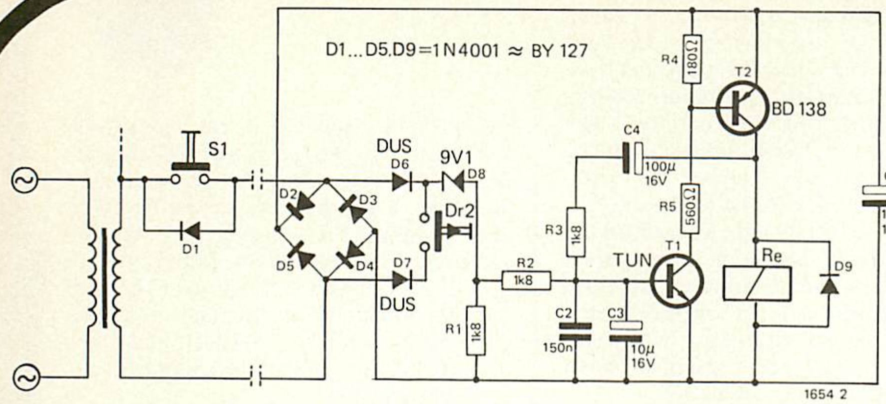


Figure 2. Circuit diagram of the complete door-chime driver. In the entrance-hall one only needs to mount D1 across the contacts of the bell-push corresponding to one's own flat; the remainder of the electronics is installed upstairs near the chime. S2 is an extra push that can be installed at the flat entrance, to replace the usual mechanical 'bicycle bell'.

one always has at least half-periods of the AC to play with upstairs. (Figure 2). The upstairs installation starts out with a bridge rectifier (D2 ... D5) and a large electrolytic capacitor (C1). This reservoir is charged, under standby conditions, almost to the peak value of the unloaded AC – typically to about 12 volts. The actual driver circuit is a monostable trigger that responds to the arrival of positive half-periods. These come in either through D6, when the downstairs push shorts D1, or through D7 and S2 (installed at the flat door). If D1 is connected in the opposite sense across the push S1 (it may not always be obvious which wire is which), the positive half-waves will come in continuously through D6. This is no cause for alarm (or for another trip downstairs) - one simply interchanges the incoming wires, so that D6 is connected to the common return and D7 to the ringing-line from S1.

The zenerdiode provides a high threshold at the input, so that interference pulses or the voltage drop in the common return (when someone elses bell is ringing) do not give a false signal.

The positive wave peaks pass through R2 to charge C2 and C3. When T1 is driven into conduction it will also turn on T2. Positive feedback through C4 and R3 will now turn T1 on further, so that the circuit quickly saturates. This applies power to the chime solenoid . . . 'Ding'.

C4 will now charge up through R3, providing a base current for T1 that will keep the circuit temporarily in saturation. The current through R2 on its own is not sufficient to do this, even when the push is held down. As C4 builds up a steadily higher voltage, the current through R3 will drop, until the point is reached at which T1 and T2 start to come out of saturation. The voltage at T2 collector now shifts slightly negative, causing a negative-going drive to be applied to T1 through R3 and C4. This further reduces the drive to T2 . . . so that the circuit rapidly turns off. 'Dong'.

The base of T1 has now been driven far negative, so that the circuit is blocked for several seconds - until C4 can discharge sufficiently through R3, R2 and R1. If one of the bell-pushes is held down the switch will re-trigger after this interval, so that the chime will play slowly but continuously:

'Ding . . . dong . . . ding . . . dong'.

The chime solenoid should be wound for 12-volt operation. If a 6-volt type is used the current surge will cause a far too violent 'ding' (the reservoir voltage being a given condition) - and T2 may be destroyed. The prototype circuit actually did use a 6-volt chime (Friedland) which happened to be on hand - but it was rewound for 12-volt operation. Inspection showed that the solenoid was fully wound with 0.3 mm diameter enamelled-copper wire (SWG 32) to a total resistance of 6 Ω. This winding was stripped and replaced by a full winding of wire-diameter 0.22 mm (SWG 36). The new solenoid had 30 Ω resistance and about the right number of 'ampere-turns'. A second choice solution would be to use a 6 Ω wirewound resistor (about 5 W) in series with the original solenoid - but this would call for a 25000 µF reservoir capacitor!

Note that D9, across the solenoid winding, prevents the rise of a back-voltage at turn-off which could (would) destroy T2. There is, incidentally, no reason why scrap-box 'germanium' transistors (such as AC 127/AC 128) should not be used - the circuit is fairly uncritical.

santatronics

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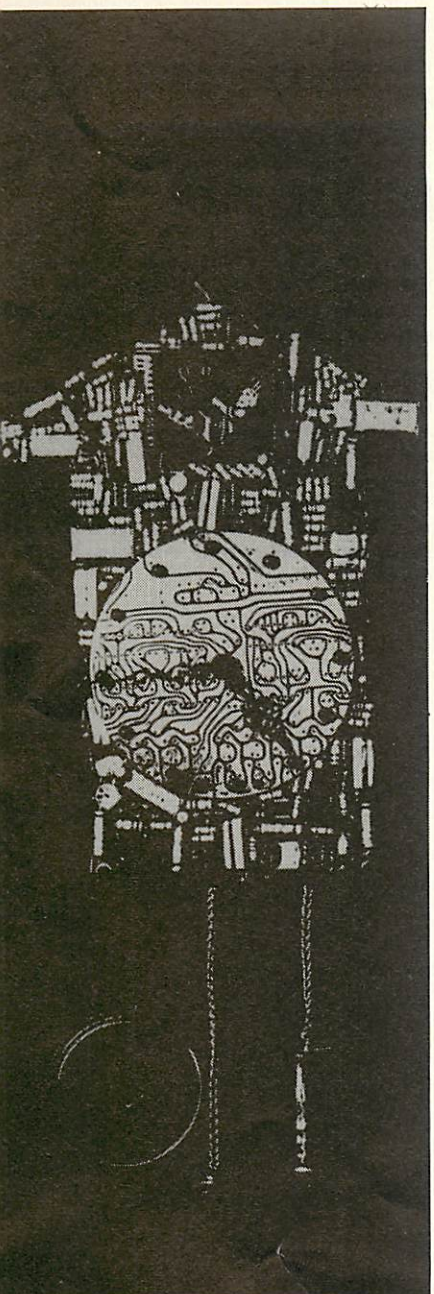


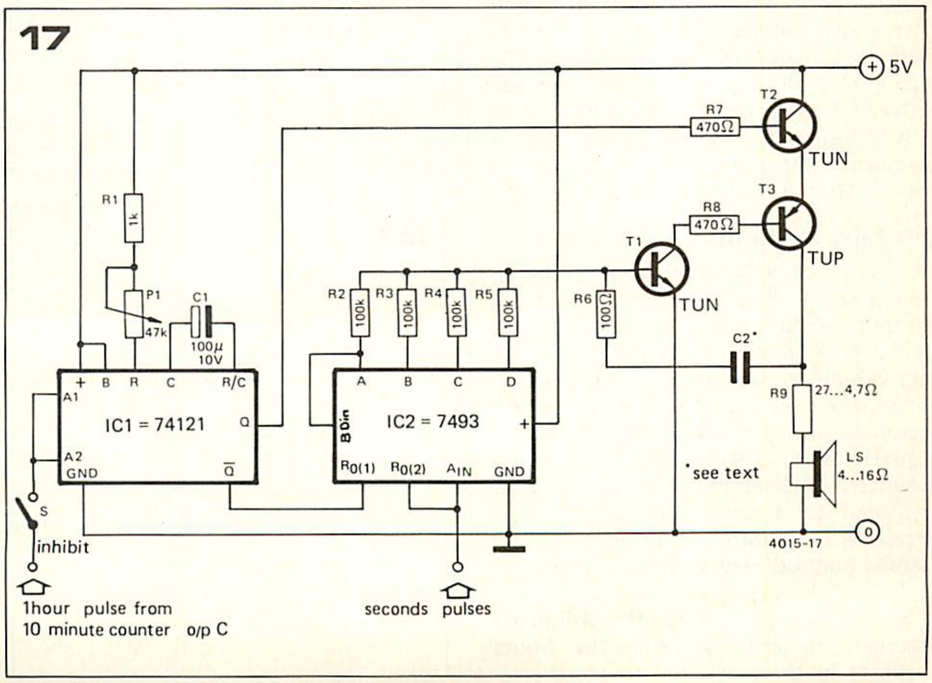
[2] clamant clock

In the last issue of Elektor various sound effects which could be added to electronic digital clocks were described, including a 'tick', alarm systems and a time signal simulator. In the second part of the article various chiming and striking systems are discussed.

In a conventional chiming clock there are two systems. A chime, which plays a tune just before the hour, and a striking system, which sounds a bell a number of times equal to the number of hours. In more sophisticated clocks the chime may also play a portion of its tune at the quarter-, half- and three-quarter-hour marks. In simpler clocks the chime may be absent altogether. It is difficult to convincingly imitate bells and chimes electronically, so in this article two types of system are described, a fully electronic system driving a loudspeaker, and a hybrid electromechanical system suitable for driving a normal electric door chime.
The circuit of a simple electronic chime is given in figure 17.
It operates as follows:

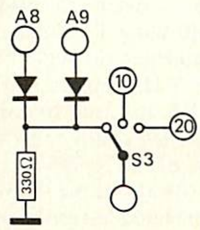
every hour the tens of minutes counter in the clock produces a negative-going pulse that changes the state of the hours counter, and hence the hour display. In the circuit of figure 17 this is used to trigger a monostable with a period of about 4 seconds. The $\overline{Q}$ output of this monostable is connected to one of the reset inputs of a 7493 divide-by-16 counter, so that when the $\overline{Q}$ output of the monostable goes low the counter is enabled and counts pulses from the clock seconds counter, which are fed into the A input. T1 and T3 form a voltage-controlled oscillator, and as the output states of the 7493 change so does the voltage applied to the base of T1, thus altering the frequency of the oscillator.
The oscillator will thus produce a sequence of notes until the monostable resets, and when the seconds pulse input (which is also connected to the other reset input of the 7493) goes high then the counter will reset. T2, which is driven by the Q outputs of the monostable, switches the power supply to the

Figure 17. Circuit of a simple electronic chime.



Missing link Clamant clock part 1

There is an error in the circuit shown in figure 12 (p. 1139). The '0' position of S3 should not go to supply common. Instead, it is connected through a 330 Ω resistor to supply common and through two diodes to the A8 and A9 outputs of the 7473.
The anodes of the diodes are connected to A8 and A9 and the cathodes of both are connected to the switch contact.



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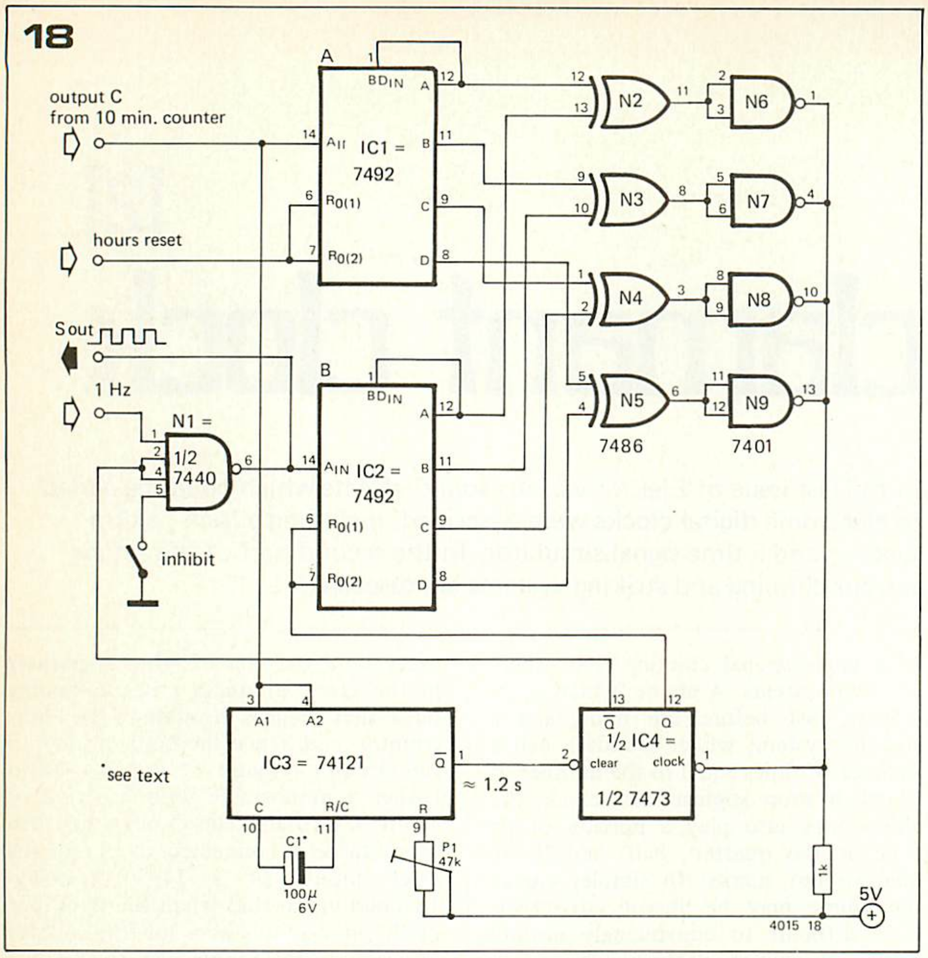

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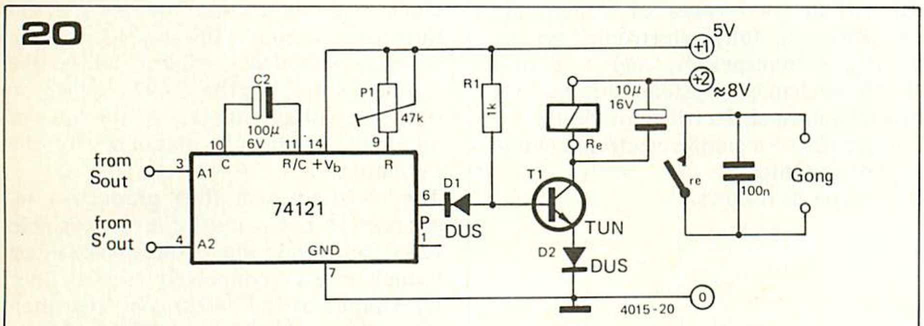


Figure 18. A striking system suitable for driving an electric bell or chime. P1 must be adjusted to give a monostable period time greater than 1 second but less then 2 seconds.

Figure 19. By gating the 3 output of the ten-minute counter and using it to drive the chime the clock will strike on the half-hours as well as the hours.

Figure 20. A suitable drive circuit to switch the chime. There are two inputs, one from the striking circuit and one from the half hour gating of figure 19.

Figure 21. If the drive circuit is used with a D.C. bell then the relay may be omitted and an additional transistor connected as shown will switch the bell.

Figure 22. Circuit of a complete striking system. P1 must be adjusted to give a monostable period time greater than 2 but less than 4 seconds.

VCO, thus disabling it when the chime has finished. P1 can be used to vary the length of the monostable pulse and hence the number of notes in the chime sequence. Altering C2 will change the frequency range of the VCO – the larger C2 the lower the frequency. As a final point, if a faster chime rate is required then the 7493 may be driven by 10 Hz pulses instead of 1 Hz pulses.

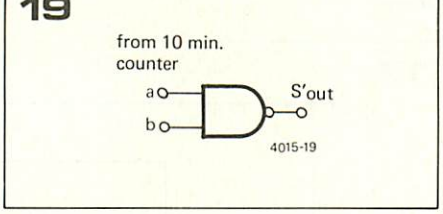
Striking the hours

A circuit for striking the hours is shown in figure 18. The basic idea is that the output of the hours counter is compared with the output of a second counter which is driven by 1 Hz pulses. Every hour on the hour 1 Hz pulses are gated into this counter until its count equals the output count of the hours counter. The number of 1 Hz pulses required to achieve this state is thus equal to the number of hours and these pulses may be used to drive a chime or bell.

The circuit operates in the following manner: instead of using the hours counter in the clock to provide the required information an auxiliary divide-by-12 counter (IC1) is used. This has the advantage that (coded) outputs from 0 - 11 are available directly from a single counter, whereas deriving these outputs from the hour and ten-hour counters in the clock would require additional gating. It should be noted that, whereas the clock counts hours 1-12 the counter counts 0-11. This is no disadvantage as there are still 12 output states for the striking system.

Every hour on the hour monostable IC3 is triggered by the output of the ten-minute counter. The $\overline{Q}$ output of this monostable is used to clear flip-flop IC4, thus allowing 1 Hz pulses from the 10-second counter through N1. IC2 now counts the 1 Hz pulses. Exclusive-OR gates N2 - N5 are used to compare each bit of the hours count with each bit of the output of IC2. When each bit is equal the outputs of N2 - N5 are all low so the commoned outputs of N6 - N9 go high. On the next pulse to IC2 the outputs of the two counters become different and the commoned outputs of N6 - N9 go low again, thus clocking IC4.

19



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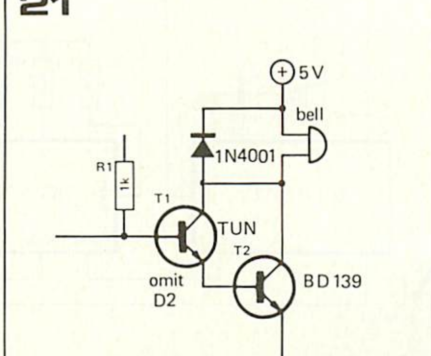

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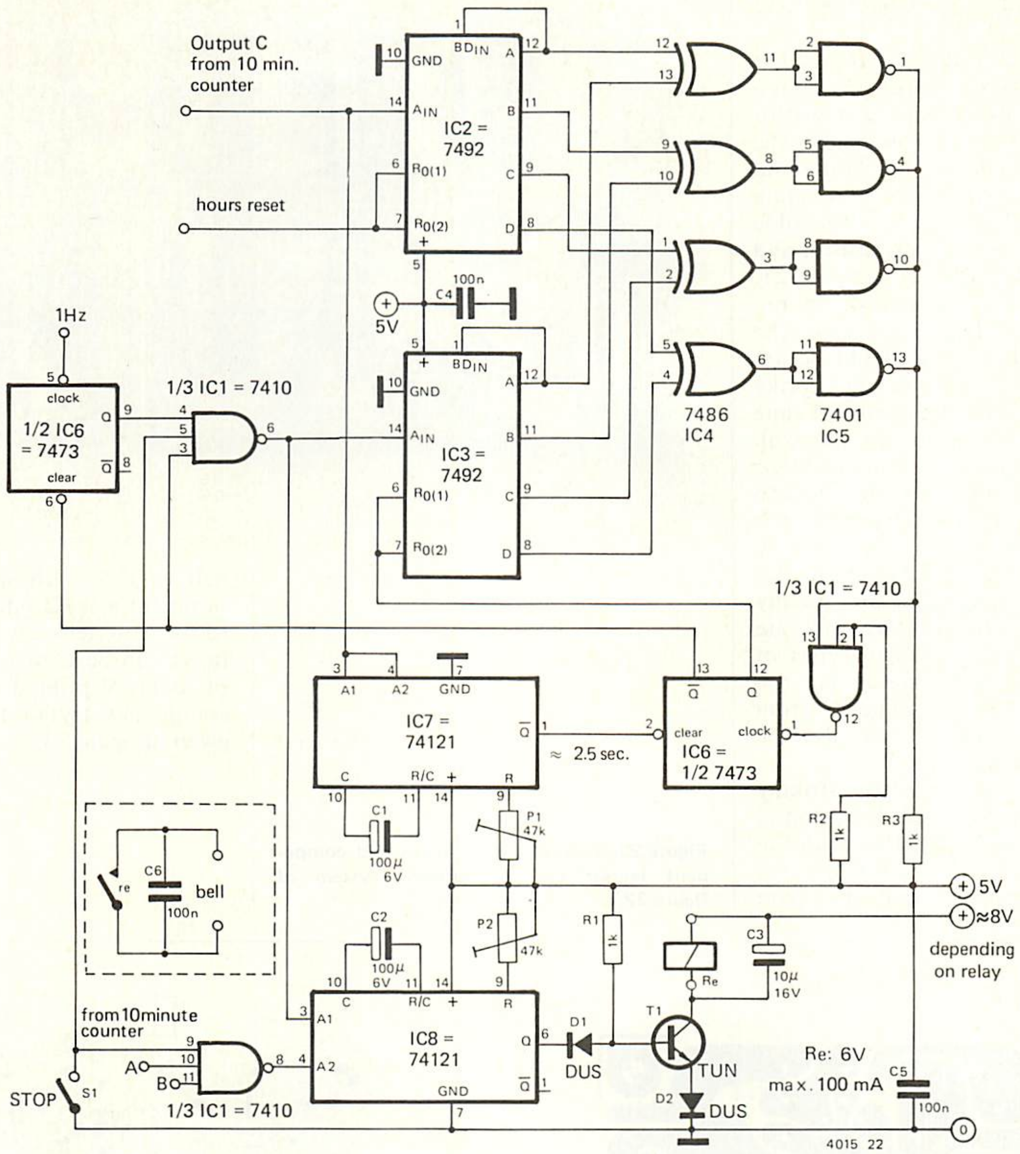
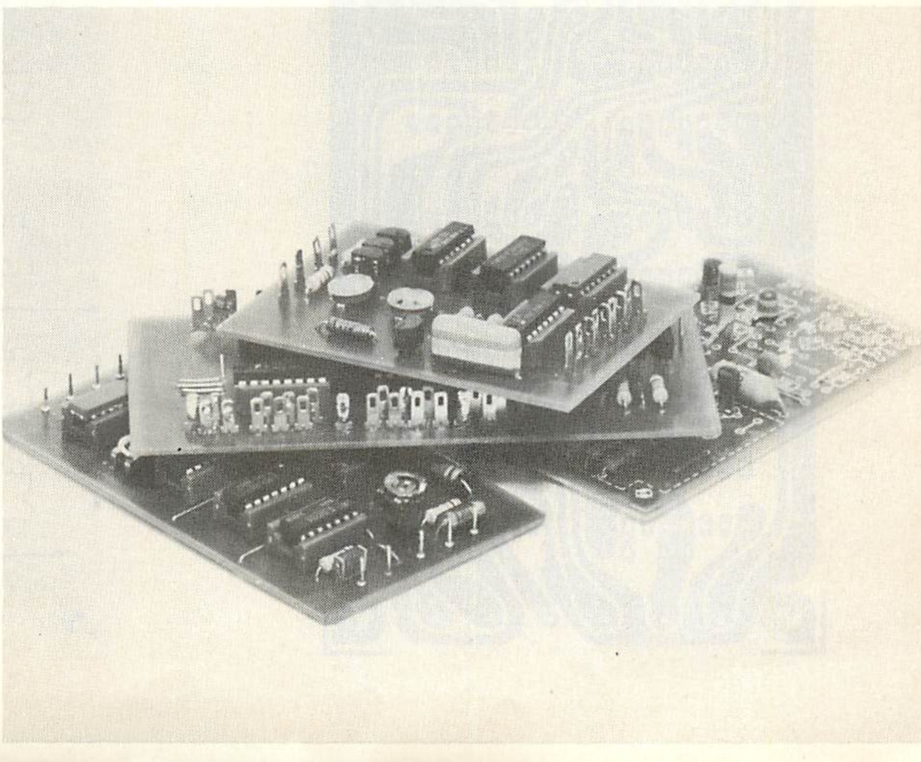


The Q output of IC4 goes high, resetting IC2, while the $\overline{Q}$ output goes low, blocking N1 so that no more 1 Hz pulses can be counted. The number of pulses allowed through N1 is thus equal to the count of IC1 plus 1, which is of course the number of hours since IC1 is always one digit behind the counters in the clock. The pulses can therefore be taken from the output of N1 and be used to drive the chime or bell.

To ensure that counter IC1 is in synchronism with the clock hours counters, and thus prevent the wrong hour from being struck, it is necessary to reset IC1 to zero at the change from 12 to 1 o' clock in a 12 hour system, or at the transition from 12 to 13 hours or 00 to 01 hours when used with a 24-hour clock.

Striking the half-hour

As a small refinement it is possible to make the clock strike once on the half-hour. As the half-hour corresponds to an output of 3 or binary 0011 on the tens of minutes counter this can easily be derived by NANDing together the A



and B outputs of the ten-minute counter in the clock, as in figure 19. The output of this NAND-gate can then be used to trigger the bell, which will then strike every half-hour.

A suitable drive circuit for the bell is given in figure 20. It consists of a monostable multivibrator driving a transistor which switches a relay. This enables the circuit to be wired into the household A.C. doorbell circuit. If a separate (D.C.) bell or chime is used it is possible to drive it directly with a transistor and dispense with the relay, as in figure 21. P1 adjusts the pulse length of the monostable and hence the time for which the bell coil is energised. It should be adjusted so that the bell will just strike reliably, to minimise the energised time and hence the dissipation in the coil. If a normal ding-dong type of door chime is used it may be a good idea to remove one of the tubular or bar resonators so that the chime produces only a single stroke. In the larger tubular type of chime the tubes are usually suspended on cord or wire and are easily removed. The smaller types of chime usually employ metal bar resonators which are suspended from rubber mounts. These can also be removed quite easily.

The circuit of a complete striking system is given in figure 22. It embodies the ideas of figure 18 together with the half-hour striking circuit of figure 19. The only difference is that the spare half of IC6 is utilised and the strikin occurs at a ½ Hz rate. If this is though to be too leisurely then the second input can be connected direct to pin 4 of IC1. A printed circuit board an component layout for this circuit ar given in figure 23. K

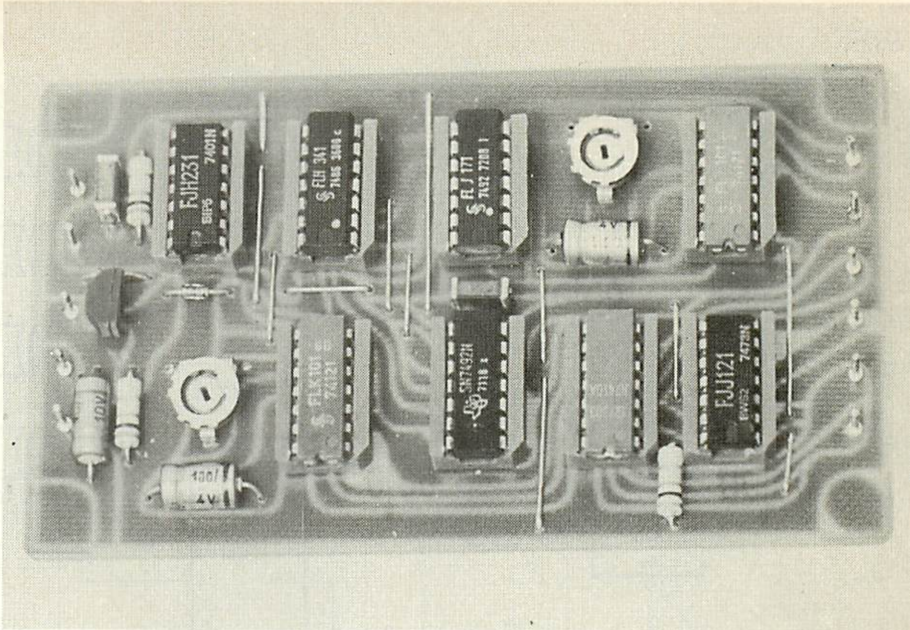


Figure 23. Printed circuit board and component layout for the striking system of figure 22.

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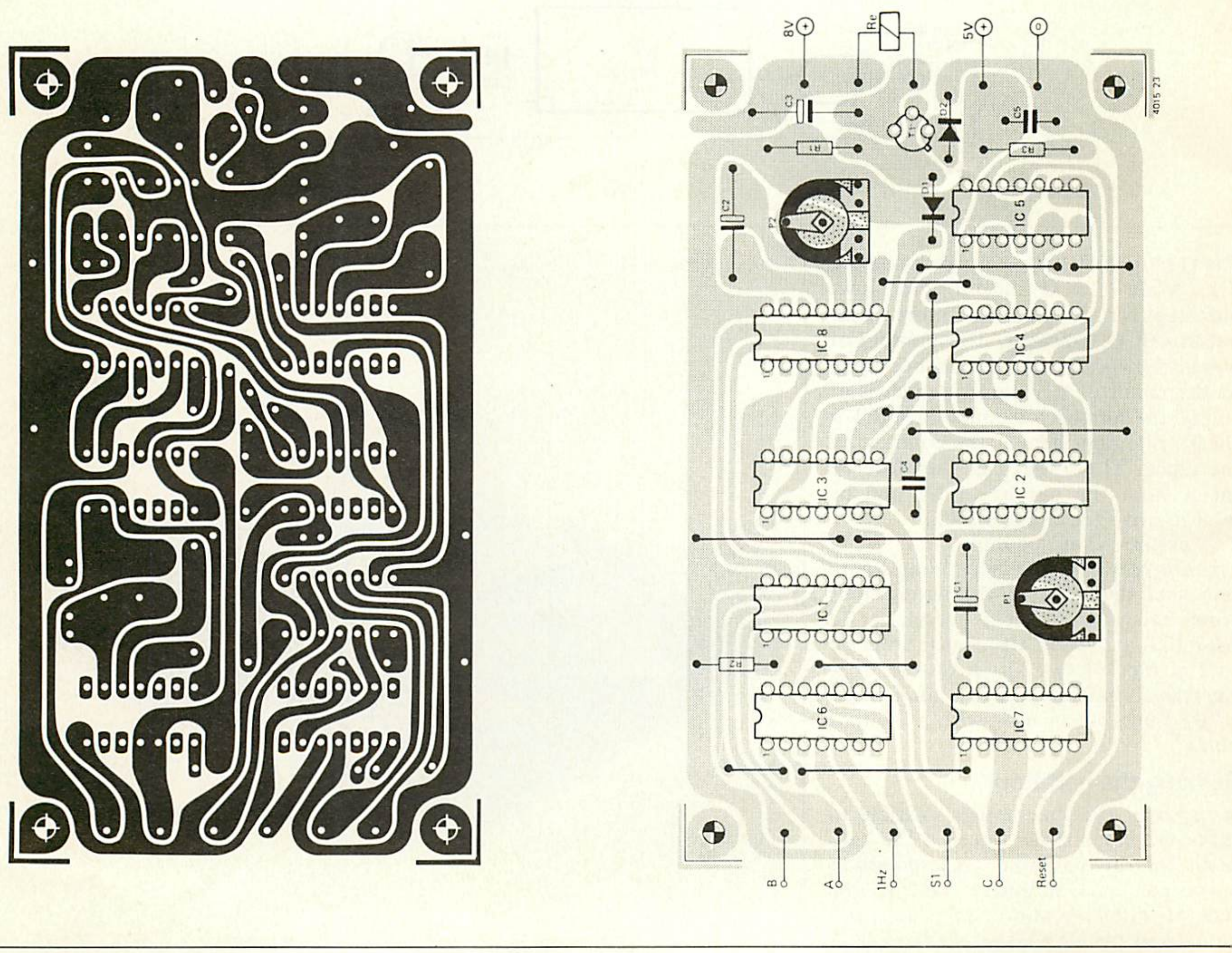
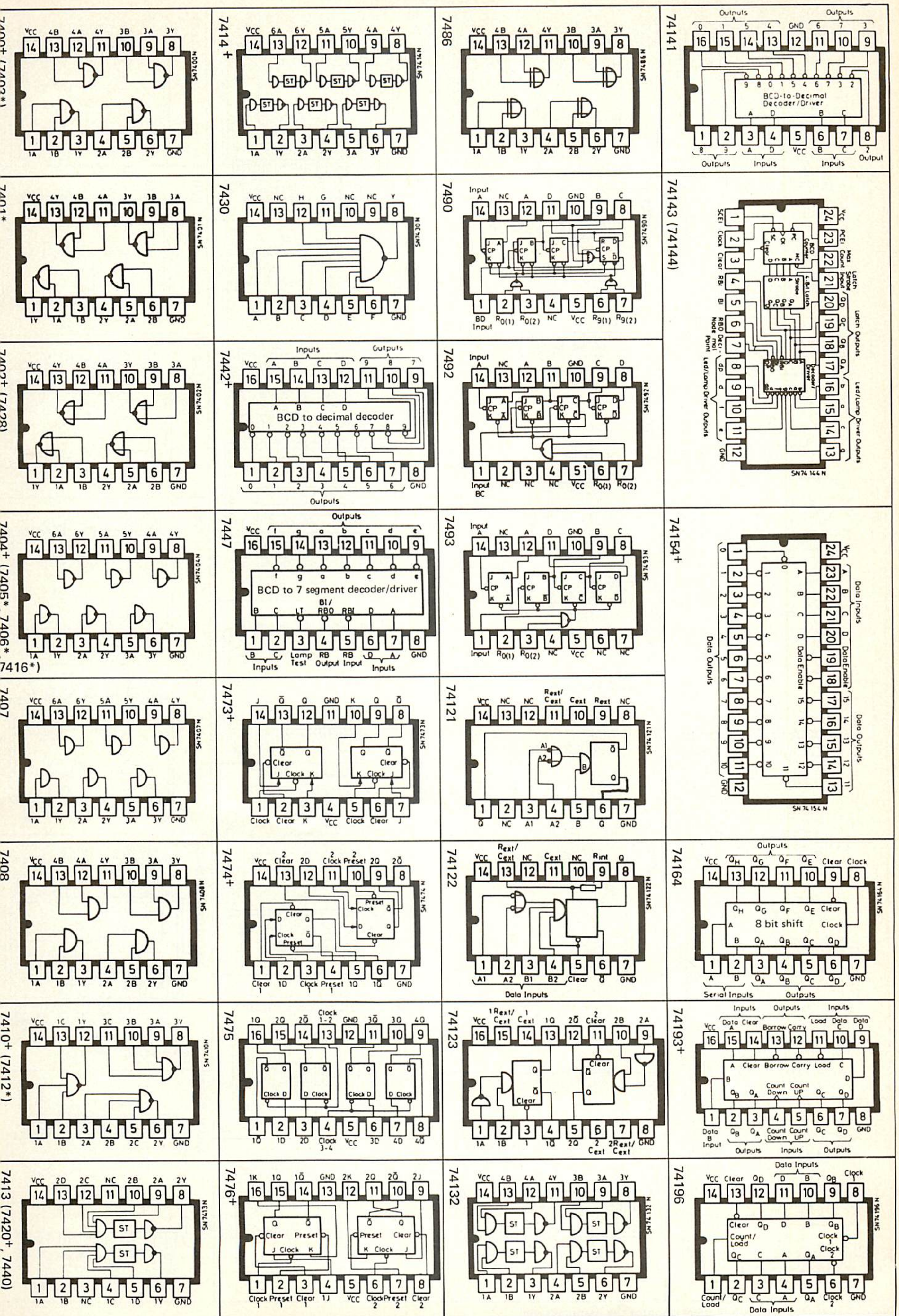
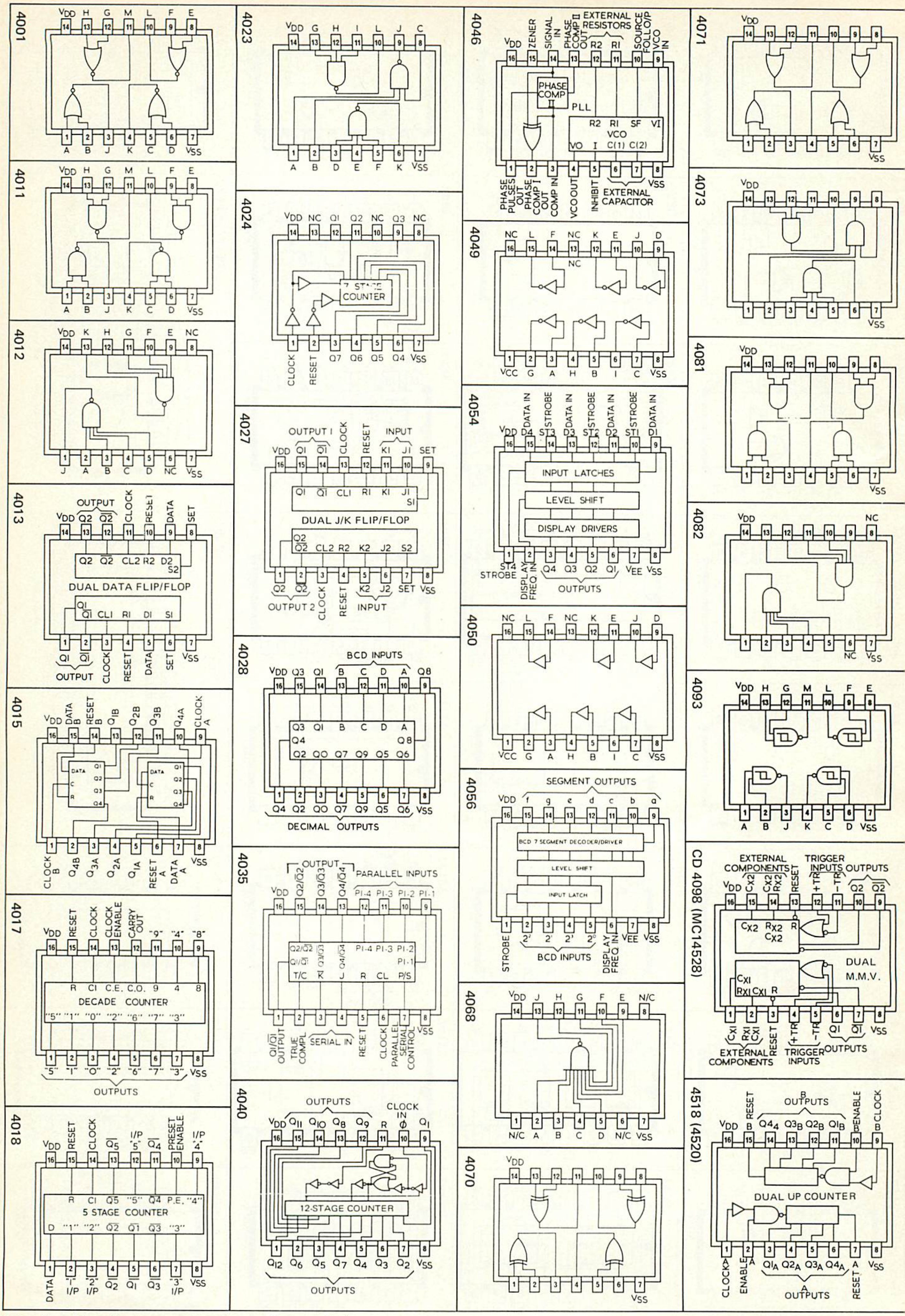




* open collector

+ Pin-compatible CMOS equivalents available from Teledyne Semiconductor and National Semiconductor



Note: A prefix to the type number denotes the manufacturer,
e.g. **CD** 4001 (RCA), **MC** 14001 (Motorola), **N** 4001 (Signetics), **SCL** 4001 (Solid State Scientific), **SIL** 4001 (Siltek).

TUP TUN DUG DUS

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP' (Transistor, Universal PNP), 'TUN' (Transistor, Universal NPN), 'DUG' (Diode, Universal Germanium) or 'DUS' (Diode, Universal Silicon). This indicates that a large group of similar devices can be used, provided they meet the minimum specifications listed above.

For further information, see the article 'TUP-TUN-DUG-DUS' in Elektor 1, p. 9.

	type	U_{ceo} max	I_c max	h_{fe} min.	P_{tot} max	f_T min.
TUN	NPN	20 V	100 mA	100	100 mW	100 MHz
TUP	PNP	20 V	100 mA	100	100 mW	100 MHz

Table 1a. Minimum specifications for TUP and TUN.

Table 1b. Minimum specifications for DUS and DUG.

	type	U_R max	I_F max	I_R max	P_{tot} max	C_D max
DUS	Si	25 V	100 mA	1 μA	250 mW	5 pF
DUG	Ge	20 V	35 mA	100 μA	250 mW	10 pF

Table 2. Various transistor types that meet the TUN specifications.

TUN		
BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP		
BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG
BA 127	BA 318	OA 85
BA 217	BAX13	OA 91
BA 218	BAY61	OA 95
BA 221	1N914	AA 116
BA 222	1N4148	
BA 317		

Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification ($I_{c,max}$ = 50 mA).

	NPN	PNP
	BC 107 BC 108 BC 109	BC 177 BC 178 BC 179
V_{ce_0} max	45 V 20 V 20 V	45 V 25 V 20 V
V_{eb_0} max	6 V 5 V 5 V	5 V 5 V 5 V
I_c max	100 mA 100 mA 100 mA	100 mA 100 mA 50 mA
$P_{tot.}$ max	300 mW 300 mW 300 mW	300 mW 300 mW 300 mW
f_T min.	150 MHz 150 MHz 150 MHz	130 MHz 130 MHz 130 MHz
F max	10 dB 10 dB 4 dB	10 dB 10 dB 4 dB

The letters after the type number denote the current gain:

A: α' (β, h_{fe}) = 125-260
B: α' = 240-500
C: α' = 450-900.

Table 6. Various equivalents for the BC107, -108, . . . families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107 BC 108 BC 109	BC 177 BC 178 BC 179	C B E	
BC 147 BC 148 BC 149	BC 157 BC 158 BC 159	C B E	P_{max} = 250 mW
BC 207 BC 208 BC 209	BC 204 BC 205 BC 206	C B E	
BC 237 BC 238 BC 239	BC 307 BC 308 BC 309	C B E	
BC 317 BC 318 BC 319	BC 320 BC 321 BC 322	C B E	I_{cmax} = 150 mA
BC 347 BC 348 BC 349	BC 350 BC 351 BC 352	C B E	
BC 407 BC 408 BC 409	BC 417 BC 418 BC 419	C B E index	P_{max} = 250 mW
BC 547 BC 548 BC 549	BC 557 BC 558 BC 559	C B E	P_{max} = 500 mW
BC 167 BC 168 BC 169	BC 257 BC 258 BC 259	E C B !	169/259 I_{cmax} = 50 mA
BC 171 BC 172 BC 173	BC 251 BC 252 BC 253	B C E	251 . . . 253 low noise
BC 182 BC 183 BC 184	BC 212 BC 213 BC 214	B C E	I_{cmax} = 200 mA
BC 582 BC 583 BC 584	BC 512 BC 513 BC 514	B C E	I_{cmax} = 200 mA
BC 414 BC 414 BC 414	BC 416 BC 416 BC 416	B C E	low noise
BC 413 BC 413	BC 415 BC 415	B C E	low noise
BC 382 BC 383 BC 384		B C E	
BC 437 BC 438 BC 439		C B E	P_{max} = 220 mW
BC 467 BC 468 BC 469		B C E !	P_{max} = 220 mW
	BC 261 BC 262 BC 263	C B E	low noise

TUP TUN DUG DUS

MARKET

LM 395, a non-suicidal power transistor

Modern power transistors can usually stand a lot of rough treatment, within the maxima specified for current, power dissipation, safe operating area, voltage, temperature, et al. However, if any of these specified limits is exceeded the transistor in question usually commits suicide - as many designers have discovered ... If this transistor happens to be the series regulator in a stabilised power supply, the total repair bill can easily be an order of magnitude higher than the cost of the transistor itself.

National Semiconductor have recently announced a new power transistor, the LM 395, which will reduce the risk of failure to a minimum. It is actually a complete integrated circuit, consisting of a darlingtontype power transistor and several overload protection circuits; it is mounted in a TO-3 case. Figure 1 shows the functional block diagram, as well as the pinning. It should be noted that the emitter is connected to the case, contrary to normal practice. Block 'A' (figure 1) contains three overload protection circuits: a current limiter, thermal shutdown and safe operating area limiter.

The current limiter is set at 2 A - this keeps the current sufficiently low to avoid melting of the aluminium connections inside the case. If the power dissipation is excessive or the cooling is inadequate, or both, the thermal shutdown becomes operative. It turns off the transistor when the chip temperature reaches 170 °C. Finally, the 'safe area' protection progressively limits the current as the collector-emitter voltage rises, thereby eliminating the possibility of second breakdown.

The only specifications that are not safeguarded by the internal circuitry are the polarity and the maximum value of the collector-emitter voltage (36 V).

The 'power transistor' itself actually consists of three transistors (figure 1): a PNP input transistor T1, and a power-Darlington configuration T2/T3. The current gain of this combination is approximately 10^6, which means that 3 μA base current will drive the LM 395 into saturation. Put another way: one CMOS gate is capable of driving 100 LM 395s in parallel . . .

The base capacitance is so low that even at high frequencies the transistor can be driven from a high impedance source. It is also sufficiently fast to make this a plausible requirement: the switching time is about 500 ns (36 V supply, 25 Ω load).

The various specifications are summarised in the tables. Figure 2 shows the complete internal circuit diagram of the 'power tran-

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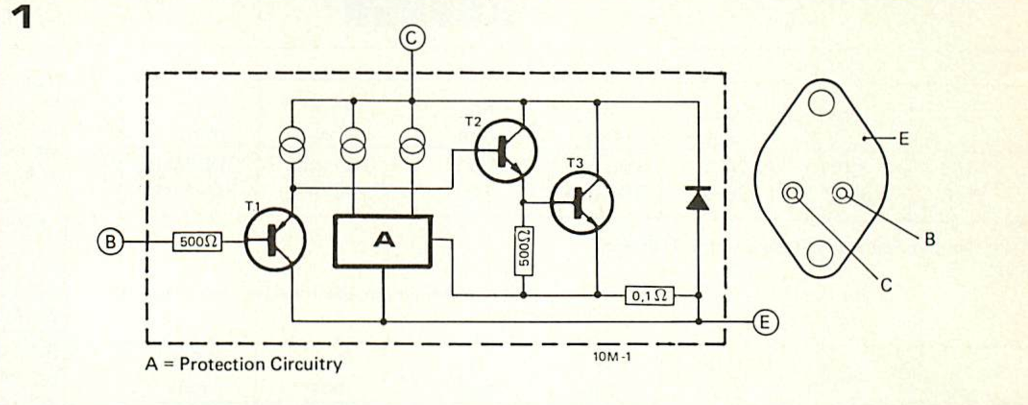

Figure 1. Block diagram and connections of the LM 395. Note that the emitter is connected to the case!

Figure 2. The internal circuitry of the LM 395. Transistors T14, T19 and T20 correspond to T1, T2 and T3 in figure 1.

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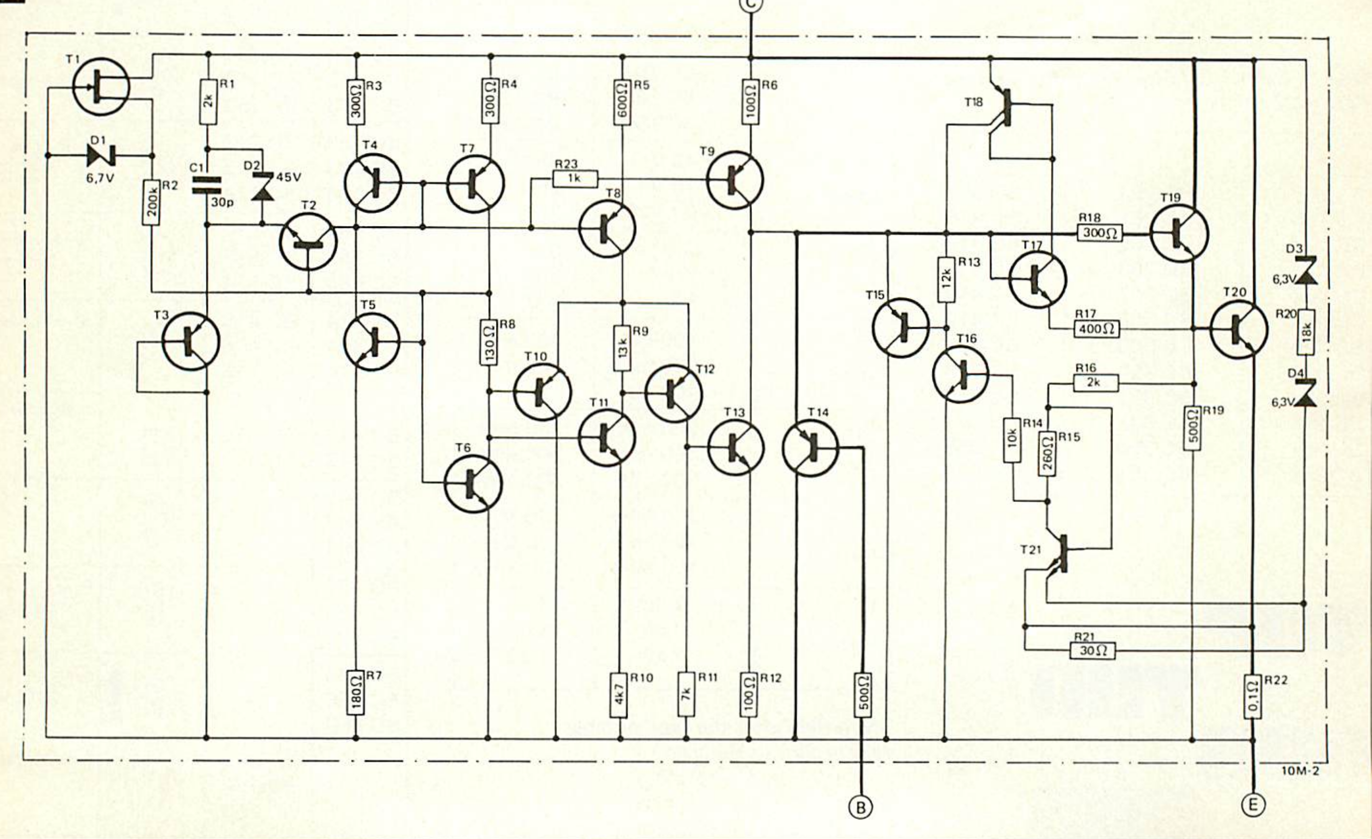

MARKET

sistor'. T14, T19 and T20 in this circuit correspond to T1, T2 and T3 in figure 1.
The 'safe operating area' protection starts to become effective at approximately V_{CE} = 17 V (I_{max} = 1.8 A); at the maximum voltage, V_{CE} = 36 V, the maximum current is limited to 0.8 A.

Applications

National Semiconductor give a whole series of practical applications for their new device, and it isn't difficult to think up several more. However, one or two practical details should be noted at the outset.
As stated previously, the 'transistor' is not voltage-protected: more than 36 V between collector and emitter, or more than −20 V base-emitter, is forbidden - it will lead to sudden death. Furthermore, if the collector and emitter are interchanged (supply voltage of the wrong polarity) the LM 395 will join its less sophisticated brothers of a previous generation in Valhalla.
If the transistor is used as an emitter follower, the high input impedance combined with the high gain can sometimes lead to low level oscillation at high frequencies. A 'stopper' resistor (4k7 - 10 k) in the base lead - soldered onto the base pin itself - is sufficient to cure this. It is a good idea also to use this resistor when the 395 is driven from a low-impedance source: it will limit the base current to a safe value.
One should always bear in mind that the 395 is a 'fast' transistor, which means that (amongst other things) decoupling capacitors in the supply should be high frequency types - e.g. ceramic discs and/or tantalum electrolytics.
Finally, it should be noted that the input transistor (T14 in figure 2) is a PNP type. This means that the base current flows *out* of the base, in the opposite direction to the base current in a 'normal' NPN power transistor. Furthermore, an *increase* in base current leads to a *decrease* in the output current! The combination of these two effects leads to the 'NPN-like' behaviour, AC-wise: a rise in base *voltage* leads to a rise in output *current*. To put it another way: once a DC bias current is set, flowing out of the base, a (smaller) AC current flowing into the base will give rise to a much larger increase in output current - which is 'normal NPN behaviour'. The symbol used in the circuit diagrams shows the PNP input transistor and the NPN output device.

Current limiter

It would not be easy to find a circuit for a current limiter using less components than the one shown in figure 3 . . . Base and collector of the device are linked together, so that it is driven into saturation (the base current is *zero*!). The current through the limiter is kept at or below 2 A by the current protection circuit in the IC. Furthermore, if an overload leads to excessive dissipation the thermal shutdown will protect the device and the load connected to it.
During normal operation, i.e. when the current limiter is not operative so that the transistor is still driven into saturation, the voltage across the device will be approximately 2 V. A further protection of the load can sometimes be effected by mounting the 395 on the same heatsink as the load: the thermal shutdown in the IC will become operative if the heatsink gets too hot.

Table 1.

Maximum ratings:	
Collector-emitter breakdown voltage:	36 V
Collector-base breakdown voltage:	36 V
Base-emitter voltage, positive maximum:	36 V
Base-emitter voltage, negative maximum:	−20 V
Collector current:	limited
Dissipation:	limited

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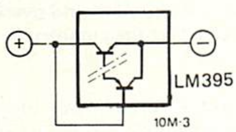

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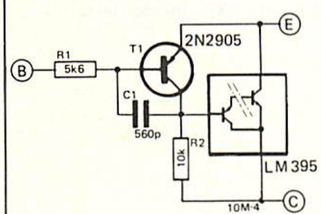

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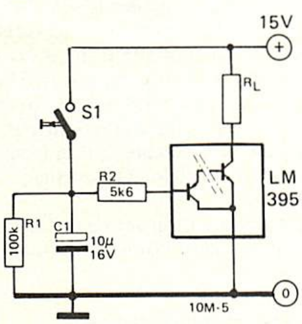

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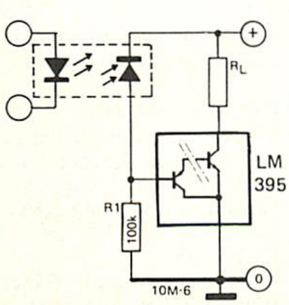

Table 2.

Electrical characteristics:	conditions	min.	typ.	max.	unit
collector-emitter voltage	$I_Q \leqslant I_C \leqslant I_{max}$			36	V
base-emitter breakdown voltage	$0 \leqslant V_{CE} \leqslant V_{CEmax}$	36	60		V
base-emitter voltage	I_C = 1 A, T_a = 25°C		0.9		V
saturation voltage	$I_C \leqslant 1$ A		1.8	2.2	V
saturation current	$V_{CE} \leqslant 15$ V	1.0	2.0		A
base current	$0 \leqslant I_C \leqslant I_{Cmax}$, $0 \leqslant V_{CE} \leqslant V_{CEmax}$		3.0	10.0	µA
quiescent current	V_{BE} = 0, $0 \leqslant V_{CE} \leqslant V_{CEmax}$		2.0	10.0	mA
Switching time	V_{CE} = 36 V, R_L = 36 Ω, T_a = 25°C		500		ns
Thermal resistance, junction to case	TO-3 case		2.3	3.0	°C/W

All specifications are based on a junction temperature of 0°C - 125°C, unless otherwise stated. Without a heatsink the thermal resistance from junction to ambient is 35°C/W.

Figure 3. A current limiter circuit.

Figure 4. A PNP transistor can be simulated in this way, for use in quasi-complementary configurations.

Figure 5. This power timer design uses a minimum number of components.

Figure 6. An opto-coupled and short-circuit proof switch.

Simulated PNP power transistor

By adding one extra transistor (figure 4) it is possible to simulate a PNP transistor, so that the 395 can be used in quasi-complementary circuits.
R1 and C1 limit the base current and suppress any tendency to instability. R2 sets the DC bias for the power device.
Note that the symbols 'B', 'C' and 'E' in the circuit refer to the base, collector and emitter of the simulated PNP transistor - not of the 395 itself.

Power timer

When S1 is closed (figure 5) C1 charges to the supply voltage. The LM 395 is driven into saturation. After S1 is opened, C1 discharges through R1. When the voltage has dropped sufficiently (down to approximately 0.8 V) the 395 turns off quite rapidly and switches off the load R_L.

Opto-coupled switch

As long as the LED in the opto-coupler (figure 6) is dark the 395 remains cut off, so no current flows through R_L. As soon as the LED is driven, the 395 turns on. A LED current of 20 µA is sufficient. The switching time is 500 ns (at 36 V and 1 A).

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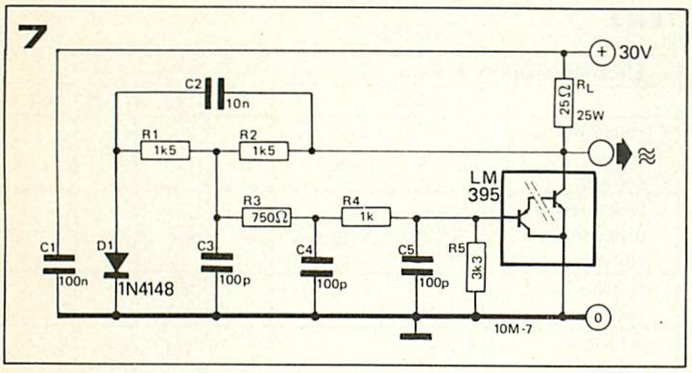

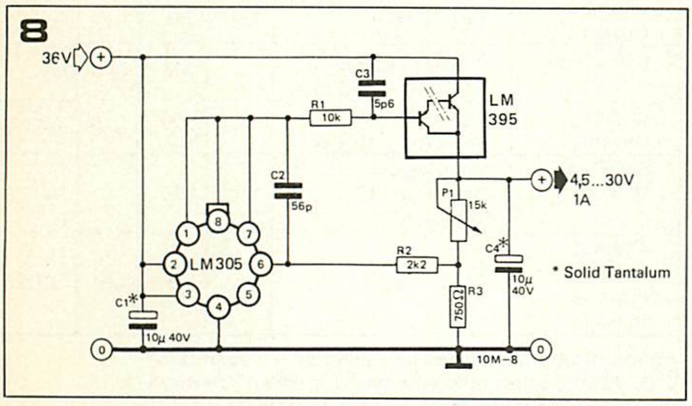

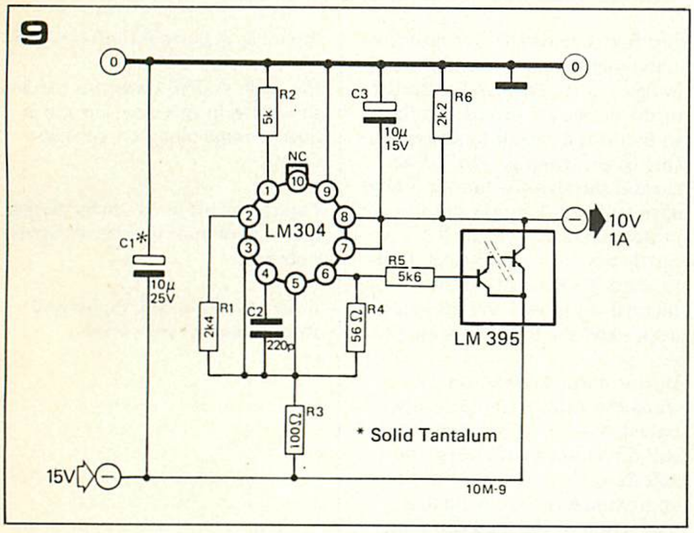

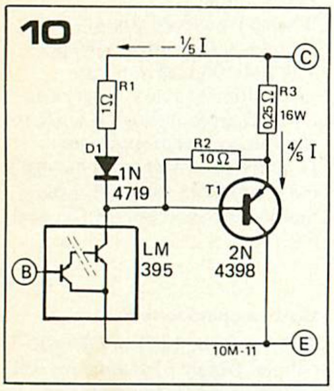

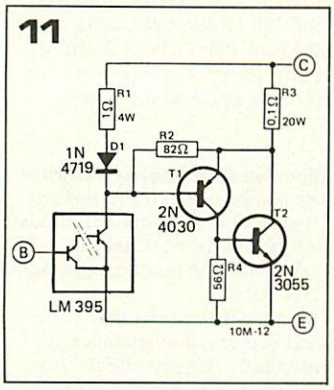

Figure 7. 1 MHz power oscillator. The R and C elements in the ladder network determine the frequency.

Figure 8. A positive supply regulator. The voltage can be set with P1 (between 4.5 and 30 V); the maximum current is 1 A.

Figure 9. A negative supply regulator. R2 sets the output voltage; the value shown gives –10 V.

Figure 10. The output current rating can be increased by adding a PNP power transistor. This circuit has the advantage that both devices are current- and overload-protected by the circuitry in the LM 395.

Figure 11. Another way of increasing the output current (and power) rating is to use an NPN power transistor in a quasi-complementary circuit. This has the additonal advantage that the NPN power device is usually cheaper than its PNP counterpart.

1 MHz power oscillator

The oscillator shown in figure 7 uses an RC ladder network. The gain of the LM 395 is sufficient to compensate for the losses in the network, so no further transistors are required. The capacitors should be high frequency low loss types.

Positive supply stabiliser

Figure 8 shows a stabilised power supply. The output voltage can be set by P1, from 4.5 to 34 V.
The voltage stabiliser IC LM 305 (SN 72305) sets the output voltage and the LM 395 is the short-circuit proof series regulator. The high gain of the 395 makes for an extremely well stabilised output voltage: the voltage change from no load to full load is less than 2 mV.
The voltage drop across the series stabiliser need not be more than 2 V.

Negative supply stabiliser

The stabilised power supply shown in figure 9 is preset for –10 V at 1 A. It is a simple matter to modify the circuit for other output voltages. Resistor R2 determines the output voltage; the rule of thumb is that the voltage is 2 V per kΩ.

Higher output currents

A number of LM 395s can be connected in parallel if higher output currents are required. There is usually no need to modify the driver stage, as each 395 draws less than 3 µA.
If the parallel connected 395s are used in an emitter follower configuration, 5k6 resistors in each base lead are required.

Figures 10 and 11 show two alternative possibilities for increasing the output current capability. The circuit in figure 10 will deliver 5 A, whereas the circuit in figure 11 can go up to 10 A. Both circuits rely on the current and dissipation in the 395 and the external power transistor being in the correct proportion. If this proportion is set correctly, the 395 will limit the output current and the power dissipation of both devices to safe levels.
Generally speaking, the circuit shown in figure 11 is preferred. Although it uses more components, the NPN power transistor is much cheaper than its PNP counterpart in figure 10.
Of couse, the heatsink for the power transistor must be adequate, to ensure that it does not overheat at a total power level which is insufficient to trigger the thermal shutdown in the 395.
If possible, the diode D1 should be thermally coupled to the heat sink for the additional power transistor.

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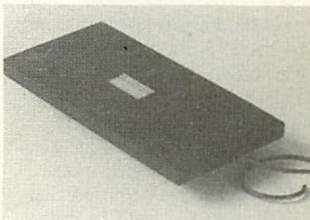
Dynamics enters module amplifier business

Known as a leading manufacturer of Instrumentation Amplifiers for 16 years, Dynamics now offers Instrument, Module 7535 Differential DC Amplifier with the following superior features.



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Price: $ 225,—

Dynamics Electronic Products, Inc., 12117 E. Slauson Avenue, Santa Fe Springs, California 90670.

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ELAC	D665-D4	M
EMPIRE	4000D/III	M
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	440D	
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JVC	X–I	M
	4MD–20X	VM
	4MD–30X	VM
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ORTOFON	SL–15Q	MC
PANA-SONIC	EPC–450C–II	SC
	EPC–451	SC
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PICKERING	XUV/4500Q	M
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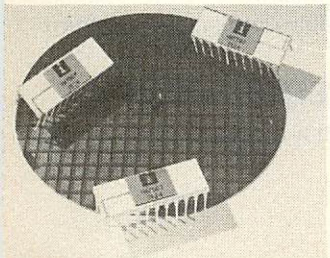
M: Magnetic
MC: Moving Magnetic
IM: Induced Magnetic
IC: Integrated Circuit
SC: Semi-conductor
C: Ceramic
(Source: JVC information)

Intersil introduces 4096 bit NMOS dynamic RAM

The IM7507 is a new 4096 × 1 bit dynamic N channel MOS RAM being introduced by Intersil, Inc. It is a direct pin for pin replacement part for the TI 4060, the Intel 2107A and the Intel 2107B. The RAM is available in three speed options. The IM7507 provides 300 nanosecond maximum access time; the IM7507-1, 250 nS; and the 7507-2, 200 nS maximum access.
The devices are available in 22 pin



DIP packages. In 100-999 quantities, price for the IM7507 is $ 24.25, for the IM7507-1, $ 26.90; and for the IM7507-2, $ 29.25.
All inputs for the IM7507 except for chip enable are TTL compatible and require no pull-up resistors. The memory's output is three state and also TTL compatible.
Intersil, Incorporated
10900 North Tantau Ave.
Cupertino, CA 95014

AC-DC absolute calibrators

Optimation Inc., announces the introduction of two Absolute Calibrators which provide high precision AC and DC calibration in a single unit.
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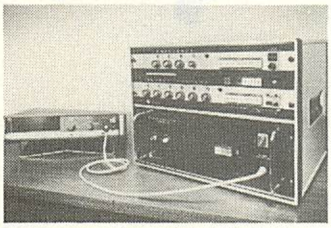
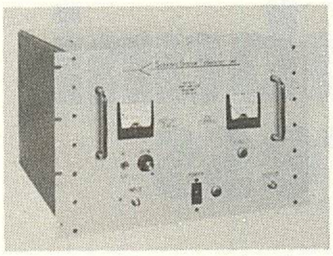


racy ranges from ±0.01% over 50 Hz to 20 kHz, to ±0.2% over 0.1 MHz to 1.1 MHz, with no other frequency range exceeding ±0.05%. AC and bipolar DC frequency ranges extend from 10 nV to 100 V in six decade ranges with six-place settability and 20% over-ranging. Frequency extends from 10 Hz to 1.1 MHz through the 10 V range and to 100 kHz through 100 V.
Optimation's PA-226 high-voltage amplifier can extend ranges on both AC and DC to 1200 volts. The complete AC-DC systems' initial investment cost is $ 5,995 (PA-226 amplifier as shown $ 3,450).
Optimation, Inc., 9259 Independence Ave., Chatsworth, California, 91311.

Power amplifiers

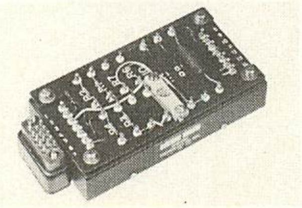
The A 7200 A2-2 linear power amplifier is designed to meet high power needs of various applications. The A 7200 A2-2 provides excellent test equipment capabilities for RFI/EMI testing, ultrasonics, vibration, sonar and calibration covering the frequency range of 50 KHz-10 MHz, amplifying a one volt signal at 50 ohms to 400 watts of output power into a 50 ohm load.
The A 7200 A2-2 amplifier contains overload protection, features



complete solid-state construction, requires no tuning and has self-contained metering. The A 7200 A2-2 features low distortion, low cost and the ability to drive reactive loads.
The A 7200 A2-2 weighs 125 pounds, is 12 1/4 inches high, 19 3/4 inches deep, mounts in a standard 19 inch rack and the front panel knob provides more than 50 dB gain control.
Other models are available from 100 to 400 watts and in frequency ranges from 10 KHz to 30 MHz. Custom units are available at off the shelf prices.
Scientific System Technology, Inc., 603 Business PKWY., Richardson, Texas 75080

110 watt DC power amplifier

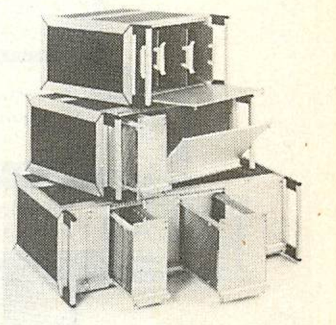
The model 916 is a DC power amplifier featuring differential input and differential output. With its power sharing circuitry, the amplifier is capable of delivering 110 Watts output as an integral unit. Adjustable current limiting is provided to prevent motor demagnetization due to the back E.M.F. when reversing at high speed. This circuit also protects the amplifier against an accidental momentary short circuit across the output terminals. Stable operation with either voltage feedback or current feedback is achieved even with very high open loop gain. The amplifier is intended for use in



DC control systems. The Model 916 is supplied with a removable component board mounted on top of the amplifier. Input impedance, amplifier gain, voltage or current feedback, and current limiting can be set by adjusting the value of the resistors on the board. The amplifier is constructed as a 'Plug In' unit and measures only 4.70 × 2.75 × .94 inches H. It draws the bulk of its power from the 28 VDC line and also requires 10 mA from a 15 VDC supply. Connections to the amplifier can be made either by solder terminals or by means of a plug-in connector. This connector can be oriented for plug-in from above, as shown or from below or for horizontal plug-in configuration. Because of its versatility, this power amplifier is useful in applications requiring precise control of Position, Velocity or Torque. Complete application notes showing how it is used are available.
Control Technology Co., Inc., 41-16 29th Street Long Island City, N.Y. 11101

Additions to card frame 4

As part of their introduction of the Eurocard system, Vero Electronics Limited have now released a range of clad card frames in a 3U height and a variety of widths. Each unit consists of a basic card frame together with a set of covers comprising a top cover without ventilation slots, a bottom cover with ventilation slots, a rear cover and two side covers together with side extrusions and four feet. This is supplied in kit form, but assembly is extremely simple and rapid.



Card guides and connector mounting strips are supplied separately. The rear cover is removable to permit the fixing of connector mounting strips. These units can also be fitted with attractive front handles which are supplied separately and reduce the total front panel width by 2E (1E = 5.08 mm). Standard front panel widths are 42E, 60E and 84E.
These assemblies are designed to accept any standard 100 × 160 mm Eurocard and also the wide range of modules and front panels which are already available as part of the Vero Card Frame System 4. Standardisation on Eurocards is already widely accepted in Europe and more and more companies in the U.K. are also looking to this system for the future.
England: Vero Electronics Limited, Industrial Estate, Chandlers Ford, Eastleigh, Hants; USA: Vero Electronics Inc., 171 Bridge Road, Hauppauge, New York, 11787 USA.

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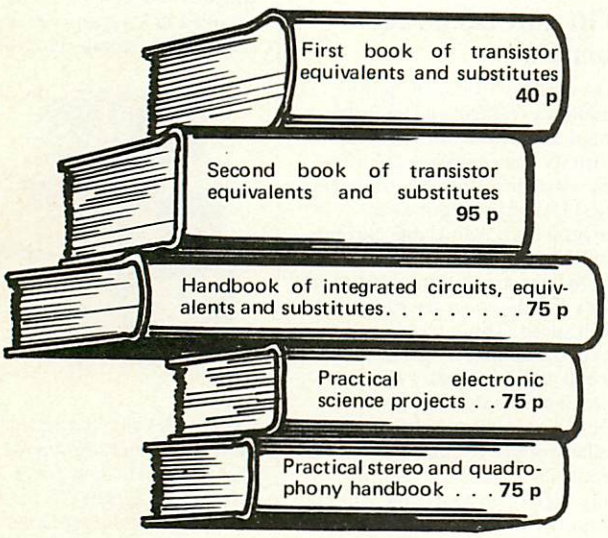

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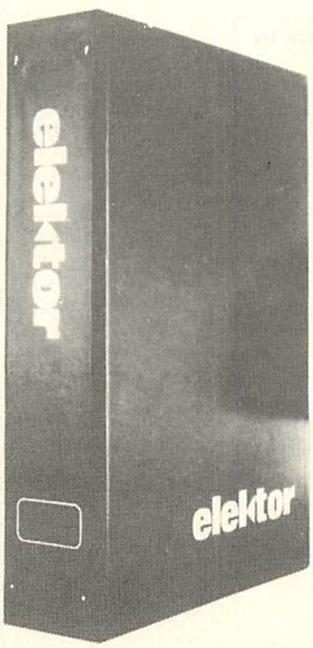

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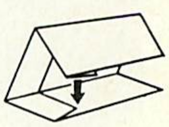

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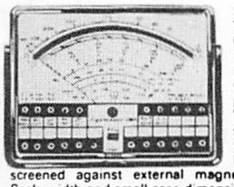

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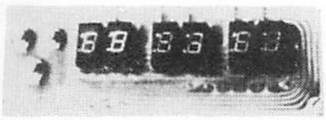

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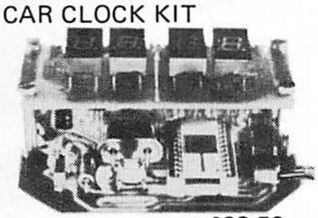

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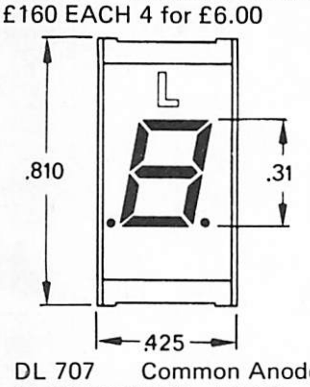

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