ELEKTOR 21

Elektor Decoder

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What is a TUN?
What is a 10 n?
What is the EPS service?
What is the TQ service?
What is a missing link?

Semiconductor types

Very often, a large number of
equivalent semiconductors exist
with different type numbers. For
this reason, 'abbreviated' type
numbers are used in Elektor
wherever possible:
- '741' stands for µA741,
LM741, MC741, MIC741,
RM741, SN72741, etc.
- 'TUP' or 'TUN' (Transistor,
Universal, PNP or NPN re-
spectively) stands for any low
frequency silicon transistor
that meets the specifications
listed in Table 1. Some
examples are listed below.
- 'DUS' or 'DUG' (Diode, Uni-
versal, Silicon or Germanium)
stands for any diode that meets the speci-
fications listed in Table 2.
- 'BC107B', 'BC237B',
'BC547B' all refer to the same
'family' of almost identical
better-quality silicon transis-
tors. In general, any other
member of the same family
can be used instead. (See
below.)

For further information, see
'TUP', TUN, DUG, DUS',
Elektor 20, p. 1234.

Table 1. Minimum specifications
for TUP (PNP) and TUN (NPN).

V_{CEO}, max	20V
I_C, max	100 mA
h_{fe}, min	100
P_{tot}, max	100 mW
f_T, min	100 MHz

Some 'TUN's are: BC107, BC108
and BC109 families: 2N3856A,
2N3859, 2N3860, 2N3904,
2N3947, 2N4124. Some 'TUP'
are: BC177 and BC178 families;
BC179 family with the possible
exception of BC159 and BC179;
2N2412, 2N3251, 2N3906,
2N4126, 2N4291.

Table 2. Minimum specifications
for DUS (silicon) and DUG
(germanium).

	DUS	DUG
V_R, max	25V	20V
I_F, max	100mA	35mA
I_R, max	1µA	100 µA
P_{tot}, max	250mW	250mW
C_D, max	5pF	10pF

Some 'DUS's are: BA127, BA217,
BA218, BA221, BA222, BA317,
BA318, BAX13, BAY61, 1N914,
1N4148.
Some 'DUG's are: OA85, OA91,
OA95, AA116.

BC107 (-8, -9) families:

BC107 (-8, -9), BC147 (-8, -9),
BC207 (-8, -9), BC237 (-8, -9),
BC317 (-8, -9), BC347 (-8, -9),
BC547 (-8, -9), BC171 (-2, -3),
BC182 (-3, -4), BC382 (-3, -4),
BC437 (-8, -9), BC414

BC177 (-8, -9) families:

BC177 (-8, -9), BC157 (-8, -9),
BC204 (-5, -6), BC307 (-8, -9),
BC320 (-1, -2), BC350 (-1, -2),
BC557 (-8, -9), BC251 (-2, -3),
BC212 (-3, -4), BC512 (-3, -4),
BC261 (-2, -3), BC416.

Resistor and capacitor values

When giving component values,
decimal points and large numbers
of zeros are avoided wherever
possible. The decimal point is
usually replaced by one of the fol-
lowing international abbrevi-
ations:

p (pico-) = 10^{-12}
n (nano-) = 10^{-9}
µ (micro) = 10^{-6}
m (milli-) = 10^{-3}
k (kilo-) = 10^{3}
M (mega-) = 10^{6}
G (giga-) = 10^{9}
A few examples:
Resistance value 2k7: this is
2.7 kΩ, or 2700 Ω.
Resistance value 470: this is
470 Ω.
Capacitance value 4p7: this is
4.7 pF, or
0.000 000 000 004 7 F . . .
Capacitance value 10 n: this is the
international way of writing
10,000 pF or .01 µF, since 1 n is
10^{-9} farads or 1000 pF.

Mains voltages

No mains (power line) voltages
are listed in Elektor circuits. It is
assumed that our readers know
what voltage is standard in their
part of the world!
Readers in countries that use
60 Hz should note that Elektor
circuits are designed for 50 Hz
operation. This will not normally
be a problem; however, in cases
where the mains frequency is used
for synchronisation some modifi-
cation may be required.

Technical services to readers

- EPS service. Many Elektor
articles include a lay-out for a
printed circuit board.
Some — but not all — of these
boards are available
ready-etched and predrilled.
The 'EPS print service list' in
the current issue always gives a
complete list of available
boards.
- Technical queries.
Members of the technical staff
are available to answer tech-
nical queries (relating to
articles published in Elektor)
by telephone on Mondays
from 14.00 to 16.30.
Letters with technical queries
should be addressed to:
Dept. TQ. Please enclose a
stamped, self addressed envel-
ope ; readers outside U.K.
please enclose an IRC instead
of stamps.
- Missing link. Any important
modifications to, additions to,
improvements on or correc-
tions in Elektor circuits are
generally listed under the
heading 'Missing Link' at the
earliest opportunity.

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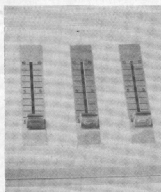
Despite its simple design the stereo audio mixer will accept inputs from microphone, magnetic cartridge, or 'flat' line sources.
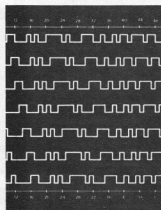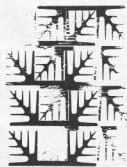
The noise generator described in this issue uses digital techniques to produce a pseudo-random binary noise signal. Suitable filtering converts this to analog 'white' or 'pink' noise.
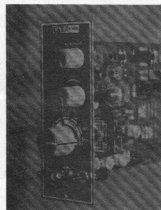
This photo of a Y-preamp illustrates the modular construction of the Elektorscope.

up-to-date electronics for lab and leisure

elektor 21

Not a microphotograph of snow crystals, but neatly packed heat-sinks!

STEREO AUDIO MIXER

This is a design for a simple but high-quality, portable, five-input, stereo mixer intended for use in discos or for tape recording. Despite its simple design the mixer will accept inputs from microphone, magnetic cartridge, or 'flat' line inputs.

The total current consumption is quite low, so the unit may be powered from batteries as well as its own, integral, mains power supply.

In the fields of application for which this mixer is intended it was felt that the cost, complexity and weight of such facilities as tone and balance controls were not justified. Such facilities are best left to the professional studio mixer.

A block diagram of one channel of the mixer is shown in figure 1. This is of course duplicated for the other channel. It can be seen that the first three inputs are each provided with a preamplifier,

and any or all of these preamplifiers can be constructed as either a disc or microphone preamp. The outputs of the preamplifiers feed into faders (gain controls). The two remaining inputs are intended to be fed from 'flat' sources such as tape, and these inputs are fed direct into the faders.

The outputs from all the faders are mixed (more properly 'summed') at the virtual earth input of the post amplifier, and the mixed output can then be fed

to the tape recorder, disco amplifier or whatever. The post amplifier, according to the whim of the individual constructor, may or may not be equipped with a master gain control.

Preamplifiers

Figure 2 is the complete circuit of one channel of the stereo mixer. The input preamplifier is constructed around T1 and T2, and is, of course, duplicated for inputs 2 and 3, though this is not shown in full. T1 functions as a voltage amplifier with a relatively high gain, and the noise figure is good due to the low collector current of approximately 86 μA.

T2 also operates as a voltage amplifier, but since the output signal is taken from its collector, the collector resistor must be fairly low to obtain a reasonably low output impedance that will not be unduly loaded by the fader P1.

Negative feedback is provided from the collector of T2 to the emitter of T1 via an equalisation network connected between points X and Y.

The networks for disc and microphone inputs are shown at the bottom of figure 2. Note that for the disc preamp R3 is 470 Ω, and for the microphone input, 1k5.

The two line inputs require little comment, since they simply feed direct into the faders P4 and P5. It is, of course, perfectly possible to convert any or all of the preamp inputs to line inputs simply by omitting the preamp components and joining points A and B.
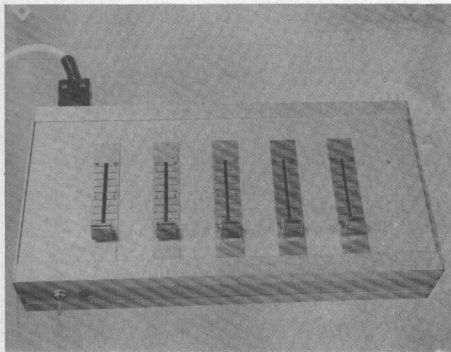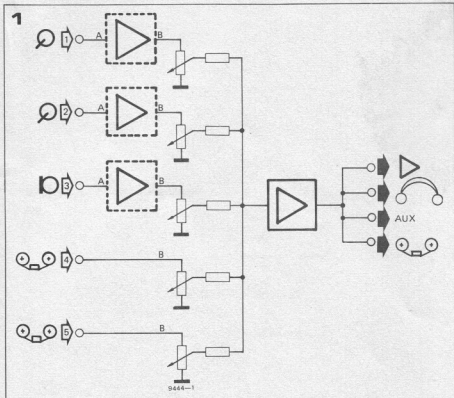
figure 1. Block diagram of one channel of the stereo mixer.

figure 2. Complete circuit of one channel of the stereo mixer.
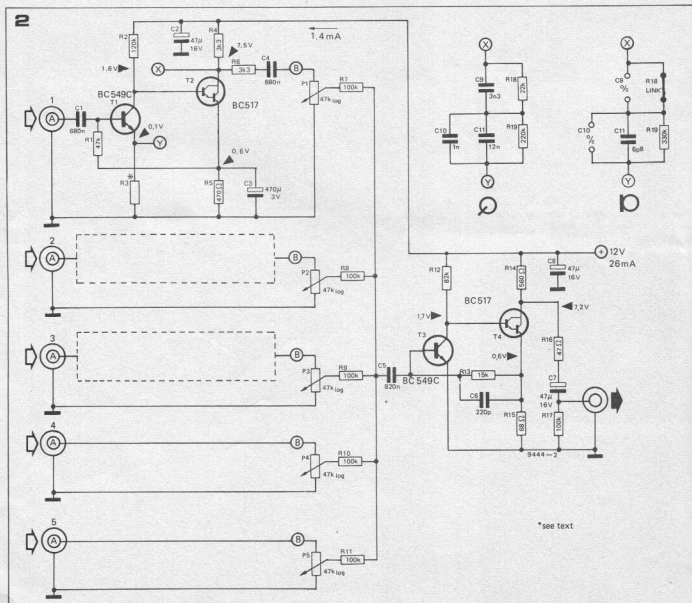
*see text
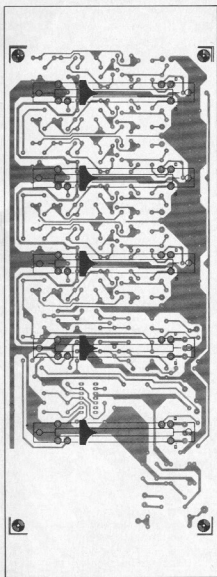
Photos 1 and 2. Showing how the potentiometers may be mounted direct on the back of the p.c. board.

RADIOHM N 75

47KB 0
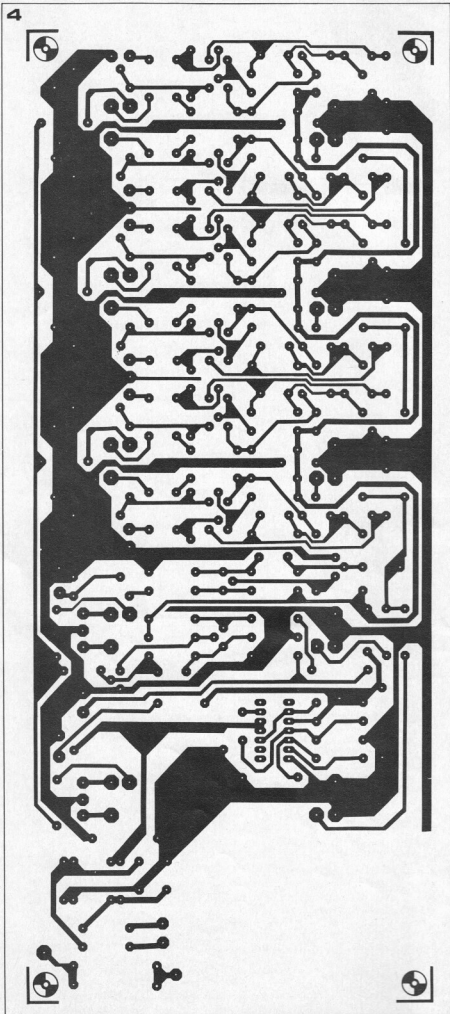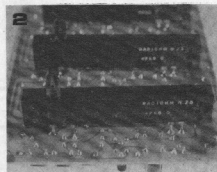
5
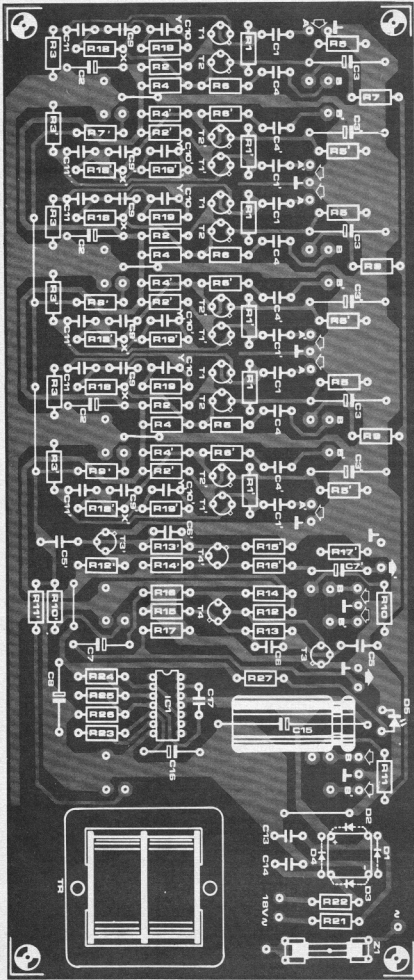
Parts list

Resistors:
R1 = 47 k
R2 = 120 k
R3 = 470 Ω DISC
1k5 MIC
R4,R6,R25 = 3k3
R5 = 470 Ω
R7 . . . R11,R17 = 100 k
R12 = 82 k
R13 = 15 k
R14 = 560 Ω
R15 = 68 Ω
R16 = 47 Ω
R18,R19 = see text
R21,R22,R24 = 10 Ω
R23 = 1k8
R26 = 4k7
R27 = 820 Ω

Capacitors:
C1,C4 = 680 n
C2,C7,C8 = 47 µ/16 V
C3 = 470 µ/3 V
C5 = 820 n
C6 = 220 p
C9,C10,C11 = see text
C13,C14 = 47 n
C15 = 470 µ/40 V
C16 = 10 µ/10 V
C17 = 100 p

Semiconductors:
T1,T3 = BC 549 C
T2,T4 = BC 517 (Darlington)
D1 . . . D4 = 4 x 1N4001 or
bridge rectifier B 40 C 400
D5 = LED
IC1 = 723 DIL

Miscellaneous:
Tr = 15 - 18 V/50 mA
(minimum) transformer
Z1 = 50 mA fuse
P1 . . . P5 = 47 k log. stereo-
slider potentiometer

figure 4. Printed circuit board for the mixer and power supply (EPS 9444).

figure 5. Component layout for figure 4.
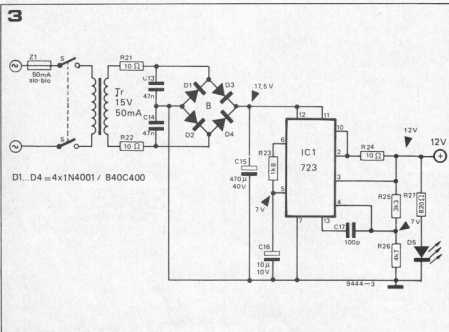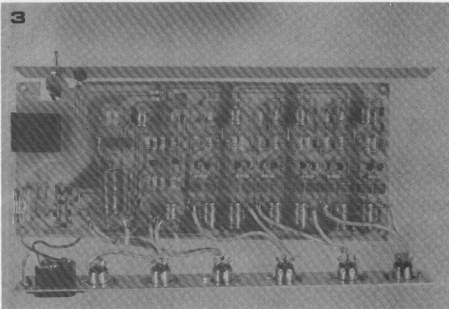
The outputs of the faders are connected to the input of the post amplifier via mixing resistors R7 to R11. To avoid any unwanted interaction between the input signals the a.c. voltage at the mixing node must be zero. This is basically what is meant by the term 'virtual earth': although the amplifier input is not actually grounded its input voltage is always very small. In other words the amplifier has a very low input impedance.

This result is achieved by applying a large degree of negative feedback from the emitter of T4 to the base of T3. When one of the input signals swings positive this will attempt to force more base current into T3. The collector of T3, and hence the emitter of T4, will swing negative until the current through R13 is the same as that through the input resistor (neglecting T3 base current), and the a.c. voltage at the input node will remain zero.

The overall gain of the post amplifier is the product of the gain of T3 (with feedback) and the gain of T4. This is

given by

$$\frac{R13}{R_{in}} \times \frac{R14}{R15}$$

i.e. about 1.25; R_{in} is one of the resistors R7 ... R11.

The output of the post amplifier is taken from the collector of T4, the output impedance being 600 Ω. If desired R17 may be replaced by a master fader control, though in many cases this will not be necessary as the succeeding equipment will have gain controls.

Power Supply

The power supply is based on a 723 IC regulator, with its output set to 12 V, and this is more than adequate to supply the small current taken by the mixer without the need for heatsinks or external transistors. Due to tolerances in the 723's internal reference voltage the output voltage may not be precisely

6a

9444 - 6a

b

9444 - 6b

c

9444 - 6c
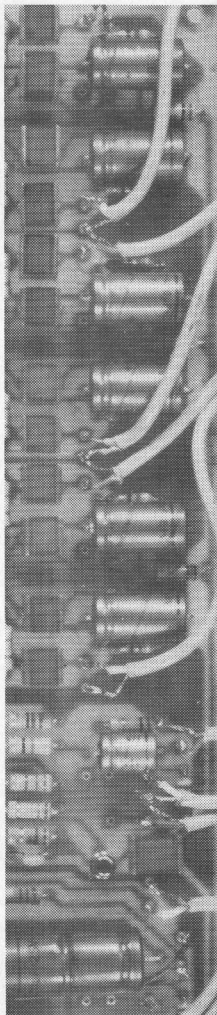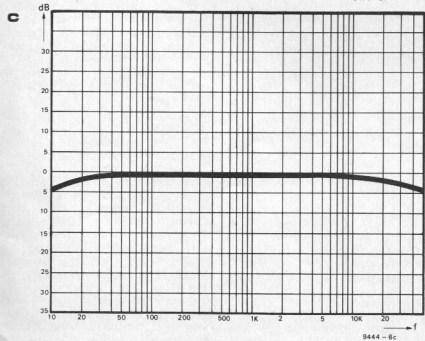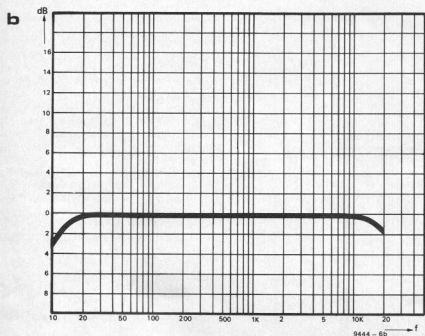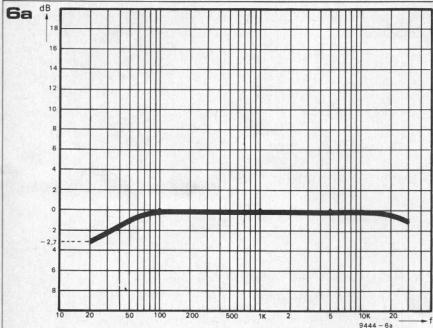
Photo 3. The completed mixer in its case with the lid removed.

figure 3. Power supply for the stereo mixer.

figure 6. Frequency response of the mixer for the disc (fed via reciprocal RIAA network) microphone and line inputs.

12 V, but this is no cause for concern.

Construction

A printed circuit board and component layout for the mixer are given in figures 4 and 5. It will be seen that the input preamplifiers are duplicated in three pairs, each numbered identically, the right channel components being identified by an apostrophe. When ordering components it must be remembered that for the input preamps 6 off are required of each component, and for the post amplifier, 2 off.

For the faders, slider pots of the RS Components, Doram or Radiohm type should be used, as these may be mounted direct on the back of the p.c. board as shown in photos 1 and 2. It should be noted that the sliders for the line inputs are mounted on the back of the board adjacent to the power supply, on either side of IC1. Provision is made for mounting the mains transformer on the p.c. board, and this should prove satisfactory. However, if hum on the inputs is a problem it may be necessary to mount the transformer remote from the board.

Input and output wiring should conform to normal audio practice, care being taken to avoid earth loops.

Performance and Applications

Figures 6a, b, and c show respectively the frequency response of the disc, microphone and line inputs. It would have been extremely easy to have extended the h.f. response into the MHz region, but bearing in mind the probable applications it was felt that this was simply inviting problems due to radio breakthrough and instability, especially in such applications as discos and tape recording where the layout of leads may be somewhat haphazard. For this reason the response is confined strictly to the audio spectrum by the inclusion of C6, and C12 in the microphone preamp.

The mixer may be used with most types of magnetic cartridge and dynamic microphone, as well as with high-level sources such as cassette decks, tape decks and tuners. With high output cartridges it may be found that overloading of the preamp occurs, and the cure for this is simply attenuation of the cartridge output so that the preamp reaches maximum output only on peaks.

MARBLES

Playing marbles is still one of the most universal of childhood pleasures. In this modern day and age, it was only a question of time before some designer tried his hand at designing an electronic equivalent . . .

There are any number of different games that can be played with marbles. This electronic version simulates one particular variant: the object is to roll the marble towards a wall, and the person whose marble ends up closest to the wall is the winner. It doesn't matter whether it bounces off the wall first — the only thing that counts is the final position.

In the electronic version, the rolling marble is simulated by an up/down counter driving a column of LEDs (figure 1). It is 'rolled' by pressing the start button; the length of time the button is depressed corresponds to the initial speed and this is where some skill is called for. Initially, LED 1 is on. As soon as the button is pushed this LED goes out and LED 2 lights up; then this, in turn, goes out and LED 3 lights and so on. The speed with which the point of light moves up the column depends on how long the start button is held down.

Since real marbles don't keep rolling at the same speed all the way, some 'friction' has been built in: the point of light slows down gradually until it finally comes to a standstill. One LED is now on, corresponding to the final position of the marble. The three LEDs across the top of the column are the 'wall' against which the 'marble' bounces, so the object of the exercise is to end up with LED 16 lit up.

Pushing the reset button resets the counter, so that LED 1 is lit up ready for the next try.

The circuit

The basic operation of the circuit is as follows. When the start button is depressed an oscillator is started. The initial frequency depends on how long the button is held down, and after it is released the frequency of the oscillator gradually decreases until it finally stops. The output from the oscillator drives the up/down counter (see figure 1). The four-bit output from this counter is passed to a decoder which drives the LEDs.

The complete circuit is shown in figure 2a and 2b. T1 and T2 are the oscillator — in this case, a fairly standard multivibrator circuit. The frequency is

1

9753-1

Reset   Start
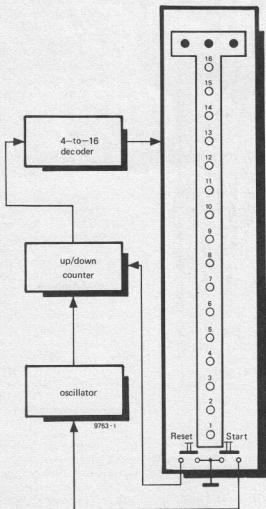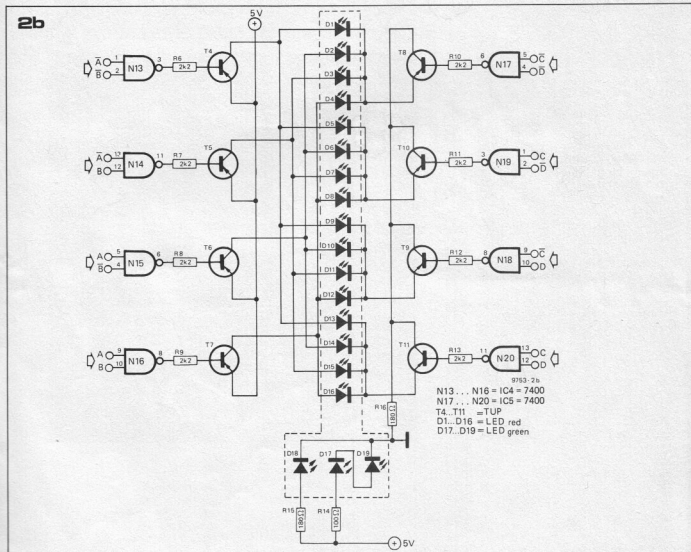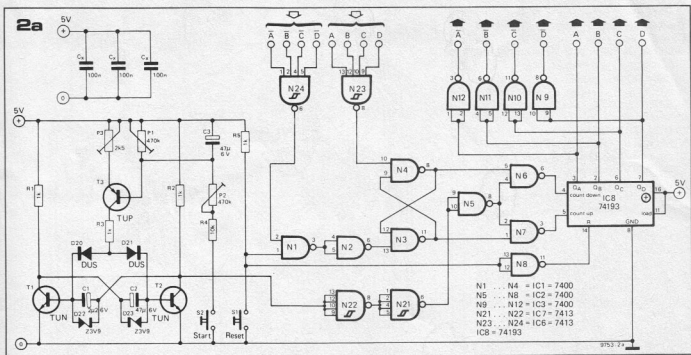
Figure 1. Block diagram of 'electronic marbles', showing the layout of the LEDs.

Figure 2. The complete circuit diagram. Figure 2a is the oscillator and counter with associated logic; figure 2b is the decoder/driver.

determined by the setting of current source T3, or, to be more precise, on the base voltage of this transistor. When the start button is depressed C3 charges up. The higher the voltage across C3, the higher the frequency of the oscillator — and the longer it will take for the capacitor to discharge.

The rate of charge of C3 can be preset with P2, so this sets the ratio between the initial speed and the length of time the button is held down. The discharge time depends on the setting of P1 — the 'friction' adjustment. P3 is the actual

'marble speed' control.

The output at the collector of T2 is not a particularly good square-wave, so it is 'polished up' by two Schmitt-triggers (N22 and N21) in cascade.

The up/down counter (IC8) has two inputs, one for 'count up' and one for 'count down'. Which of these inputs is driven by the oscillator depends on the state of the RS-flip/flop N3/N4.

When the output of N3 is at logic '1', N7 is freed and the counter counts up; when the output of N4 is 'high', the counter counts down.

When the reset button is depressed, the flip/flop is reset to the condition where the output of N3 is '1'. The counter will now count up until it reaches the maximum count (1111). At this point the output of N23 changes from '1' to '0'. This low-level input to N4 sets the flip/flop. The output of N4 is now 'high' and the counter counts down. When it reaches the lowest count (0000) the output of N24 goes 'low', resetting the flip/flop again so that the counter starts to count up again. The result of all this is that the counter counts up and down continuously until the oscillator stops.

The '4 - to - 16' decoder and the LED drivers are shown in figure 2b. The number of components required has been reduced by incorporating two tricks: the LED drivers are part of the decoder, and the decoder actually consists of two '2 - to - 4' decoders instead of one '4 - to - 16' type. For a particular LED to light up, the left-hand transistor connected to its anode and the right-hand transistor connected to its cathode must both be conducting. The left-hand transistors are driven by the A and B outputs of the counter, as decoded by N13 through N16, and the right-hand transistors are driven by the C and D outputs through a similar decoder (N17 through N20).

The transistors are connected to the LEDs in such a way that the final result is the desired '4 - to - 16' decode. To give one example, if the counter output is '1100' (A = 0, B = 0, C = 1 and D = 1) corresponding to a count of 12, the thirteenth LED should light up — remember that '0000' corresponds to LED 1! In this case the output of N13 will be low, turning on T4. At the same time the output of N20 will also be low, turning on T11. T4 is connected to D1, D5, D9 and D13, whereas T11 drives D13, D14, D15 and D16. The only LED connected to both transistors is D13, so it lights up, as intended.

LEDs D17, D18 and D19 are the 'wall'.

NOISE GENERATOR

Usually, noise is something we want to get rid of.
However, there are applications in which noise is turned to practical use, such as for measuring and testing audio systems.
A digital method of generating so-called pseudo-random 'white' and 'pink' noise is described in this article and applied in a practical circuit.

Noise is one of the oldest known and still the most fascinating signals in modern electronics. It is a signal which apparently varies at *random* with time. 'Apparently', because certain laws of probability and statistics are obeyed. These mathematical backgrounds provide us with quantities which can accurately define such a signal. They say something about the probability of a certain value being assumed, and become relevant only after the noise signal has been observed during a long period.

An example of such a mathematical quantity is the mean square value of the noise voltage, $\overline{v^2}$. The root is the root mean square (RMS) value of the noise voltage.

White noise

For one class of noise signals the mean square value of the noise voltage is defined by:

$$\overline{v^2} = c\, \Delta f,$$

where $\Delta f = f_2 - f_1$, the difference between the highest and the lowest frequency of the frequency band under consideration (see figure 1). The factor c says something, or rather everything, about the power density spectrum.

If c is frequency-independent, the power density spectrum is constant. This means that all frequencies are then represented equally in the noise. The quantity $\overline{v^2}$ increases with the band-width Δf. This type of noise signal, where c is constant, is called 'white noise'.

The term 'coloured noise' is used for signals where c is frequency-dependent within the frequency range under consideration.

Note that in practice, due to physical limitations, noise can only be 'white' in a band-limited frequency range. If Δf were to become infinitely large while c remained constant, the signal power $\overline{v^2}$ would also become infinitely large.

Pink noise

One form of coloured noise is 'pink' noise. Both pink and white noise are useful in audio and acoustic measurements. To determine the frequency response of a system, a suitable noise signal is fed to the input. When the output is passed through a band-pass filter with a given central frequency and bandwidth, the r.m.s. value of the noise voltage corresponding to that particular frequency band will be measured. By using several band-pass filters with suitable quality factors and central frequencies, the entire relevant frequency response of the system can be measured.

1. For *filters with a constant bandwidth* the quality factor Q increases proportionally with the central frequency f_c.
   If a noise signal is measured with bandfilters of this type, the r.m.s. value of the output voltage measured for *white* noise is constant for each bandfilter.

2. For *filters with a constant quality factor* Q the bandwidth B increases with the central frequency f_c. A well-known example of this type are the so-called 'octave filters', where the ratio between the highest and the lowest bandpass frequency is 2. 'Third octave filters' are also in common use. If white noise is applied to a system with a 'flat' frequency response, selective measurement at the output with this type of filter will show that the r.m.s. value of the measured voltage increases in proportion to the square root of the central frequency. This is equivalent to saying the frequency characteristic rises at + 3 dB per octave.

To correct for this, it is necessary to include a low-pass filter with a slope of - 3dB per octave.

This filter is connected between the white noise generator and the

Figure 1. The frequency spectrum of a band-limited 'white' noise signal. The r.m.s. value of the noise voltage in a range Δf between f_1 and f_2 is proportional to the square root of Δf.

Figure 2. An n-bit shift register in combination with suitable EXOR-feedback will produce pseudo random binary noise.

$$Q_0 = \overline{Q}_n \cdot Q_m + Q_n \cdot \overline{Q}_m$$

Table 1

t/T_k	Q0	Q1	Q2	Q3	Q4	Q5	Q6	decimal
0	0	1	1	1	1	1	1	63
1	0	0	1	1	1	1	1	62
2	0	0	0	1	1	1	1	60
3	0	0	0	0	1	1	1	56
4	0	0	0	0	0	1	1	48
5	1	0	0	0	0	0	1	32
6	0	1	0	0	0	0	0	1
7	0	0	1	0	0	0	0	2
8	0	0	0	1	0	0	0	4
9	0	0	0	0	1	0	0	8
10	1	0	0	0	0	1	0	16
11	1	1	0	0	0	0	1	33
12	0	1	1	0	0	0	0	3
13	0	0	1	1	0	0	0	6
14	0	0	0	1	1	0	0	12
15	1	0	0	0	1	1	0	24
16	0	1	0	0	0	1	1	49
17	1	0	1	0	0	0	1	34
18	0	1	0	1	0	0	0	5
19	0	0	1	0	1	0	0	10
20	1	0	0	1	0	1	0	20
21	1	1	0	0	1	0	1	41
22	1	1	1	0	0	1	0	19
23	1	1	1	1	0	0	1	39
24	0	1	1	1	1	0	0	15
25	1	0	1	1	1	1	0	30
26	0	1	0	1	1	1	1	61
27	0	0	1	0	1	1	1	58
28	0	0	0	1	0	1	1	52
29	1	0	0	0	1	0	1	40
30	1	1	0	0	0	1	0	17
31	1	1	1	0	0	0	1	35
32	0	1	1	1	0	0	0	7
33	0	0	1	1	1	0	0	14
34	1	0	0	1	1	1	0	28
35	0	1	0	0	1	1	1	57
36	0	0	1	0	0	1	1	50
37	1	0	0	1	0	0	1	36
38	0	1	0	0	1	0	0	9
39	1	0	1	0	0	1	0	18
40	1	1	0	1	0	0	1	37
41	0	1	1	0	1	0	0	11
42	1	0	1	1	0	1	0	22
43	1	1	0	1	1	0	1	45
44	1	1	1	0	1	1	0	27
45	0	1	1	1	0	1	1	55
46	1	0	1	1	1	0	1	46
47	1	1	0	1	1	1	0	29
48	0	1	1	0	1	1	1	59
49	0	0	1	1	0	1	1	54
50	1	0	0	1	1	0	1	44
51	1	1	0	0	1	1	0	25
52	0	1	1	0	0	1	1	51
53	1	0	1	1	0	0	1	38
54	0	1	0	1	1	0	0	13
55	1	0	1	0	1	1	0	26
56	0	1	0	1	0	1	1	53
57	1	0	1	0	1	0	1	42
58	1	1	0	1	0	1	0	21
59	1	1	1	0	1	0	1	43
60	1	1	1	1	0	1	0	23
61	1	1	1	1	1	0	1	47
62	1	1	1	1	1	1	0	31
63	0	1	1	1	1	1	1	63

Figure 3

Spectrum axes: $\overline{v^2}$ versus f, with markings at $\frac{f_k}{N}$, $\frac{2f_k}{N}$, f_k, $2f_k$, $3f_k$, $4f_k$, $5f_k$.   9487-3

system. The noise signal at the output of this filter is called *pink noise*.

How do we make noise?

This may sound like a ridiculous question considering the fact that the major problem in audio is usually how to get rid of it. However, what is meant is: how can we make noise with the greatest possible spectral purity? And that is something quite different.

White noise can be derived from the noise produced by the BE junction of a transistor which is reverse-biased into the break-down region. This produces a very low-level signal which must be amplified, and the $\frac{1}{f}$ - noise of the amplifier may be a problem. The signal-to-noise ratio of the amplifier must be very high. An even greater problem is that this type of noise is of thermal origin. The noise (r.m.s. value) is sensitive to temperature variations.

Pseudo random noise

Pseudo random noise, unlike random noise, consists of a periodical repetition of a specific random noise pattern. As an example, imagine that a true random noise signal is recorded on a closed loop of tape. When this tape is played back, the output will be pseudo random noise. An advantage of using pseudo random noise as a test signal is that the measuring time need not be infinitely long. (Theoretically, this is a requirement when measuring with true random noise . . .).

Pseudo random binary noise

It is not too difficult to generate pseudo random noise using digital techniques. A pseudo random binary noise signal is passed through a suitable low pass filter to give the analog noise required. It will be shown that both the binary and the analog noise signal are sufficiently 'noisy'.

The cycle character of pseudo random noise results in a repetition rate T_0 of the analog noise (T_0 is the period of one noise pattern), and as a cycle time T_0 for the binary noise.

Figure 2 gives the block diagram of a binary pseudo random noise generator. The n flipflops FF$_1$ . . . FF$_n$ are cascaded thus forming an n-bit shift register.

The register is shifted by a clock pulse with period time T_k and frequency f_K.

Since the continuous clocking of only 'zeros' or 'ones' into the shift register will certainly not lead to the required

Figure 4

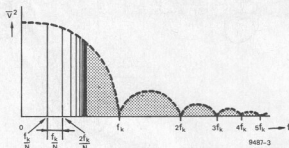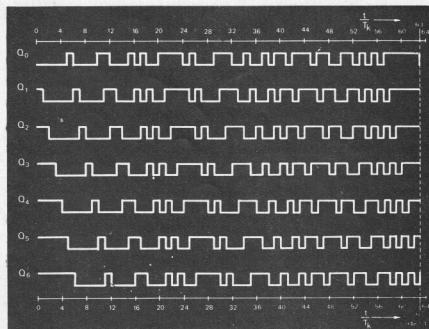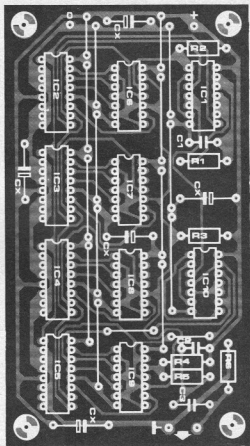Pulse diagram with traces Q_0, Q_1, Q_2, Q_3, Q_4, Q_5, Q_6 against axis $\frac{t}{T_k}$.

Table 1. The truth table for one complete cycle of a 6-bit shift register with EXOR-feedback from the outputs Q5 and Q6.

Figure 3. The frequency spectrum of pseudo random binary noise.

Figure 4. The pulse diagram corresponding to table 1.

Figure 5. The circuit diagram of the white noise generator. N9 . . . N29, N3 and N4 are needed to terminate the 'all-zero' output condition.

binary noise signal, the first flipflop FF_1 should receive a digital signal which is in some way related to the logic state of the register. The input of FF_1 receives a signal Q_0 which is related to the signals Q_n and Q_m, according to the following truth table:

Q_n	Q_m	Q_0
1	0	1
0	1	1
0	0	0
1	1	0

The objective now is to choose values for n and m such that the maximum number of different output states of the flipflops FF_1 . . . FF_n is achieved. This corresponds to the maximum cycle time of the shift register.

This requires some further explanation. The shift register consists of n flipflops, and each of the n Q-outputs can be considered as one bit of an n-bit binary number represented by the contents of the shift register.

If the n flipflops are read out in parallel in the sequence $Q_n, Q_{n-1} \ldots Q_1$, we get an n-bit number corresponding to a given decimal number. The state of Q_1 corresponds to the value of the least significant bit (LSB) *), the state of Q_n corresponds to the most significant bit (MSB) *).

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*) The concepts LSB and MSB indicate the place of the bit in the number. They are a measure of the weighting factor allocated to the value of the bit concerned. The MSB is to the extreme left and in the case of an n-bit binary number it indicates (0 or 1) x 2^{n-1}. The LSB indicating the units (0 = even, 1 = odd), is to the extreme right, and has the lowest weighting factor for whole numbers. In the decimal number 1976, digit 1 is the MSB (thousands), and 6 the LSB (units).

The whole can be regarded as a counter that counts in a seemingly random sequence. The choice of m should be such, that all possible binary 'numbers' occur within a corresponding number of clock pulses. All possible numbers occur only once within the cycle period T_0. This maximum number of logic states is

$$N = 2^n - 1.$$

This is one less than the absolute maximum because an 'all-zero' output has to be avoided, since this would otherwise continue infinitely.

The (maximum) cycle time T_0, corresponding to this maximum number of states N is:

$$T_0 = N T_k.$$

If, for a given number of flipflops n, feedback takes place from Q_n and a randomly selected Q_m, there is a good chance that the cycle will be shorter than the maximum cycle time $N T_k$. It is very difficult to find values of m, corresponding to the selected n, in such a manner that the cycle time is maximum.

Fortunately this work has already been done for us.

Table 2 shows which outputs of the register should be used for the EXOR-feedback, for registers up to a maximum length $n = 33$. The last column also gives the corresponding cycle time expressed in clock periods T_k.

From table 2 it can be seen that there are always at least two possibilities: either Q_{n-m} or Q_m can be used. In table 2 Q_{n-m} is shown in brackets.

In a number of cases it is necessary to have EXOR-feedback from four Q-outputs. For n = 8, for example, the feedback condition is:

$$Q_0 = Q_2 \oplus Q_3 \oplus Q_4 \oplus Q_8$$

The $\oplus$ sign indicates the exclusive OR-function.

Table 1 shows the truth table for a 6-bit shift register with a cycle time of 63 clock pulses. The number in the first column gives the order in which the 'random' numbers appear at the output.

5

IC1,6...10 = 14; = 7
N1 . . . N4 = IC1 = 74132
IC2 . . . IC5 = 7496
N5 . . . N8 = IC10 = 7400
N9 . . . N13,N29 = IC6 = 7405
N14 . . . N18 = IC7 = 5/6 7405
N19 . . . N23 = IC8 = 5/6 7405
N24 . . . N28,N30 = IC9 = 7405

$C_x = 2\mu2/16V$

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6

The second column lists the EXOR information Q_0 which is fed to the first flipflop. The next six columns indicate the output from the 6 flipflops and the last column gives the decimal value of the 6-bit binary number, where Q_1 represents the LSB and Q_6 the MSB. Table 1 and the pulse diagram of figure 4 both clearly illustrate that the circuit is basically a shift register: the bits move one step to the right at each clock pulse. After 63 clock pulses the register is back at its initial state.

The pseudo random character of the output states is expressed as follows:

1. Of the total of N clock periods in one cycle, any particular Q output is 'high' during (N+1) :2 periods, and low during (N−1) :2 clock periods. This is because the zero state of the register is excluded. As n, and with it N, increases, the chance of a logic '0' approaches the chance of a logic '1' (50%).

2. If by traject we mean the number of clock periods within which the logic state of a particular Q output does not change, there are (N+1) : 2 trajects in each complete cycle. Half of these trajects are equal to one clock period; one quarter are equal to two clock periods, one eighth are equal to three clock periods, and so on. There is also one traject that is equal to n clock periods.

3. The number of trajects of each length is equally divided over trajects with logic '0' and ditto with logic '1'; the

Parts list

Resistors
R1 = 390 Ω
R2, R3, R4, R5 = 1 k
R6 = 100 k

capacitors
C1 = 4n7
C2 = 6n8
C3 = 1 μ
Cx = 2μ2/16 V

semiconductors
IC1 = 74132
IC2, IC3, IC4, IC5 = 7496
IC6, IC7, IC8, IC9 = 7405
IC10 = 7400

Table 2. A survey of possibilities and connections for feedback shift registers with bit lengths ranging from 3 to 33.

Figure 6. The printed circuit board and component layout for the circuit of figure 5.

Figure 7. The circuit of a passive low-pass filter with a slope of 3 dB per octave. If white noise is applied to this filter, pink noise is produced at the output.

Figure 8. Frequency response of the filter of figure 7.

traject of n-1 clock periods occurs in '0' only and the traject of n clock periods occurs in '1' only. These rules can be verified by means of table 1 and figure 4.

The design described here (figure 5) uses a 20-bit shift register with EXOR feedback from the outputs Q_{17} and Q_{20}. The cycle duration is 1,048,575 (see table 2). It would be possible to set up the truth table, as was done for the 6-bit register in table 1. However, such a truth table would comprise 23 columns instead of the 9 in table 1, meaning that it would be nearly three times as wide. The number of lines becomes 1,048,576 instead of the 64 of table 1, which means that the truth table becomes more than 16,000 times as long. Since table 1 occupies a full column of an Elektor page, this truth table would cover over 16,000 pages. So as not to make this article unnecessarily long, we have refrained from publishing the table in question. . . .

The cycle time T_0 of the above-described shift register counter with maximum cycle time can be extended considerably. At n = 33 (see table 2) and a clock pulse frequency of 10 MHz ($T_k = 0.1$ μs) it takes about 859 seconds (almost 15 minutes) before the cycle is completed. If, instead, a clock period of 1 second is used ($f_k = 1$Hz), the cycle time would be equal to about 8.6 x 10^9 seconds, considering that one year takes on average 60 x 60 x 24 x 365.25 = 31,558 x 10^6 seconds, it would take

over 270 years to complete the cycle!
Chances are that this exceeds the life of
the hardware constituting the equip-
ment.

The frequency spectrum

Figure 3 is an attempt to illustrate the
power density spectrum of the pseudo
random binary noise on the Q-outputs.
This spectrum is not continuous, but
consists of an infinite number of lines.
The spacing between the lines (fre-
quency difference) equals

$$f_0 = \frac{1}{T_0} = \frac{f_k}{N},$$

so that the spectrum consists of the fre-
quencies

$$0, \frac{f_k}{N}, \frac{2f_k}{N}, \frac{3f_k}{N}, \text{etc.}$$

The envelope of the frequency spectrum
varies according to the function
$\left(\frac{\sin x}{x}\right)^2$,

x being related to the ratio between f
and f_k. The spectrum contains no com-
ponent for f_k and multiples thereof.
It can be calculated that the power
spectrum has dropped 3 dB at a fre-
quency equal to 0.45 x the clock fre-
quency f_k.
The spectrum is equivalent to a band-
limited white noise signal (within
0.1 dB) for frequencies between 0 and
$f_k/4\pi$ Hz. To be on the safe side, the
band can be limited to

$$f_g \leqslant \frac{f_k}{20}.$$

For the final design f_g was set about at
25 kHz, so that a clock frequency f_k of
about 500 kHz. This drives the clock
inputs (pin 1) of four 5-bit shift regis-
ters IC2 . . . IC5; these are cascaded to
form the 20-bit shift register.
The EXOR function is achieved by
means of the gates N5 . . . N8. Feedback
is taken from Q17 and Q20, in accord-
ance with table 2. The EXOR feedback
signal (the output of N5, Q_0) is fed to
the input of the shift register via in-
verter N3 and gate N4.
Point 1 of N4 is normally 'high' so that
the feedback signal arrives at point 9 of
IC2. However, if all 20 Q-outputs of
IC2 . . . IC5 are 'low', the input of in-
verter N29 become high. As a result point 1
of N4 goes low. A '1' is now fed into
the register so that the condition of
twenty zeros, which might occur due to
faults, is terminated.
The output is fed through a low-pass
filter (R4, R5, C2) with a cut-off fre-
quency f_g of about 25 kHz and a slope

The circuit

The final circuit is shown in figure 5.
Schmitt trigger gates N1 and N2 are
used as a clock pulse generator which
runs at 500 kHz.

of 6 dB per octave. The output im-
pedance is about 1k; the peak value of
the white noise voltage at the output is
about 4 V. It can be calculated that this
peak value is about 3.16 times the
r.m.s. value.
Consequently, this noise signal is emi-
nently suitable for testing loudspeakers
and amplifiers. If the drive level is set so
that no 'clipping' occurs (this is audible
as a change in the timbre of the noise),
the amplifier will deliver only 10% of its
maximum output power. This will
usually mean that the loudspeaker will
be in no danger of falling victim to the
measurements.
To conclude with, figure 7 gives a cir-
cuit for a 3 dB per octave low-pass
filter. This can be connected to the out-
put to convert the 'white' noise into
'pink'. It is strongly recommended to
use 5% capacitors and resistors. Figure 8
shows the frequency response of this
filter.

Table 2

length of shift register (n):	Exor feedback taken from outputs:		cycle time in clock periods T_k:
3	Q3	and Q2 (Q1)	7
4	Q4	and Q3 (Q1)	15
5	Q5	and Q3 (Q2)	31
6	Q6	and Q5 (Q1)	63
7	Q7	and Q6 (Q1)	
	or Q4 (Q3)		127
8	x)		255
9	Q9	and Q5 (Q4)	511
10	Q10	and Q7 (Q3)	1023
11	Q11	and Q9 (Q2)	2047
12	x)		4095
13	x)		8191
14	x)		16,383
15	Q15	and Q14 (Q1)	
	or Q4 (Q11)		32,767
16	x)		65,535
17	Q17	and Q14 (Q3)	131,071
18	Q18	and Q11 (Q7)	262,143
19	x)		524,287
20	Q20	and Q17 (Q3)	1,048,575
21	Q21	and Q2 (Q19)	2,097,151
22	Q22	and Q21 (Q1)	4,194,303
23	Q23	and Q5 (Q18)	
	or Q9 (Q14)		8,388,607
25	Q25	and Q3 (Q22)	
	or Q7 (Q18)		33,554,431
28	Q28	and Q3 (Q25)	
	or Q13 (Q15)		268,435,455
31	Q31	and Q3 (Q28)	
	or Q13 (Q18)		2,147,483,647
33	Q33	and Q13 (Q20)	8,589,934,591

x) This shift register length requires EXOR feed-
back from four outputs.

# AUDIO WATTMETER

J.Jacobs

Tantalized by the scent of more watts, potential buyers are often seduced by the over-glowing specifications that some manufacturers give for their amplifiers. On closer investigation, for instance, a '2 x 30 watt' amplifier may only by quoting music power, with the real power at no more than 20 watts sine power per channel, and with both channels being driven simultaneously the maximum power turns out to be only 2 x 14 watts. By means of the wattmeter described in this article, it is possible to determine the real output power of an amplifier (up to 140 watts per channel into a resistive load).

The important figure in an amplifier's power specifications is the total output power with both channels driven. One channel on its own may deliver more power than with its partner if the power supply is inadequate. Also remember that it is unwise to test an amplifier beyond its specification, in case the heat sinks, for instance, are only sufficient for running within the specified limit.

The actual output power of an amplifier can only be determined accurately by using an audio tone generator (signal source), an oscilloscope (to inspect the waveform), and an audio wattmeter. The wattmeter described here has been designed to have a wide frequency range (5 Hz-400 kHz) and is suitable for use up to 140 watts (into either 4 or 8 ohms).

Various Measuring Methods

The output power can be measured in various ways, as shown in figures 1,2
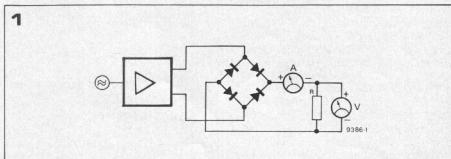
and 3. In the arrangement of figure 1, the output signal of the amplifier is rectified by a bridge rectifier and then fed to a load resistor (R) via an ammeter. A voltmeter is connected in parallel with the load resistor. The output power is calculated by multiplying together the current and voltage values given by the meters. The advantages of this method are its simplicity and wide frequency range; furthermore, it is only necessary to measure DC voltages and currents. However, the non-linearity of
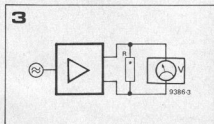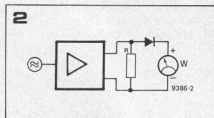
the rectifier and the meter often leads to inaccurate results.

Figure 2 shows a method where the output of the amplifier is connected directly to the load resistor R. This resistor is shunted by a rectifier and moving-coil instrument in series. The power can be read directly from the meter. The same comments that apply to figure 1 are also valid for this system, with the extra disadvantage that the indication is non-linear, so that a custom-calibrated scale is required.

Figure 3 shows a third possibility where an electronic AC voltmeter is connected in parallel with the load resistor R. This allows a high degree of accuracy because the non-linearity of the rectifier and the meter can now be compensated for by the electronics. The drawback with this system is that the output power is not presented as a direct reading: it must be calculated from the formula

$$P = \frac{V^2}{R}.$$

It is possible, of course, to calibrate one or two scales corresponding to specific resistance values (4 and 8 Ω, for instance).

From the above, it can be concluded

Figures 1, 2 and 3. Various ways of accurately determining the output power of an amplifier.

Figure 4. Detailed circuit diagram of the wattmeter, two of these circuits being required for stereo equipment.

Figure 5. A simple symmetrical power supply suitable for use as the current source for the wattmeter.

that each method has its drawbacks. However, the method shown in figure 3 has fewer disadvantages that the others, so it was chosen for the wattmeter described here.

The circuit

The amplifier under test is loaded by several resistors connected in series/parallel (figure 4). Instead of using high power 4 and 8 Ω resistors, which would be difficult to obtain, these values are approximated by the resistor networks shown. If 17 W types are used, the total power dissipated can be anything up to 140 W. Don't mount these resistors too close to each other or to a base board: they can get very hot! It is recommended that non-inductive resistors are used here – normal carbon resistors will do quite well.

The load resistance is selected with S2, which should preferably be a make-before-break type. Note that the position marked '600 Ω' only gives 600 Ω load impedance when S3 is in position 1. This facility has been included for dB measurements, where 0 dB corresponds to 0.775 V across 600 Ω (1 mW).

S3 is the range selector switch. With the resistance shown, the ranges will be sufficiently accurate. The '9 k' resistor is actually two 18 k resistors connected in parallel. The opamp is connected in a standard AC voltmeter configuration. The trick is that the opamp tries to maintain the same voltage on both its inverting and non-inverting inputs. The non-inverting input is connected to the input, and the inverting input 'sees' the voltage across the series connection of R1, P1 and C1. The opamp will therefore produce an output *current* that builds up exactly the right voltage (i.e. the input voltage) across this series connection.

The meter is connected in a bridge rectifier circuit in series with the opamp output. The output current must flow through the meter, and any non-

linearities of the diodes (or meter) are compensated for by the opamp. The (rectified AC) current through the meter is equal to

$$I_M = \frac{V_{in}}{R_1 + P_1},$$

provided the impedance C1 is negligable when compared to R1 + P1, at the lowest frequencies involved. This capacitor should be a non-polarised type or, if this is unavailable, two 1000 μ capacitors connected 'back-to-back' as shown in the diagram. The 47 n capacitor is necessary to maintain a low impedance at high frequencies. The pin numbering shown for the opamp refers to the TO or mini-DIL case style. The bandwidth is set by the compensation networks R2/C2 and C3. With the

5

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values shown it will be approximately 400 kHz.

Power Supply

The supply voltage used here for the opamp is approximately ±10 V. The current consumption of the circuit (even in the stereo version) is so low that a very simple supply is sufficient. Figure 5 gives a simple, symmetrical supply which is suitable. The two 100 n capacitors are for h.f. decoupling, and although they are shown in the power supply here, they should be located as close as possible to the opamp.

Calibration

The wattmeter is calibrated with P1.

The procedure is as follows.
1. Set S2 in the '600 Ω' position.
2. Set S3 in position 2.
3. Temporarily short out C1.
4. Connect a 2k2 resistor between the '+10 V' supply and the input.
5. Adjust P1 for full scale deflection (e.g. 3 Watts on the 4 Ω scale).
6. Remove the resistor and the short across C1.

It should be noted that the scale is not linear – it is square-law. As an example, if there are 10 divisions on the original (linear) scale on the meter, and full scale is now '300', the original markings will now correspond to '0', '3', '12', '27', '48', '75', '108', '147', '192', '243' and '300'.

Furthermore, when using the instru-

ment one must realise that the scale calibration is only valid for a sine-wave input. If the sine-wave sounds audibly distorted, the actual power output can be either higher or lower than the value indicated.

In general, one should not consider this unit to be 'precision instrument'. This is one of the reasons why precision resistors are not specified. However, no one should worry about the difference between, say, 100 W and 'only' 95 W – it just is not audible.

◄

4

	f.s.d. (volts)	f.s.d. (watts) 4 Ω	f.s.d. (watts) 8 Ω
5	35	300	150
3	11	30	15
2	3.5	3	1.5
1	1.1	0.3	0.15

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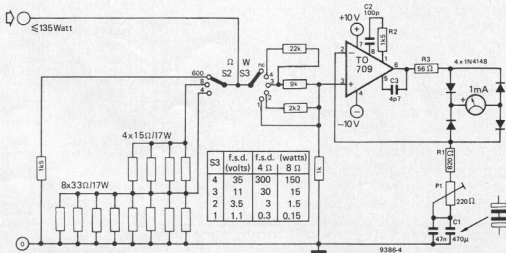
ELEKTORSCOPE PART 2

A linear timebase and stable trigger circuits are essential to the operation of an oscilloscope. Good linearity of the timebase ensures that there is no distortion of the displayed waveform along the X-axis, while stable triggering ensures a jitter-free display.

In this month's article the circuits of the timebase, trigger circuit, X and Y amplifiers, channel switches and Y-preamps are discussed.

Figure 1a, 1b, 1c, 1d

For the benefit of the less experienced reader the general principles of timebase and trigger circuits will briefly be discussed. The timebase output consists of a linear ramp or sawtooth voltage which is applied to the X plates of the oscilloscope, causing the trace to sweep horizontally across the screen in a linear fashion. Once the trace has been deflected across the entire screen width the ramp voltage drops rapidly to zero and the trace returns quickly to the starting position. To prevent the flyback or retrace from appearing on the screen the CRT beam current is cut off during this period, as mentioned earlier.

During the sweep the trace is deflected in a vertical direction by the signal applied to the Y plates, thus causing the input waveform to appear on the screen. If the timebase were allowed to free run with no trigger input then it is likely that the sweep would not start every time at the same point on the signal waveform. The portion of the signal waveform displayed during each sweep would thus be different, and the trace would appear to run one way or the other across the screen (figure 1A). In order to obtain a stable trace the timebase must not be allowed to free run but must be started at the same point on the waveform for each sweep. This is shown in figure 1B. The trigger circuit detects the amplitude of the waveform and also whether the slope is positive or negative-going — it would not do to have one sweep of the timebase triggered on a positive slope and the next sweep (at the same level) on a negative slope, since this would give rise to a mixed trace on the screen.

Where successive cycles of a waveform are of the same amplitude the trigger level is relatively unimportant and it is common practice to trigger near the zero-crossing point so that the trigger point does not vary if the signal amplitude changes (figure 1C). However, if the amplitude of successive cycles was not the same then triggering at the zero-crossing point would mean that successive cycles of differing amplitude would appear at the same point on the screen. In this case the timebase must be triggered only on the highest amplitude cycle of the waveform (figure 1D). The trigger circuit is thus provided with a trigger level control to ensure reliable triggering on any repetitive waveform.
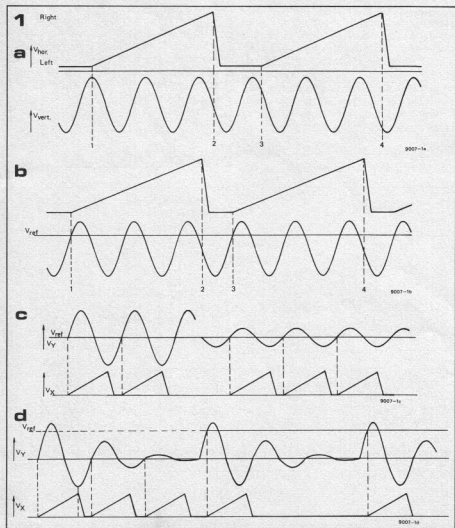
Figure 1. Showing the principle of a triggered timebase.

Figure 2. Block diagram of the Elektorscope timebase and trigger circuit.

Figure 3. Diagram of the trigger circuit.

Figure 4a. Circuit of the timebase.

2

1 = trigger amplifier
2 = polarity selector
3 = Monoflop
4 = automatic trigger
5 = sweep generator
6 = output stage

9007-2

3

IC2 = N1...N4=7400
IC3 = 74123

9007-3

LM311

Top view

* Tantalum

V+
8

Ground 1
Output 7
Input 2
Balance 6
Input 3
Balance 5
4
V−

4a

* Tantalum

AA119
(D6)

9007-4a

Figure 2 shows a block diagram of the trigger circuit and timebase. The output of the Y1 or Y2 preamp or an external signal may be selected as the trigger source. The trigger signal is compared with a continuously variable reference voltage (trigger level control). When the signal level exceeds the trigger level the output of the comparator goes high, and when the signal level falls below the trigger level the comparator output goes low.

A polarity selector determines whether the timebase shall trigger on the positive or negative-going edge of the comparator output. The selected edge triggers a monostable that produces a short, fixed-length pulse which triggers the sweep generator. Finally, the output of the sweep generator is buffered by an output stage which drives the X amplifier. With the timebase in the 'automatic' mode the timebase will free run in the absence of a trigger signal. This is particularly useful when observing DC levels which provide no trigger signal.

Trigger circuit

The complete trigger circuit is given in figure 3. T1 provides a fairly high input impedance and a gain of 4.7 to the input signal. The output from the collector of T1 is fed into the inverting input of an LM311 high speed comparator, while the non-inverting input is fed from the slider of P1 to provide the trigger reference level. A small amount of positive feedback is applied around the comparator via R12 to provide a regenerative or 'Schmitt Trigger' type of action to avoid trigger jitter on noisy waveforms.

Triggering of the timebase is performed by the upper of the two monostables IC3. This can only be triggered by a positive-going pulse, so this makes for easy selection of trigger polarity. With S5 in the 'pos.' position the comparator output is routed through N4 and N3 so that the timebase is triggered on a positive-going edge. With S5 in the 'neg.' position the output of the comparator is inverted by N1 (giving a positive pulse on the negative-going edge of the comparator output). The output of N1 is routed through N2 and N3 to the B input of the monostable. When the monostable is triggered it provides a short negative-going pulse to trigger the timebase.

The second monostable is associated with the auto free-run facility. When a trigger signal is present this monostable is continuously retriggered and its Q output remains high. In the absence of a trigger signal the monostable will reset and the Q output will go low, thus continuously triggering the timebase when S4 is in the auto position. The trigger circuit may be inhibited and the timebase switched into a continuous free-run position, thus grounding the trigger input of the timebase.

Timebase

The timebase (figure 4a) makes use of the well-known 555 timer. Those un-
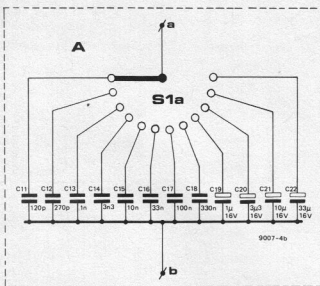
5
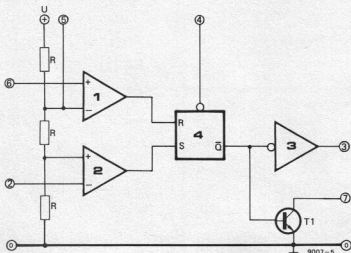
familiar with this IC should read the following description in conjunction with the internal diagram of the 555, given in figure 5.

Before a trigger pulse arrives to trigger the timebase the trigger input (emitter of T4) is held high by R30, so T4 is turned off and the collector voltage is at +15 V. The trigger pulse grounds the emitter of T4, turning it on so that the collector voltage, and hence the voltage at the top end of R29, falls. This takes the voltage on the inverting input of comparator 2 of the 555 below the voltage on the non-inverting input, so the output goes high, setting flip-flop 4 (figure 5). T1 (figure 5) is turned off, removing the short across the timing capacitor (block A in figure 4a), which is now charged linearly by the constant current source T2. When the voltage on the timing capacitor exceeds 2/3 supply voltage the output of comparator 1 (figure 5) goes high, resetting the flip-flop, which turns on T1 and shorts out the timing capacitor.

Figure 4b. Timebase range switch and timing capacitors.

Figure 5. Internal circuit of the 555 timer.

Figure 6. Circuit of the X and Y output amplifiers.

Figure 7. Printed circuit board and component layout for the X and Y output amplifiers.

6

+ 150 V

15V

Y

X̄

T1,T2,T6,T7 = BF 458
T3,T4,T5,T8,T9,T10 = BC140 ,BC141
D1 . . . D4 = 1N4148

* Tantalum

-15V

9007-6
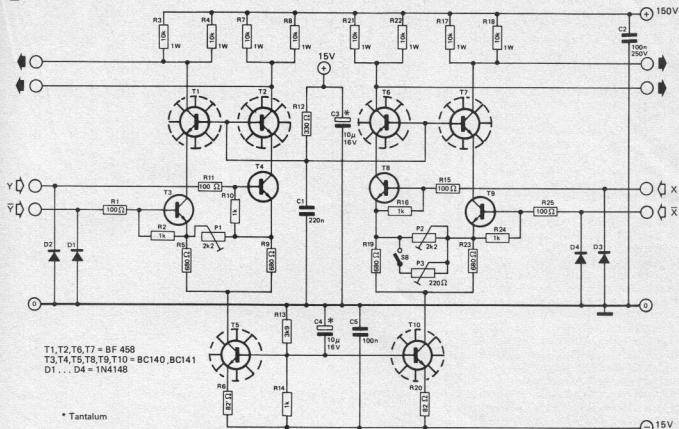
7
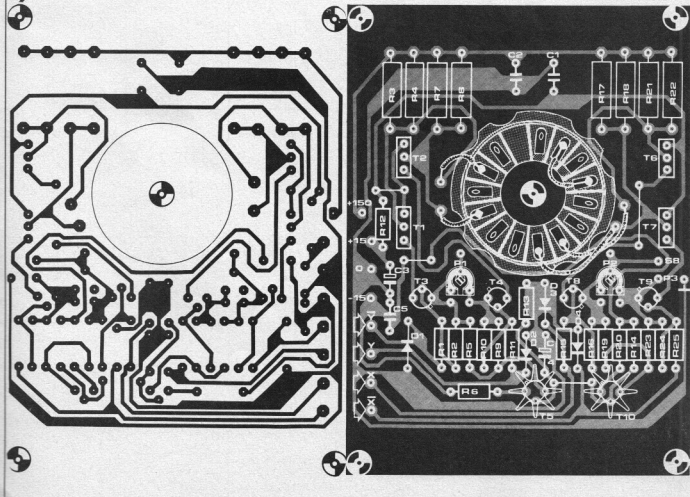
To avoid current being robbed from the capacitor, which would spoil the ramp linearity, the ramp output is buffered by a high impedance amplifier comprising T5 and T6. The sweep output is taken from the collector of T6. During the sweep the trigger input is inhibited by T3. This transistor is turned on when the ramp voltage exceeds its V_{be} and it shorts the base of T4 to ground for the duration of the sweep. This also facilitates the free-run facility. When the trigger circuit is in the free-run mode, or in the auto mode with no input signal, the emitter of T4 is permanently grounded. At the start of each sweep T4 will be turned on and will trigger the 555. It will then be turned off by T3 until the 555 resets, when T3 will turn off and T4 will turn on again, thus retriggering the timebase.

The flyback blanking pulse, which is obtained from pin 3 of the 555, is routed through the beam switching circuit where it is gated with the chop mode blanking pulses. Fine speed calibration of the timebase is provided by P2, which varies the current through T2, and X-position control is provided by P3, which applies a variable DC bias to one input of the X amplifier.

Timebase range selection is performed by S1a (figure 4b), which switches in various values of timing capacitor. This figure corresponds to block A in figure 4a. A second bank of this switch, S1b, is used to switch automatically from the 'chop' to 'alternate' channel switching mode. From 100 ms/cm to 1 ms/cm the 'chop' mode is used, and from 300 μs/cm upwards the 'alternate' mode is used.

X and Y output amplifiers

It will be convenient at this point to describe the X and Y output amplifiers, since an understanding of their operation is necessary to understand the design philosophy behind the channel-switching circuits.

Each amplifier (figure 6) consists of a differential cascode amplifier, and the X and Y amplifiers are identical except for the x5 trace expand switch (S8) of the X amplifier.

As an example, the Y-amplifier proper consists of a differential cascode amplifier (T3/T4) with a current source (T5) in the common emitter connection. This configuration, known as a 'long-tailed pair', can handle relatively large input voltage swings. The 'cascode' transistors T1 and T2 serve as output buffers. They are used in a grounded base configuration, at a base voltage of 15 V. This arrangement has two advantages: the differential amplifier proper operates at a reasonably low collector voltage, so high-gain transistors can be used, and there is very little internal feedback from output to input, so there are practically no stability problems.

The gains of the amplifiers may be adjusted by P1 and P2 and by P3 in the x5 position. Both amplifiers operate from the +150 V H.T. rail, and their outputs are connected direct to the X

Figure 8. Showing the principle of the electronic switch.
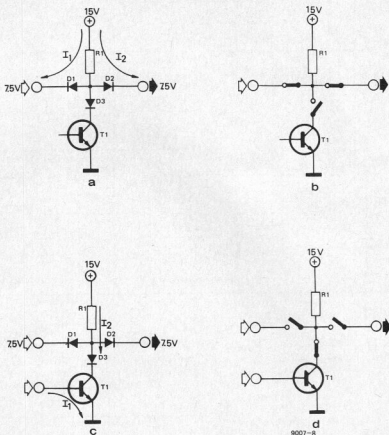
and Y plates.

To avoid problems due to loading of the outputs by long leads the X and Y amplifier p.c. board is mounted directly behind the CRT base. The layout of this board is given in figure 7.

Electronic switches

The signal switching arrangements in the Elektorscope are fairly complicated. Firstly, the (differential) outputs of the Y preamplifiers must be routed to the inputs of the Y output amplifier, either one at a time when only Y1 or Y2 is selected, or alternately at high speed in the Y1/Y2 chopped or alternate modes. Secondly, switching must be included to transpose the outputs of the Y2 preamplifier to invert the trace. Finally to switch between the normal and X-Y modes it must be possible to route either the timebase outputs, or the output of the X1 preamplifier, to the inputs of the X amplifier.

To avoid problems that may be caused by long lengths of lead, such as capacitive loading, instability, hum pickup etc. the switches cannot be mounted on the front panel but must be located so that the signal path between the Y preamps and the output amplifiers is as short as possible. This means mounting the switches at the back of the Y preamp boards.

Commercial oscilloscopes overcome the problem of controlling such switches by ingenious mechanical linkages such as extension spindles, rods, Bowden cables
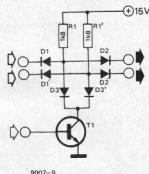
Figure 8. Showing the principle of the electronic switch.

Figure 9. The electronic switch may be extended to two or more channels, still controlled by a single transistor.

Figure 10. Circuit of one Y preamplifier.

Photo 1. The completed output amplifier board.

Table 1. Test point voltages for the Y preamp.

1

Table 1.

Y preamp test point voltages

| Test Point	Voltage	Conditions
A	+2.6 V	Input grounded.
B	+2 V	P1 in mid-
C	+9.5 V	position.
D	+10 V	
A	+2.6 V	Input grounded.
B	+2 V	P1 at end of
C	+9 ... +10 V	travel
D	+9.5 ... +10.5 V	

All voltages measured with a 20 kΩ/V meter. A tolerance of ± 10% on these readings is allowable. Measurements at points A' - D' will be identical.
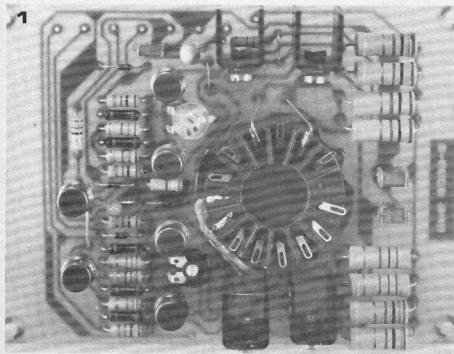
and the like, but such solutions are not suitable for the amateur, who generally likes the mechanical arrangements to be simple. In addition the Y1/Y2 channel switches must be completely electronic as they have to operate at the chopping frequency of 50 kHz. For these reasons it was decided to make all channel switching in the Elektorscope completely electronic. This has the ad-

ditional advantage that all these complicated functions can be controlled by single pole switches.

The principle of the electronic switch is shown in figure 8. When T1 is turned off D1 will always be forward biased provided the input voltage does not exceed the H.T. voltage (+15 V). The voltage at the junction of D1 and D2 will thus follow the input signal, but

will always be about 0.6 V higher due to the forward voltage drop across D1. The output will follow the signal at the junction of D1 and D2, but will always be 0.6 V lower due to the forward voltage of D2, i.e. it will be equal to the input voltage.

Provided D1 and D2 have approximately the same characteristics, any distortion introduced due to variations

10

D1 ... D14 = 1N4148
T1,T3,T8,T9 = BC547B
T2,T4,T5,T6,T7 = BC557B
T10 = E420

9007–10
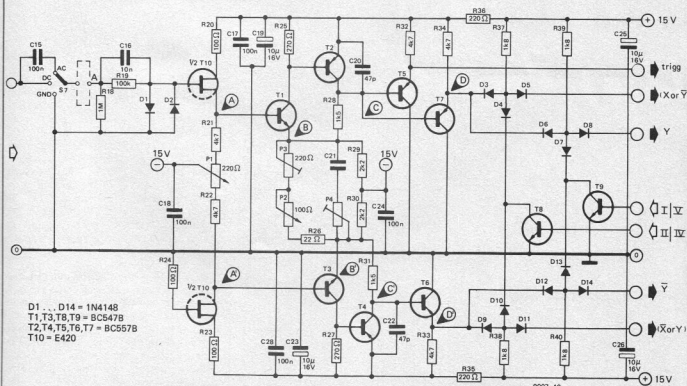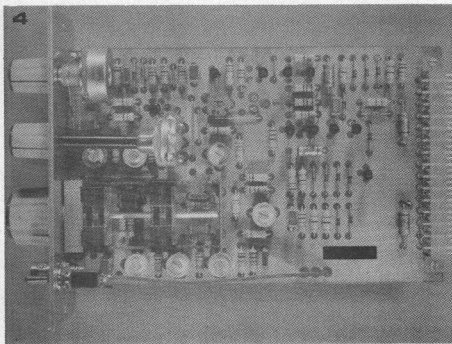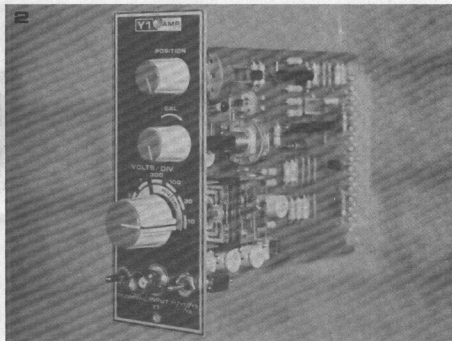
in the forward voltage of D1 with variations in the current through it will be cancelled by similar variations in the voltage drop of D2, provided the input and output impedances are similar.

When T1 is turned on by feeding current into its base the voltage at the junction of D1, D2 and D3 is held to just above the forward voltage drop of D3 (slightly greater due to the saturation voltage of T1) provided the input voltage remains above 0 V. Again about 0.6 V is dropped across D2, so the output voltage is approximately 0 V. When the output of the switch is connected in parallel with other switches then D2 will be cut off by any signals present on their outputs, provided the voltage is greater than 0 V. When the electronic switch is in the 'off' position therefore, it will not load the output of any other switch that is on.

If a switch is to control more than one signal channel then it is necessary to duplicate only the resistor/diode network, not the transistor, as shown in figure 9. D3 and D3' isolate the two channels from each other.

Y preamplifiers

The circuit of one Y preamplifier is given in figure 10. It will be seen that, with the exception of the trigger output taken from emitter follower T5, the circuit is completely symmetrical. This improves temperature stability and also provides the differential outputs necessary to drive the output amplifiers.

The input stage consists of a dual-FET T10 connected in a differential source-follower configuration. Use of a dual-FET means that the two devices are matched and are also in close thermal contact so that their characteristics will track together with temperature changes, thus minimising drift of the DC conditions within the amplifier. It is possible to use two E300 FET's mounted in a common cooling clip, but it may be necessary to experiment with the value of R21 to achieve a balanced condition at the outputs of the preamp.

The next two stages of the preamp are also differential, comprising transistor pairs T1/T3 and T2/T4. With the front panel gain control P2 in the 'cal' position the gain of the preamp may be varied between about 10 and 50 by P3. Provision has been made on the p.c. board layout for a compensation circuit P4/C21 to extend the h.f. response of the preamplifier. However, this is included only for the benefit of the serious experimenter and these components are not included in the parts list. P1 is the Y-position control.

To enable the preamplifier to drive the output amplifier and the inherent capacitances in the electronic switches without undue loss of bandwidth, emitter followers T6 and T7 are provided.

The electronic switches consist of T8, T9 and their associated diode networks D3 to D14. In the case of the Y1

2
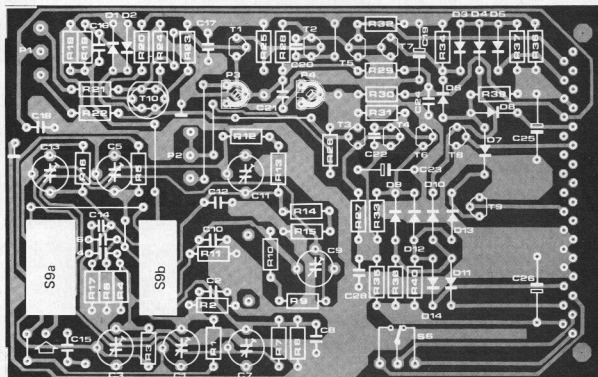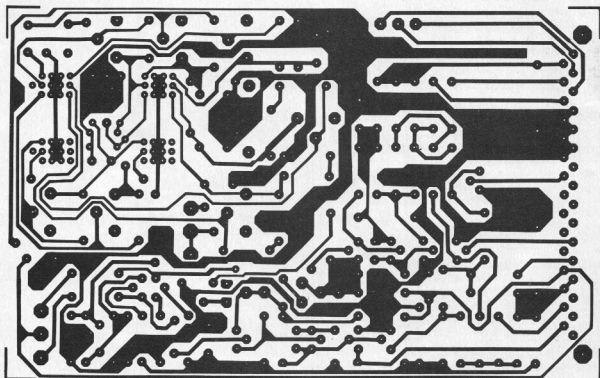
Figure 12. Printed circuit board and component layout for one Y preamp and attenuator.

Photo 2, 3 and 4. Three views of the completed Y preamp, showing the wiring to the two toggle switches.

preamp T9 controls the switching of the Y and $\overline{Y}$ outputs to the inputs of the Y output amplifier, while T8 controls the switching of the outputs to the inputs of the X amplifier for the X-Y mode. In the case of the Y2 preamp T9 again controls switching to the Y output amplifier, but T8 switches the outputs of the Y preamp to the Y amplifier inputs in a transposed manner for the trace invert mode (i.e. Y output to $\overline{Y}$ input and $\overline{Y}$ output to Y input)

Y attenuator

When connected to the Y amplifier and correctly calibrated the Y preamplifier has a basic sensitivity of 10 mV/cm. To display larger input signals without exceeding the screen limits some form of attenuator must be incorporated. This is connected behind S7 in figure 10 and its circuit is given in figure 11. The input resistance of the Y preamp is 1 M, and the input attenuator consists basically of resistive potential dividers designed to maintain a constant input resistance of 1 M while giving input sensitivities of 30 mV, 100 mV and so on.

However, the 1 M input resistance is also shunted by a capacitance of a few pF due to the gate capacitance of the FET, and if this were left uncompensated it would form a low-pass filter with the series arm of the attenuator, leading to an early roll-off in the frequency response. To avoid this the attenuator resistors are paralleled by capacitors. When the trimmer capacitors are correctly adjusted the reactances of the capacitors (taking into account the preamp input capacitance) will be in the same ratios as the attenuator resistors, so the attenuation factor will remain constant whatever the frequency. However the input impedance will reduce with increasing frequency due to the falling reactance of the capacitors.

It will be noted that the lower resistors in the attenuator sections are shunted with in some cases fairly large values of capacitance, and at first sight this may seem strange: it is the undesirable effects of the FET shunt capacitance for which we are trying to compensate, so why make it deliberately worse? The reasons for this are twofold. Firstly, this arrangement gives a fairly constant input capacitance of around 30 pF. This is necessary if the oscilloscope is to be used with high impedance probes, since these are designed to work into an input resistance of 1 M in parallel with between 20 and 40 pF. Secondly, the use of shunt capacitors avoids the necessity for impossibly small trimmer capacitors. For example if R2 were shunted simply by the 5 pF or so of the FET then R1 would have to be shunted by a trimmer whose reactance was $\frac{1000000}{330}$ times as much, or to put it

another way, whose capacitance was .0003 times the FET capacitance — about .0015 pF, which is ridiculous. The Y attenuators are mounted on the same p.c. board as the preamplifiers, the
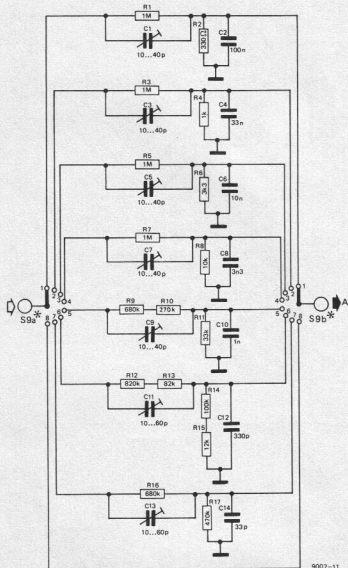
11

Figure 11. The compensated Y input attenuator.

layout of which is given in figure 12. For screening and stability an earth plane is provided on the upper side of this p.c. board, and care should be taken not to let the bodies of components short to this ground plane. This applies particularly to unsleeved electrolytic capacitors, to capacitors with metal end caps (e.g. Siemens MKM types) and to resistors, which may have only a thin paint film covering the end caps. The best plan is to place a thin strip of card beneath each component while soldering to stand it off from the board, or alternatively to give the top of the board a good coating of lacquer or insulating varnish.

NOTE All component lists will be given in the final part of this article.

QUADI-COMPLIMENTARY COMPLEMENTED

Several readers have sent us comments and queries concerning the article Quadi-Complimentary (Elektor, December 1975). Some further explanation appears to be in order.

The original article dealt with the principles involved in Quad's 'Current Dumping Amplifier' type 405. The majority of the readers request us to investigate the possibility of using this principle in a new amplifier design.

Before going into details, it should be plainly stated that this will be practically impossible if the final design is to be a reliable 'home construction' project in the Equa, Edwin, Equin tradition. This is why we are still looking for alternatives; see 'Ejektor' in last month's issue.

The 'current dumping' principle is unsuitable for a home construction project; it should only be considered in mass-produced commercial amplifier designs.

Why? This can be made clear as follows. In the case of 'current dumping' it is of prime importance that four impedances Z_1, Z_2, Z_3 and Z_4 should be very accurately defined. And that is the main difficulty! Figure 1 shows the overall block diagram; the conditions for $Z_1 \ldots Z_4$ are given in figure 2.

The impedances Z_1 and Z_3 of figure 1 are shown as resistors R1 and R3 in figure 2. For various reasons, Z_4 becomes a self inductance L4. Unfortunately, in practice this will be a coil rather than a pure self inductance, so there will be a resistance R4 in series with the coil.

This, in turn, means that Z_2 must consist of a capacitor C2 and a resistor R2 connected in parallel, in order to achieve the required bridge balance.

The bridge is in balance if:

$$Z_1 \cdot Z_3 = Z_2 \cdot Z_4 \; *)$$

The transformation from figure 1 to figure 2 is defined by:

$$Z_1 = R_1$$

$$Z_3 = R_3$$

$$Z_2 = \frac{R_2}{1 + j\omega R_2 C_2}$$

$$Z_4 = R_4 + j\omega L_4$$

In this case there are *two* conditions for bridge balance:

$$R_1 R_3 = R_2 R_4, \, and$$

$$L_4 = R_1 R_3 C_2 = R_2 R_4 C_2, \, or$$

$$R_2 = \frac{L_4}{R_4 C_2}$$

In the theoretical case where R_4 is zero, R_2 becomes infinitely large and can be omitted.

In actual practice, however, two alignments are needed, both equally difficult. In an experimental circuit it proved necessary to use a preset potentiometer for R_2 and a trimmer for C_2. The slightest deviation from bridge balance resulted in ugly cross-over phenomena.

A simple quiescent current adjustment as used in the Equin, for example, is a lot easier and gives better *guaranteed* results . . . . .

For a mass-produced version, the situation is somewhat different. There the specifications of the passive components $Z_1 \ldots Z_4$ are a dead fix, so it is possible to eliminate the alignment procedure and still get (very) good results.

Literature:
Quadi Complimentary, Elektor 12, December 1975, p. 1220.

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* Several readers have remarked that the assumption of an infinitely large open-loop gain also implies an infinitely large feedback factor. At first sight it would appear that this is what eliminates the non-linearity of the output stage. However, this assumption is incorrect. The balance condition for a finite gain A_o is:

$$Z_2 Z_4 = Z_1 Z_3 + \frac{(Z_1 + Z_2) Z_3}{A_o}$$

This is where 'current dumping' differs fundamentally from the Edwin principle: in the latter case the highest possible A_o, c.q. feedback factor, is indeed required.
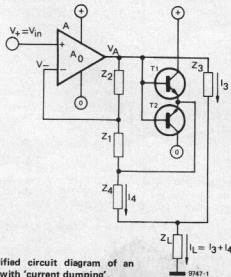
Figure 1. Simplified circuit diagram of an output amplifier with 'current dumping'.
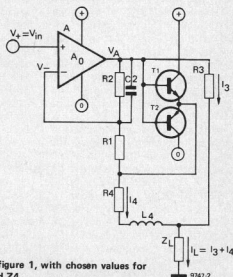
Figure 2. As figure 1, with chosen values for Z1, Z2, Z3 and Z4.

BI-FET OPAMPS

Interesting results can often be obtained by using several different types of active device in one circuit. Examples of this type of 'hybrid' circuit are designs incorporating both transistors and valves (or 'tubes' Am. or 'bottles' Sl.) or TTL and CMOS, or bipolar transistors and FETs. A relatively new example of this is the BI-FET opamp. It consists of JFETs and bipolar transistors on the same chip, and this could well give interesting results at a reasonable price.

The manufacturer describes the new opamps as 'monolithic JFET-input operational amplifiers incorporating standard bipolar transistors on the same chip, manufactured using ion-implantation techniques'. Furthermore, 'these amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, offset adjust which does not degrade drift or common-mode rejection, high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner'. Since they are also supposed to be rugged and relatively cheap, it would appear that some further investigation is called for . . .

The simplified circuit diagram of the new opamps (National Semiconductor types LF355, LF356 and LF357) is shown in figure 1. The ion-implantation manufacturing technology makes for well-matched FETs in the input stage, so that the input offset voltage can be very small. The input impedance is $10^{12} \Omega$ and the input bias current is only 30 pA. As the technical specifications show (table 1) the input noise figures are also exceptionally low.

The second stage is a 'long-tailed pair' of bipolar transistors. This stage provides most of the open-loop gain (106 dB, or 200,000 x !).

The output stage is a rather unusual hybrid quasi-complementary circuit. The basic circuit is shown separately in figure 2. It is short-circuit protected and it can withstand capacitive loads up to 10 nF without danger of instability.

These BI-FET opamps are eminently suitable for use in precision high-speed integrators; fast D/A and A/D converters; high impedance buffers; wide-band, low-noise, low-drift amplifiers; logarithmic amplifiers; sample and hold circuits; etc. They can also be used, of course, in conventional opamp circuits. One of the few conventional things about these opamps is the pinning: they are pin-compatible with the well-known 741, as shown in figure 3. The only thing to watch is that the offset control is connected to the positive supply - not the negative supply as with the 741.

Applications

A basic wide-band amplifier circuit using the LF357 is shown in figure 4. If required, an offset control can be included as shown in figure 3. The gain is x 10, the p-p output voltage swing is 20 V, the power bandwidth is 500 kHz and the distortion is less than 1%.
A more sophisticated circuit, using the LF356, is shown in figure 5. The

parasitic input capacitance C1 consists of the input capacitance of the opamp (3pF or less) and any additional capacitance introduced by the printed circuit board of other wiring. It can be compensated for by including C2, where

$$C2 \geq \frac{R1 \cdot C1}{R2}.$$

In this case the power bandwidth is approximately 240 kHz at the same distortion level (1%).
A more interesting application is shown in figure 6. This is a sharp notch filter; provided the components in the twin-T network are sufficiently well matched a quality factor Q of more than 100 can be obtained. As an example, if

$$R = 2R1 = 10M \text{ and } C = \frac{C1}{2} = 300 \text{ p}$$

the centre frequency of the notch will be approximately 100 Hz and the 'depth' will be −55 dB.

Final notes

The National Semiconductor opamps described here are the first of a new generation. NS have already announced a FET-input opamp, the LF13741. This has an input bias current of 200 pA, but in all other aspects (bandwidth, gain and rise-time) it has the same specifications as the 741.
Quite recently they introduced the LF352 series; these are instrumentation amplifiers with high gain linearity for low-level input signals and a high common-mode rejection ratio. They have also announced that the LF355, 356 and 357 are now to be made available in a much cheaper 8-pin mini-DIP version.
Furthermore, the opamps described here are already being supplied by Fairchild and Texas Instruments as second sources. This is often considered the 'acid test' of a new technology: how long does it take for other manufacturers to jump on the bandwagon . . . . .

(National Semiconductor application note).

Figure 1. Simplified circuit diagram of the BI-FET opamps.

Figure 2. Basic circuit of the output stage.

Figure 3. Pinning of the LF355, LF356 and LF357. They are pin-compatible with the 'traditional' 741, but the offset compensation is connected to the positive supply.

Figure 4. A basic wide-band amplifier circuit.

Figure 5. A more sophisticated circuit, including compensation for parasitic capacitances.

Figure 6. Circuit for a high-Q notch filter.

1

FET input | Bipolar diff. amp | Output stage

9472-1

2

9472-2
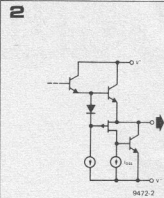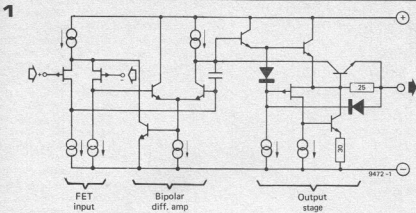
Table 1.

Absolute maximum ratings

Supply voltage	± 18 V
Power dissipation	500 mW
Operating temperature range	0°C . . . 70°C
T_j (max)	100°C
Differential input voltage	± 30 V
Input voltage range	± 16 V
Output short-circuit duration	continuous

DC electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	LF355/6/7			UNITS
			MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_s = 50\Omega$, $T_A = 25°C$		3	10	mV
	Over Temperature	$R_s = 50\Omega$			13	mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_s = 50\Omega$		5		$\mu V/°C$
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_s = 50\Omega$		0.5		$\mu V/°C$ per mV
I_{os}	Input Offset Current	$T_j = 25°C$		3	50	pA
		$T_j \leq T_{HIGH}$			2	nA
I_B	Input Bias Current	$T_j = 25°C$		30	200	pA
		$T_j \leq T_{HIGH}$			8	nA
R_{in}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{vol}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$	25	200		V/mV
		Over Temperature	15			V/mV
V_o	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		V
V_{cm}	Input Common-Mode Voltage Range		±10	+15.1 −12		V
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$	80	100		dB
PSRR	Supply Rejection Ratio		80	100		dB

PARAMETER		LF355		LF356		LF357		UNITS
		TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current		2	4	5	10	5	10	mA

AC electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	LF355	LF356	LF357	UNITS
			TYP	TYP	TYP	
SR	Slew Rate	LF355/6: $A_v = 1$. LF357: $A_v = 5$	5	12	50	V/µs
GBW	Gain-Bandwidth Product		2.5	5	20	MHz
t_s	Setting Time to 0.01%		4	1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	$R_S = 100 \Omega$ f = 100 Hz	25	15	15	$nV/\sqrt{Hz}$
		f = 1000 Hz	20	12	12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1.0 Hz	0.01	0.01	0.01	$pA/\sqrt{Hz}$
C_{in}	Input Capacitance		3	3	3	pF

3

TOP VIEW

9472-3

4

9472-4

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9472-5

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9472-6
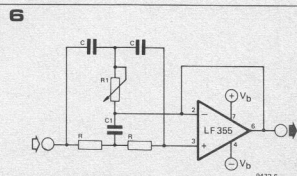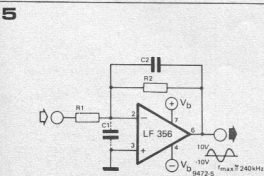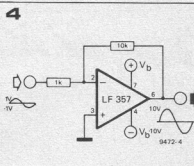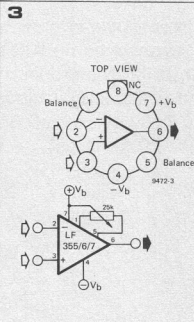
IC AUDIO

In this article two completely different types of high-power audio IC's are discussed. To avoid confusion the article is split into two parts. The first part deals with hybrid power-integrated circuits while the second section deals with the TDA 2020 IC.
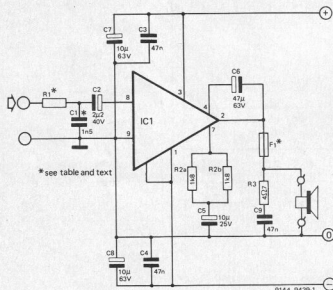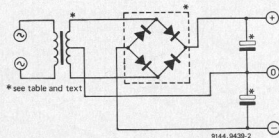
In a monolithic audio IC the entire circuit is integrated onto a single chip or die. As this chip is extremely small the problems involved in conducting away the heat dissipated in the circuit are enormous. Higher power audio IC's (greater than 20 W) generally use a hybrid form of construction whereby the output devices are on separate chips from the rest of the circuit, which may be integrated using monolithic or thick film techniques. The individual parts of the circuit are bonded to a large metal substrate and, after interconnections have been made, the whole assembly is encapsulated in resin or silicone rubber. The metal substrate provides good thermal contact with a heatsink, though the package is, of course, somewhat more bulky than a 14 pin DIL IC!

There are many hybrid audio IC's currently available, with power outputs up to more than 100 W, but of particular interest are a family of IC's manufactured by ITT, Skiltronics and Sanyo. These are of special interest

a) because they are available with output powers from 20 to 40 W in an identical package, so the same circuit layout can be used for all versions.

b) because they are obtainable from three different manufacturers, so they should be easier to obtain.

The maximum ratings and principal electrical characteristics of this family are given in table 1. Note that the Skiltronics type numbers are prefixed SPH, while the ITT and Sanyo type numbers are prefixed STK.

Figure 1 shows the external components required by the amplifier. The number of external components may seem rather large, but of course many of these are electrolytic capacitors, which are difficult to incorporate into a small package, and which might be damaged by the high temperatures that can occur within the IC. It will be noted that these circuits operate from a symmetrical supply (figure 2) with the loudspeaker direct coupled to the output.

Since the IC's are used as function building blocks or 'black boxes' the internal circuitry will not be discussed in detail. However, it should be stated that the output stage is of the quasi-complementary type, and the input stage is a differential amplifier of a fairly common configuration.

Precautions

Provided a few simple precautions are observed few problems should be encountered when using these IC's. These are as follows:

1. Both the positive and negative supply voltages must be applied to the IC simultaneously, since if only one voltage is applied a large d.c. offset will appear at the output, causing a large current to flow through the loudspeaker that could damage both loudspeaker and IC. Even a fuse in series with the loudspeaker will not protect the IC in these circumstances.

3

Parts list for figures 1 and 3.

Resistors:
R1 = see text
R2a/R2b = 1k8
R3 = 4Ω7

Capacitors:
C1 = see text
C2 = 2µ2/40 V
C3, C4, C9 = 47 n
C5 = 10µ/25 V
C6 = 47µ/63 V
C7, C8 = 10µ/63 V

Semiconductors:
IC1 = types 022, 025, 032 or 036

Miscellaneous:
F1 = see table 1
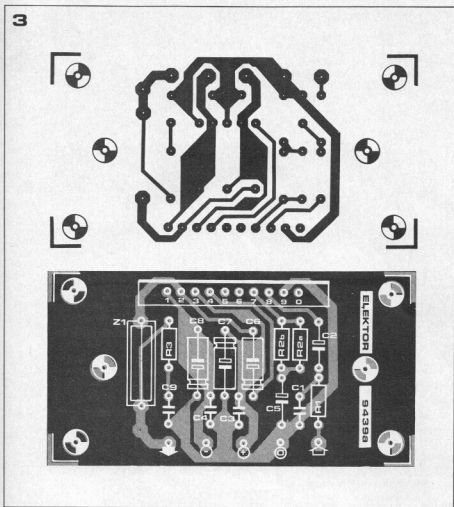
Figure 1. Application circuit for the 022, 025 032 and 036 IC's.

Figure 2. The Hybrid IC amplifiers require only a simple power supply.

Figure 3. Printed circuit board and component layout for the 022, 025, 032 and 036 IC's (EPS 9439a).

To minimise the d.c. current that flows through the loudspeaker (and hence the 'thump') when switching the amplifier on and off it is essential that the rise-times of both supply rails should be similar. Since the supply need only be a transformer, bridge rectifier and two reservoir capacitors this simply means that the reservoir capacitors should be of the same value. This will also ensure that the two supply voltages are as nearly the same as possible, which will minimise the d.c. offset voltage of the amplifier. This will normally be no more than ± 50 mV.

2. The second precaution is to ensure that the heatsink is of an adequate size, since these IC's do not incorporate thermal protection. The thermal resistance of suitable heatsinks is given in table 1. These are adequate even if the amplifier is driven for long periods at full output. For normal domestic use smaller heatsinks may be adequate.

When mounting the IC on a heatsink it is essential that the spacing of the fixing holes should be as accurate as possible, otherwise the heatsink or baseplate of the IC may become distorted, leading to poor thermal contact. Some silicone heatsink grease could be used to improve thermal contact.

3. It might be thought that fusing the positive and negative supply rails would be a suitable method of protection, but this is not the case since failure of a fuse in one rail would cause the fault condition discussed earlier, i.e. a large d.c.

offset on the output. The only fuse should be in the primary of the mains transformer, and this is intended to protect the power supply rather than the amplifier.

Construction

A printed circuit board and component layout suitable for use with IC's type 025, 032 and 036 is given in figure 3. The input resistor R1 forms an attenuator with the input impedance of the IC and should be chosen to provide the required input sensitivity/input impedance, taking into account the gain of the IC.

For example, suppose the STK032 is required to provide 25 W into an 8 Ω load with an input sensitivity of 1 V.

25 W into 8 Ω means an rms output voltage of approximately 14 V. The gain of the IC is about 30 dB or 31 times, so the voltage required at the input is 14/31 or 0.45 V. Since the required input sensitivity is 1 V this means that 0.55 V must be dropped across R1 so R1 is $\frac{0.55}{0.45}$ x Z_{in} or about 33 k. The input impedance of the amplifier (with R1) is thus 60 k.

R1 and C1 together form a lowpass filter to protect the IC against high slew-rates (which gives rise to transient intermodulation distortion) by limiting the risetime of the input signal.

If R1 is changed then C1 should also be changed to maintain the same break-

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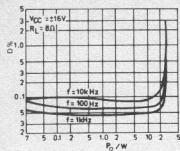
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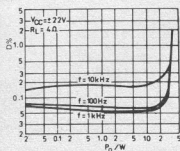
9144,9439-4b
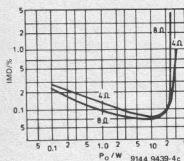
9144,9439-4c

Figure 4. Distortion v power graphs for the 025.

Figure 5. Circuit for a 20 W amplifier using a single supply rail.

Table 1. Pertinent data for the 022, 025, 032 and 036 IC's.

Table 2. Absolute maximum ratings of the TDA2020.

Table 3. Electrical characteristics of the TDA2020.
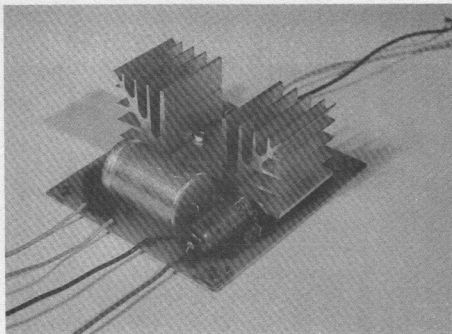
Table 1. Maximum ratings, electrical characteristics and applications data of hybrid audio IC's for use with symmetrical power supply

Skiltronics, ITT, Sanyo	SPH 022 — STK 022	SPH 025 STK 025 STK 025G	SPH 032 — STK 032	SPH 036 STK 036 STK 036
Maximum supply voltages	±25 V	±29 V	±32 V	±35 V
Nominal supply voltages	±19 V	±22 V	±24 V	±27 V
quiescent current	30-50 mA			
Minimum output power into 4 ohm	23 W	30 W	35 W	40 W
Minimum output power into 8 ohm	15 W	20 W	25 W	30 W
Maximum case temperature	85°C			
Maximum output short-circuit duration	two seconds under full drive			
recommended mains transformer	2 x 15 V 75 VA	2 x 17 V 90 VA	2 x 18 V 100 VA	2 x 20 V 120 VA
speaker fuse, if required	5 . . . 6 A, fast blow			
voltage gain (dB)	33 dB	30.5 dB	30.5 dB	30 dB
input impedance	27 k			
recommended thermal resistance of heatsink	2° C/W	1.7° C/W	1.5° C/W	1.4° C/W
bridge rectifier	40 V 2 A	40V/3.2A		80 V 5 A
Reservoir capacitor	≥2200 µ	≥3300 µ	≥3300 µ	≥3300 µ

Table 2

Absolute maximum ratings TDA2020.

V_s	Supply voltage	±22 V
V_i	Input voltage	V_s
V_i	Differential input voltage	±15 V
I_o	Output peak current (internally limited)	3.5 A
P_{tot}	Power dissipation at T_{case} <75°C	25 W
T_{stg}, T_j	Storage and junction temperature	−40 to 150°C

Table 3

Electrical characteristics TDA2020 ($V_s = \pm17V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		±5		±22	V
I_d	Quiescent drain current	$V_s = \pm22V$		60		mA
I_b	Bias current			0.15		μA
$V_{i(off)}$	Input offset voltage	$V_s = \pm17V$		5		mV
$I_{i(off)}$	Input offset current			0.05		μA
$V_{o(off)}$	Output offset voltage			10	100	mV
P_o	Output power	$d = 1\%$ $G_v = 30$ dB $T_{case} \leqslant 70°C$ $f = 40$ to 15,000 Hz				
		$V_s = \pm17V$ $R_L = 4\ \Omega$	15	18.5		W
		$V_s = \pm18V$ $R_L = 4\ \Omega$		20		W
		$V_s = \pm18V$ $R_L = 8\ \Omega$		16.5		W
		$d = 10\%$ $G_v = 30$ dB $T_{case} \leqslant 70°C$ $f = 1$ kHz				
		$V_s = \pm17V$ $R_L = 4\ \Omega$		24		W
		$V_s = \pm18V$ $R_L = 4\ \Omega$		20		W
V_i	Input sensitivity	$G_v = 30$ dB $f = 1$ kHz				
		$P_o = 15W$				
		$V_s = \pm17V$ $R_L = 4\ \Omega$		260		mV
		$V_s = \pm18V$ $R_L = 8\ \Omega$		380		mV
B	Frequency response (−3 dB)	$R_L = 4\ \Omega$ $C4 = 68$ pF		10 to 160,000		Hz
d	Distortion	$P_o = 150$ mW to 15W $R_L = 4\ \Omega$ $G_v = 30$ dB $T_{case} \leqslant 70°C$				
		$f = 1$ kHz		0.2		%
		$f = 40$ to 15,000 Hz		0.3	1	%
		$P_o = 150$ mW to 15W $V_s = \pm18V$ $R_L = 8\ \Omega$ $G_v = 30$ dB $T_{case} \leqslant 70°C$				
		$f = 1$ kHz		0.1		%
		$f = 40$ to 15,000 Hz		0.25		%

point for the filter. As a rule-of-thumb, if R1 is 1 k then C1 should be 3n3, and if R1 is increased then C1 should be decreased by the same factor. For instance, if R1 is increased to 10 k (multiplied by 10) then C1 should be divided by 10 (reduced to 330 p). When making these calculations the output impedance of the source feeding the amplifier (e.g. a preamp) must be taken into account. For example, if the preamp has an output impedance of 5 k and R1 is 1 k then the effective value of R1 is 6 k, so the nominal value for C1 should be divided by 6.

In practice, of course, the value of C1 is not so critical. The value shown in figure 1 (1n5) can be used for any value of R1 between 1 k and 5k6, for instance. Furthermore, the minimum value is 330 p.
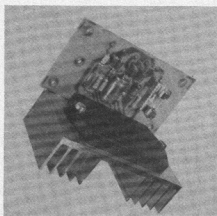
Distortion

Finally, figure 4 includes graphs of one important parameter shown in table 1 — distortion. Figures 4a and 4b show harmonic distortion versus power output at three frequencies, into 8 Ω and 4 Ω loads, for the 025 IC, while figure 4c shows intermodulation distortion versus output power into 8 and 4 Ω loads.
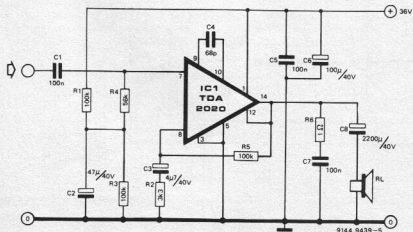
Twenty twenty

The next type of audio IC to be discussed is the SGS TDA2020. It is a monolithic audio IC that can achieve an output power of (typically) twenty watts continuous. Furthermore, crossover and harmonic distortion are low so that the IC is truly 'hi-fi'. The chip incorporates safe area limiting to keep the output transistor dissipation within acceptable limits, together with a

5

9144,9439–5

7

LS L

LS R

TDA2030

TDA2030

22k

22k

B40C 3300

4700μ
40V

R15

.33V

15V

24V∼

3A

R17 R16
1k5 330Ω

4x
10k lin

6

thermal shutdown system to protect the whole IC against overheating.

The absolute maximum ratings of the TDA2020, which should never be exceeded, are given in table 2. The electrical characteristics are given in table 3.

The TDA2020 may be used with either a symmetrical (±) power supply, in which case the loudspeaker can be direct-coupled to the output stage, or with a single power supply rail, in which case an output coupling capacitor is needed.

Although a direct-coupled output theoretically saves components, it has the disadvantage that the loudspeaker is unprotected against d.c. fault conditions in the amplifier, and the supposed saving is more than outweighed by the need to provide loudspeaker protection circuits. For this reason the practical circuit is based on an amplifier with a single power rail, as shown in figure 5.

In this circuit, 100% d.c. feedback is provided via R5, and the non-inverting input is biased to half the supply voltage by R1 and R3. This means that the quiescent output voltage of the amplifier is also half the supply voltage. The gain of this circuit is about 30 dB.

Maximum output power of 16 W into 8 Ω is thus achieved with an input voltage of 360 mV rms, or with a 4 Ω load 20 W may be obtained with a 285 mV input.

With an 8 Ω load, distortion at 1 kHz is less then 0.1% for output powers from 150 mW to 15 W. Distortion into a 4 Ω load is approximately twice this.

Figure 6 shows a printed circuit board and component layout for this particular application circuit. A special spacer (supplied with the TDA2020) is

Parts list for figures 5 and 6.

Resistors:
R1, R3, R5 = 100 k
R2 = 3k3
R4 = 56 k
R6 = 1 Ω

Capacitors:
C1, C5, C7 = 100 n
C2 = 47μ/40 V
C3 = 4μ7/40 V
C4 = 68 p
C6 = 100μ/40 V
C8 = 2200μ/40 V

Semiconductors:
IC1 = TDA2020

Figure 6. Printed circuit board and component layout for a 20 W amplifier using the TDA2020 (EPS 9144).

Figure 7. A suggested layout for an 'all IC' stereo amplifier using the TDA2020 and the TCA 730/740 control amplifier.

mounted beneath the device before soldering it into the board. This supports the heatsink, which is mounted on top of the IC and is secured by bolts passed through the spacer. Good thermal contact between the IC and the heatsink is ensured by a copper slug which is integral with the IC package. Some heatsink compound should be smeared on the IC and the back of the heatsink to improve this contact still further.

The exact shape of the heatsink is unimportant, provided it fits the board. However, if the IC is to be run at full power for long periods of time then the thermal resistance of the heatsink should not be less than 2°C per watt. In normal domestic use heatsinks of up to 8°C per watt may be acceptable.

It should be noted that the copper slug (and hence the heatsink) is internally connected to pin 5, so the heatsink is at ground potential. However, if a symmetrical supply is used, the negative supply potential is present on the heatsink!

Figure 7 shows a suggested layout for a simple 'all IC' stereo amplifier using two TDA2020's and the TCA730/740 control amplifier described in Elektor 8. If a disc input were required then the control amplifier could be preceded by the IC disc preamplifier featured in Elektor 3.

The power supply to the TDA2020's may be unstabilized and is derived simply from a transformer, bridge rectifier and reservoir capacitor. The 15 V stabilized supply to the control amplifier may be obtained either from a suitable IC voltage regulator, or from a simple zener stabilizer. If the IC disc preamp is also used this, of course, has a built-in voltage regulator.

THE BF 494 A CASE IN POINT

116

(TO-92)

116a	b	c
116b	c	b
116c	s	g	d
116d	g	s	d
116e	b	e	c
116f	N	c	og

9784 1

Editor's lament:
Oh why, tell me, why
Can our readership's eye
More clearly descry
Than an author, or I,
Any slip, imperfection,
Or faulty connection?

The BF 494 is an extremely useful HF transistor, and it is used in many Elektor circuits for this reason. The specifications are quite good and the price is quite reasonable, which means that it can be used as a kind of 'Univeral HF Transistor'. Applications range from

found that these two reliable sources had different ideas about the BF 494 . . A few 'phone calls to the two parties concerned taught us that, in this case, the Philips data are accurate. Pro-Electron, for once, appears to have slipped up. Figure 2 therefore gives the official pinning for the BF 494.
As a final note we would like to remark that we were highly impressed by the rapid and energetic action undertaken by the 'Association Internationale Pro-Electron' to locate and remedy the mistake. We will continue to rely on their data handbooks in the future, albeit perhaps not quite so blindly . . . ◼
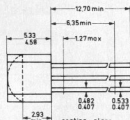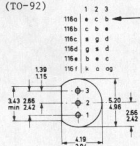
1

Low power HF transistors
Transistors HF - HF-Transistoren   **BF**

TYPE	RATINGS (at Tamb = 25°C, unless otherwise stated)						CHARACTERISTICS (at Tamb = 25°C, unless otherwise stated)															P O L A R I T Y	O U T L I N E S
	V_{CBO}	V_{CEO} or V_{CER}	V_{EBO}	I_C	P_{tot}	T_j	h_{FE}	h_{fe} at 1 kHz	V_{CE} V_{CB}	I_C I_E	f_T f_{ab}	C_{ob} C_{re}	V_{CB} V_{CE}	V_{CEsat} V_{BE}	I_C	I_B	V_{CE} V_{CB}	I_C I_E				
	V max	V max	V max	mA max	mW max	°C max	min – max	min	V	mA	MHz min	pF max	V	V max	mA	mA	V	mA	MHz			
BF494	30	20	5	30	300c150		260'	0,85'	'10	'0,74	1	'10	4'	10	1	100	N					116a

9784 1

oscillator and mixer stages in AM and FM receivers to HF and IF amplifier stages.
However, there is a problem. As several observant readers have pointed out, the pinning shown in the transistor list in E17, p.947, is at variance with the pinning used on the Elektor printed circuit boards. As we mentioned in the 'Missing Link' last month, the information in the transistor list was incorrect; this has been corrected in the more recent lists.
The reason for the slip is perhaps interesting. We took extreme care to keep the list in exact accordance with the 'Standard Handbook' issued by Pro-Electron. When the reader's enquiries started coming in, we compared the Pro-Electron data (figure 1) with the pinning shown in the Philips data handbook (figure 2). To our surprise we

2

SILICON PLANAR EPITAXIAL TRANSISTOR   **BF494**

Dimensions in mm

MECHANICAL DATA

TO-92 variant

4,2
1,6
4,8 max
2,54
0,65 max

5,2 max
12,7 min
0,35 max
0,48 max
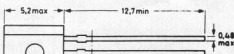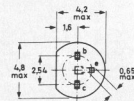
diameter within 2,5 max is uncontrolled

9784 2

Legend

PNP = P		
NPN = N		

V_CEO (Volt)	I_C(max) (mA)	P_max (mW)	h_FE(min)
00 = < 20	0 = < 50	not cooled:	0 = < 20
000 = 25-40	00 = 55-100	0 = < 300	00 = 25-50
0000 = 45-60	000 = 105-400	00 = 305-1000	000 = 55-120
00000 = 65-80	0000 = 405-2 A	cooled:	0000 = > 125
000000 = > 85	00000 = > 2 A	00* = 1-10 W	
		00** = 10-35 W	
		00*** = > 40 W	

Type	PNP=P NPN=N	V_CEO (Volt)	I_C(max) (mA)	P_max (mW)	h_FE(min)	case nr.	comments
TUN	N	0	00	0	000		
TUP	P	00	00	0	000		
AC126	P	0	00	00	0000	2	
AF239	P	0	0	0	000	1	grounded base: f f_T = 700 MHz
BC107	N	000	00	0	000	2	
BC108	N	0	00	0	000	2	
BC109	N	0	00	0	000	2	low noise
BC140	N	00	0000	00*	000	2	
BC141	N	000	0000	00*	000	2	
BC160	P	000	0000	00*	000	2	
BC161	P	000	0000	00*	0	2	
BC182	N	000	000	0	0000	2	
BC212	P	000	000	0	000	2	
BC546	N	000	00	0	000	2	
BC556	P	000	00	0	000	2	
BD106	N	00	00000	00**	00	7	
BD130	N	00	00000	00***	0	7	
BD132	P	000	0000	00**	0	9	
BD137	N	000	0000	00**	00	9	
BD138	P	000	0000	00**	00	9	
BD139	N	0000	0000	00**	00	9	
BD140	P	0000	0000	00**	00	9	
BDY20	N	00	00000	00***	0	7	
BF180	N	0	0	0	0	1	grounded base: f_T = 675 MHz
BF185	N	0	0	0	00	12	grounded emitter: f_T = 220 MHz
BF194	N	0	0	0	000	10	grounded emitter: f_T = 260 MHz
BF195	N	0	0	0	000	10	grounded emitter: f_T = 200 MHz
BF199	N	0	0	00	000	11	grounded emitter: f_T = 550 MHz
BF200	N	0	0	00	0	1	grounded base: f_T = 240 MHz
BF254	N	0	0	0	00	11	grounded emitter: f_T = 260 MHz
BF257	N	00000	00	00	000	11	grounded emitter: f_T = 90 MHz
BF494	N	0	0	0	00	11	grounded emitter: f_T = 260 MHz
BFX34	N	000	00000	00	00		f_T = 70 MHz
BFX89	N	0	0	0	0	1	grounded emitter: f_T = 1000 MHz
BFY90	N	0	0	0	0	1	grounded emitter: f_T = 1000 MHz
BSX19	N	0	0	0	00	2	
BSX20	N	0	0000	0	00	2	
BSX61	N	000	0000	0	000	2	
HEP53	N	00	0000	00	00		f_T = 150 MHz
HEP55	N	00	0000	00	00		f_T = 200 MHz
HEP56	N	00	0000	00	00	5	f_T = 750 MHz
MJE171	N	00	00000	00**	00	9	
MJE180	N	00	00000	00**	00	9	
MJE181	N	00	00000	00**	00	9	
MJE340	N	00000	0000	00**	00	9	
MPS A05	N	000	000	00	00	13	
MPS A06	N	0000	000	00	00	13	
MPS A09	N	0000	0	0	00	13	
MPS A10	N	00	00	00	00	13	
MPS A13	N	00	000	00	0000	13	
MPS A16	N	00	00	0	0000	13	
MPS A17	N	00	00	0	0000	13	
MPS A18	N	00	00	0	0000	13	
MPS A55	P	0000	000	00	00	13	
MPS A56	P	0000	000	00	00	13	
MPS U01	N	00	000	00*	00	14	
MPS U05	N	00	00	00*	00	14	
MPS U56	P	00	000	00*	00	14	
MPS2926	N	0	00	00	000	13	f_T = 300 MHz
MPS3394	N	0	00	00	000	13	f_T = 100 MHz
MPS3702	P	00	00	00	00	13	
MPS3706	N	00	00	00	00	13	
MPS6514	N	00	00	0	0000	13	f_T = 480 MHz
TIP29	N	000	0000	00**	00	3	
TIP30	P	000	0000	00**	00	3	
TIP31	N	000	0000	00**	00	3	
TIP32	P	000	0000	00**	00	3	
TIP140	N	000	00000	00***	0000	7	Darlington
TIP142	N	00000	00000	00***	0000	7	Darlington
TIP2955	P	000	00000	00***	00	3	
TIP3055	N	000	00000	00***	00	3	
TIP5S30	N	000	00000	00***	00	3	
2N696	N	000	00	00	00	2	
2N706	N	0	0	0	00	2	
2N914	N	0	0000	00	0	2	
2N1613	N	000	00	00	00	2	
2N1711	N	000	00	00	000	2	
2N1983	N	00	00	00	0	2	
2N1984	N	00	00	00	0	2	
2N2219	N	000	000	00	00	2	
2N2222	N	000	000	00	00	2	
2N2925	N	0	0	0	0000	13	
2N2955	P	000	00000	00***	00	3	≠ MJE2955, TIP2955!
2N3054	N	000	0000	00**	00	7	
2N3055	N	000	00000	00***	0	7	
2N3553	N	000	0000	00**	0	13	f_T = 500 MHz
2N3568	N	000	000	0	000	13	
2N3638	P	000	000	0	000	13	
2N3702	P	00	00	0	000	13	
2N3866	N	00	000	00*	0	13	f_T = 700 MHz
2N3904	N	000	00	0	00	13	
2N3905	P	000	00	0	00	13	
2N3906	P	000	00	0	000	13	
2N3907	N	000	0	0	00	13	
2N4123	N	000	00	0	00	13	
2N4124	N	00	00	0	000	13	
2N4126	P	00	00	0	000	13	
2N4401	N	000	000	0	00	13	
2N4410	N	000	00	0	000	13	
2N4427	N	00	000	00*	0	13	f_T = 700 MHz
2N5183	N	0000	0000	00	0	2	

Case outline figures ① – ⑭ (right-hand column).

OPAMPS, COMPARATORS

703

DECOUPLING — OUTPUT
INPUT HIGH — INPUT LOW
GROUND
NOTE: Pin 4 connected to case.

709

INPUT COMP A
COMP B
V+
INPUT COMP B
NC
-INPUT
+INPUT
V-
OUTPUT
OUTPUT COMP
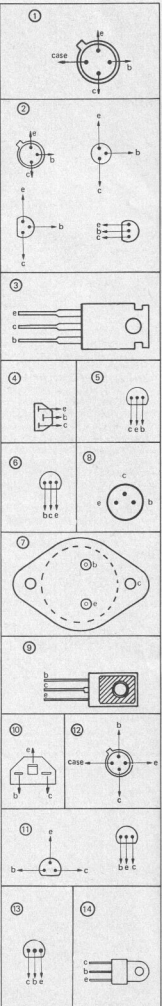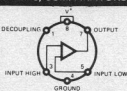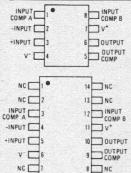
NOTE: Pin 7 connected to bottom of package.

INPUT COMP B
INPUT COMP A
-INPUT
+INPUT
V-
V+
OUTPUT
OUTPUT COMP

NOTE: Pin 4 connected to case.

BAL — NC
-IN — V+
+IN — OUTPUT
V- — BAL

NC — NC
-IN — V+
+IN — OUTPUT
V- — BAL

TAA 861 (A)

V+ — Compensation
V-
Compensation
+V — -V

1458 (5558)

1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V+

1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V+

SN 76131 ≡ TBA 231 ≡ µA 739

AMPLIFIER NO. 2
AMPLIFIER NO. 1

324

Output 1 — Output 4
-Input 1 — Input 4
+Input 1 — +Input 4
V+ — GND
+Input 2 — +Input 3
-Input 2 — Input 3
Output 2 — Output 3

CA 3080

TAB
INV INPUT
NON-INV INPUT
OUTPUT
AMPLIFIER BIAS INPUT

NOTE: Pin 4 is connected to case.

CA 3094

SINK OUTPUT (COLLECTOR)
TAB
EXTERNAL FREQUENCY COMPENSATION OR INHIBIT INPUT
DRIVE OUTPUT (EMITTER)
DIFFERENTIAL VOLTAGE INPUTS
GROUND 'V' IN DUAL-SUPPLY OPERATION
PROGRAMMABLE INPUT (STROBE OR AGC)

NOTE: Pin 4 is connected to case.

CA 3130

Phase Compensation
TAB Strobe
Offset null
Inv. Input
Output
Non Inv. Input
Offset null

NOTE: Pin 4 is connected to case.

339

Output 1 — Output 4
Output 2 — Output 3
V+ — GND
Input 1+ — Input 4+
Input 1- — Input 4-
Input 2+ — Input 3+
Input 2- — Input 3-

SPECIAL TYPES

CA 3086 ≡ CA 3046

BOTTOM VIEW

555

Ground — V_CC
Trigger — Discharge
Output — Threshold
Reset — Control Voltage

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_CC

566

Discharge — V_CC
Threshold — Discharge
Control Voltage — Threshold
Reset — Control Voltage
Trigger — Output
Ground — Trigger

NOTE: On metal can, pin 5 is connected to case.

1310

POWER SUPPLY — VCO OUTPUT
COMPOSITE INPUT — LOOP FILTER
AUDIO AMP — LOOP FILTER
LEFT DE-EMPHASISED — PHASE COMPARATOR
LEFT OUTPUT & DE-EMPHASISED — PILOT MONITOR
RIGHT OUTPUT & DE-EMPHASISED — THRESHOLD FILTER
RIGHT DE-EMPHASISED — DE-EMPHASIS
LAMP DRIVER — THRESHOLD FILTER

MC 1310
LM 1310 EP

COMPOSITE INPUT — POWER SUPPLY
AUDIO AMP & DE-EMPHASISED — VCO CONTROL
LEFT DE-EMPHASISED — LOOP FILTER
LEFT OUTPUT — LOOP FILTER
RIGHT OUTPUT — PHASE DETECTOR INPUTS
RIGHT DE-EMPHASISED — PILOT MONITOR
LAMP DRIVER — THRESHOLD FILTER
DE-EMPHASISED — THRESHOLD FILTER

MC 1311
MC 1310 E
LM 1310 N
µA 758

VOLTAGE REGULATORS

L 129/L 130/L 131

µA 78...

TBA 625 (829, 830)

BOTTOM VIEW

LM 309 H, µA 78 M.

BOTTOM VIEW

LM 309 K

NOTE: Pin 4 connected to case.

723 (550)

CURRENT LIMIT — NC
CURRENT SENSE — COMP
— V+
-INPUT — V+
+INPUT — VOUT
V_REF — VZ
V- — CURRENT LIMIT

CURRENT LIMIT
CURRENT SENSE — COMP
-INPUT — V+
+INPUT
V_REF — VOUT

NOTE: On metal can, pin 5 is connected to case.

SG 3501 (SG 4501)

NEG. INPUT V- — POS. INPUT V+
NC — NC
NEG. SENSE — POS. OUTPUT
NEG. STAB. — POS. SENSE
VOLT. ADJ. — BALANCE ADJ.
— GND

NEG. OUTPUT — POS. INPUT V+
NEG. SENSE — NC
NEG. STAB. — POS. SENSE
VOLT. ADJ. — POS. STAB.
GND

LM 325 (LM 125/LM 225)

+ BOOST — SENSE
CURRENT LIMIT — CURRENT LIMIT
NC — REFERENCE
V+ — GND
- SENSE — BOOST

LM325N
LM325AN

+ BOOST — + BOOST
CURRENT LIMIT — CURRENT LIMIT
NC — GND
- SENSE — REFERENCE
- VOUT — + VOUT

LM325S
LM325AS

GND

- CURRENT LIMIT — REFERENCE
+VOUT — BOOST
+ BOOST — GND
VIN — VOUT
- CURRENT LIMIT

LM125H
LM225H
LM325H

- VIN

NOTE: All IC's shown top view, unless otherwise stated.

4001

VDD H G M L F E

A B J K C D VSS

4011

VDD H G M L F E

A B J K C D VSS

4012

VDD H G L F E

A B J K C D VSS

4013

DUAL DATA FLIP/FLOP

Q2 Q2 CL2 D2

Q1 CL1 R1 D1

OUTPUT

4015

DATA
RESET

CLOCK

VSS

4017

DECADE COUNTER

RESET

VSS

4018

5 STAGE COUNTER

DATA
I/P

VSS

4023

VDD G H I J K L

A B C D E F VSS

4024

VDD NC NC J2 NC Q7 NC

7 STAGE COUNTER

CLOCK RESET Q6 Q5 Q4 Q3 VSS

4027

DUAL J/K FLIP/FLOP

4028

BCD INPUTS

DECIMAL OUTPUTS

4035

PARALLEL INPUTS

4040

OUTPUTS CLOCK

VDD

12-STAGE COUNTER

OUTPUTS

4070

VDD

VSS

4046

PLL

PHASE COMP

VCO

EXTERNAL CAPACITOR

4049

VCC G A H B I C VSS

4054

INPUT LATCHES

LEVEL SHIFT

DISPLAY DRIVERS

OUTPUTS

4050

NC
VCC G A H B I C VSS

4056

SEGMENT OUTPUTS

BCD TO 7 SEGMENT DECODER/DRIVER

LEVEL SHIFT

INPUT LATCH

BCD INPUTS

4068

VDD

N/C A B C D N/C VSS

4071

VDD

VSS

4073

VSS

4081

VDD

VSS

4082

VDD NC

VSS

4093

VDD H G M L F E

A B J K C D VSS

CD 4098 (MC14528)

EXTERNAL COMPONENTS TRIGGER INPUTS OUTPUTS

DUAL M.M.V.

EXTERNAL COMPONENTS TRIGGER INPUTS OUTPUTS

4518 (4520)

DUAL UP COUNTER

OUTPUTS

Note: A prefix to the type number denotes the manufacturer, e.g. CD 4001 (RCA), MC 14001 (Motorola), N 4001 (Signetics), SCL 4001 (Solid State Scientific), SIL 4001 (Siltek).

7400* (7403*)

7401*

7402* (7428)

7404* (7405*, 7406*) 7416*)

7407

7408

7410* (7412*)

7413 (7420*, 7440)

7414+

7430

7442* (7428)

7447

7473+

7474+

7475

7476*

7486

7490

7492

7493

74121

74122

74123

74132

74141

74143 (74144)

74154+

74164

74192+

74196
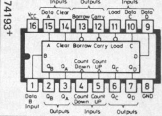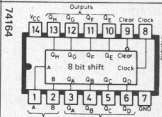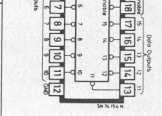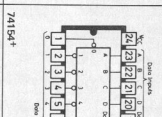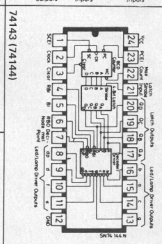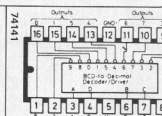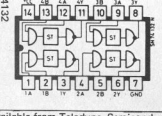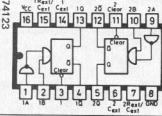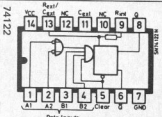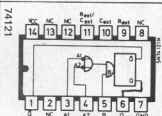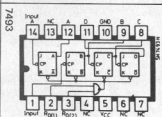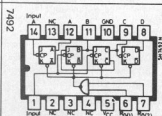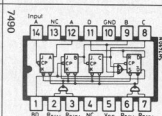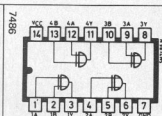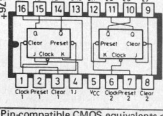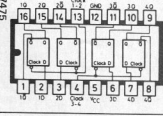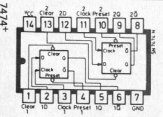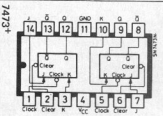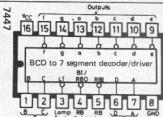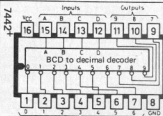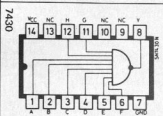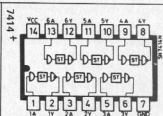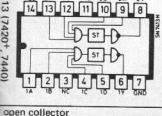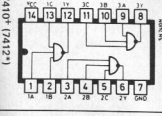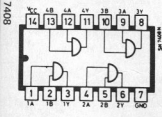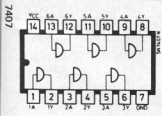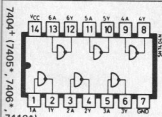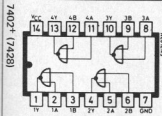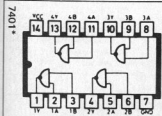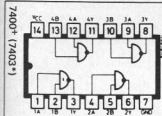
* open collector

+ Pin-compatible CMOS equivalents available from Teledyne Semiconductor and National Semiconductor

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP' (Transistor, Universal PNP), 'TUN' (Transistor, Universal NPN), 'DUG' (Diode, Universal Germanium) or 'DUS' (Diode, Universal Silicon). This indicates that a large group of similar devices can be used, provided they meet the minimum specifications listed in tables 1a and 1b.
For further information, see the article 'TUP-TUN-DUG-DUS' in Elektor 1, p. 9.

Table 1a. Minimum specifications for TUP and TUN.

	type	U_{ce_0} max	I_c max	h_{fe} min.	P_{tot} max	f_T min.
TUN	NPN	20 V	100 mA	100	100 mW	100 MHz
TUP	PNP	20 V	100 mA	100	100 mW	100 MHz

Table 1b. Minimum specifications for DUS and DUG.

	type	U_R max	I_F max	I_R max	P_{tot} max	C_D max
DUS	Si	25 V	100 mA	1 µA	250 mW	5 pF
DUG	Ge	20 V	35 mA	100 µA	250 mW	10 pF

Table 2. Various transistor types that meet the TUN specifications.

TUN

BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP

BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG	
BA 127	BA 318	OA 85	
BA 217	BAX 13	OA 91	
BA 218	BAY61	OA 95	
BA 221	1N914	AA 116	
BA 222	1N4148		
BA 317			

Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification (I_c max = 50 mA).

	NPN	PNP
	BC 107	BC 177
	BC 108	BC 178
	BC 109	BC 179
V_{ce_0} max	45 V	45 V
	20 V	25 V
	20 V	20 V
V_{eb_0} max	6 V	5 V
	5 V	5 V
	5 V	5 V
I_c max	100 mA	100 mA
	100 mA	100 mA
	100 mA	50 mA
$P_{tot.}$ max	300 mW	300 mW
	300 mW	300 mW
	300 mW	300 mW
f_T min.	150 MHz	130 MHz
	150 MHz	130 MHz
	150 MHz	130 MHz
F max	10 dB	10 dB
	10 dB	10 dB
	4 dB	4 dB

The letters after the type number denote the current gain:
A: α' (β, h_{fe}) = 125-260
B: α' = 240-500
C: α' = 450-900.

Table 6. Various equivalents for the BC107, -108, . . . families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107	BC 177		
BC 108	BC 178		
BC 109	BC 179		
BC 147	BC 157		P_{max} = 250 mW
BC 148	BC 158		
BC 149	BC 159		
BC 207	BC 204		
BC 208	BC 205		
BC 209	BC 206		
BC 237	BC 307		
BC 238	BC 308		
BC 239	BC 309		
BC 317	BC 320		$I_{c max}$ = 150 mA
BC 318	BC 321		
BC 319	BC 322		
BC 347	BC 350		
BC 348	BC 351		
BC 349	BC 352		
BC 407	BC 417		P_{max} = 250 mW
BC 408	BC 418		
BC 409	BC 419		
BC 547	BC 557		P_{max} = 500 mW
BC 548	BC 558		
BC 549	BC 559		
BC 167	BC 257		169/259 $I_{c max}$ = 50 mA
BC 168	BC 258		
BC 169	BC 259		
BC 171	BC 251		251 . . . 253 low noise
BC 172	BC 252		
BC 173	BC 253		
BC 182	BC 212		$I_{c max}$ = 200 mA
BC 183	BC 213		
BC 184	BC 214		
BC 582	BC 512		$I_{c max}$ = 200 mA
BC 583	BC 513		
BC 584	BC 514		
BC 414	BC 416		low noise
BC 414	BC 416		
BC 414	BC 416		
BC 413	BC 415		low noise
BC 413	BC 415		
BC 382			
BC 383			
BC 384			
BC 437			P_{max} = 220 mW
BC 438			
BC 439			
BC 467			P_{max} = 220 mW
BC 468			
BC 469			
	BC 261		low noise
	BC 262		
	BC 263		