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ELEKTOR 10

Swirler Sig



ACG

automatic call-sign generator

Digital watch

a single-chip with day and date

Morse decoder

converts morse into running script

Master oscillator (2)

two designs for use in organs

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The use of morse is avoided like the plague by most radio amateurs. Once the R.A.E. has been passed the morse key is often relegated to the junk box. This is a pity as morse telegraphy has advantages over telephony, in terms of bandwidth and for long-distance working. To encourage those with an aversion to 'key-bashing' the morse typewriter was developed, which makes CW operation child's play.	
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Whereas a couple of years ago a digital watch was available only as a two chip design costing around £ 40 for the two IC's, it is now possible to obtain a single IC that will perform all timekeeping functions, and will display date as well as time, for around £ 10. Two watches are in fact described in this article. A low-cost, relatively easy to construct version, and a more miniature version for the advanced constructor.	
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A title that needs some further explanation. When logic circuits are driven from 50 Hz mains pulses, unsatisfactory behaviour can be expected since the exact pulse shape requirements for proper functioning of the gates cannot, usually, be met by pulses derived straight from the sinusoidal mains. This article discusses those requirements and establishes a few basic principles in connection with digital logic driving pulses.	
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AUTOMATIC CALL-SIGN GENERATOR

According to the condition of authorization and the legal rules and regulations, a radio amateur must transmit his call letters at least three times at the beginning and end of each transmission. During the transmissions, the call letters must be included at least once per ten minutes in the text. The manner in which this should be done is not further specified. This offers the possibility of using an automatic call generator, since there is no objection to transmitting the call sign in morse. It will, however, be clear that the transmitted signal must meet a number of requirements.

Design considerations

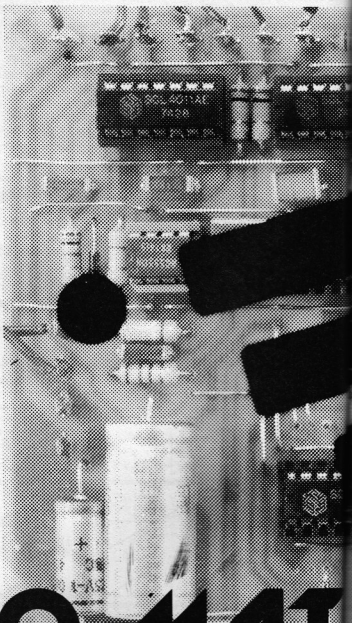
Besides the fact that the call sign must be repeated several times, the conditions of authorization also mention the permissible transmission types and the maximum permissible bandwidth. For ordinary telegraphy with an unmodulated carrier (A1) a maximum bandwidth of 0.2 kHz is specified. The band-

width actually used depends on the way in which the carrier is switched. Since the carrier would normally be switched with a morse key, it is sufficient in this design to use a relay which replaces the key. The same relay can be applied for F1-modulation (frequency shift keying). It remains to be seen, however, whether it is possible to combine A1 for the call sign with one of the A3 modulations (S.S.B.) for the speech and, similarly, whether F1 morse can be combined with F3 (FM or PM) speech. At the transmitter either of these combinations will involve little difficulty. For the receiver, however, only a combination of A1 morse and A3A or A3J speech might give reasonable results, because then the BFO in the receiver is switched on.

From the above considerations it follows that A1 and F1 modulation, although normally considered 'ideal' for morse, really do not qualify for automatic transmission of the call sign in the

Every radio amateur knows that his (or her) call sign must be transmitted at least once per ten minutes during a QSO. This requirement can easily be fulfilled by using an automatic call generator which transmits the call every ten minutes in morse.

The call generator described here can be operated automatically and manually, so that if required a QSO can be started and ended with the call in morse.



MORS-O-MAT

course of an A3 or F3 speech transmission. Consequently, the relay output would seem redundant. It can, however, be of excellent service in tone-modulated telegraphy. The contacts of the relay can then be used for switching over from microphone amplifier to tone generator.

The tone generator can be of a simple design; for instance a square-wave generator followed by a selective filter. The filter is necessary to limit the bandwidth. To obtain the purest possible signal, an active filter is used in this design, so that an almost sinusoidal signal is obtained. Furthermore the circuit is designed to give 'soft' on and off switching of the signals, so that the bandwidth of the signal remains well within the limit of 2.2 kHz (A2) or 3 kHz (F2). For SSB the bandwidth is of course no problem at all in this case. Another point for consideration is the character capacity and the programming method. The maximum number of call

letters is six. This applies to practically every country. Since each letter contains a maximum of four dots and/or dashes - only the digit that usually forms part of the call is longer - a memory capacity of 24 positions should be more than sufficient. If the circuit is also to be used in mobile transmitters, it must be possible to extend the memory capacity to accommodate the /A or /M suffix. A memory capacity of 32 positions will be sufficient in practically all cases - the theoretical limit to the length of the call sign is 34 positions. Considering that not all letters consist of four dots and/or dashes, this memory capacity will often be too great. The theoretical minimum is 10 positions, e.g. ET3TEE. This is, however, no objection since the circuit can be so designed that the memory can be expanded or reduced as required.

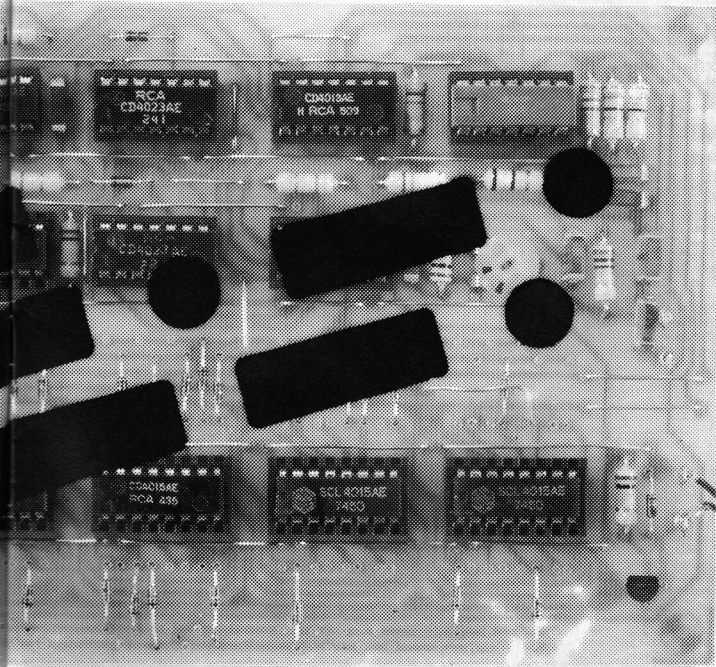
The overcapacity of the memory can, of course, also be used for adding a start (---) and stop signal (---); this will

improve the legibility of the very short CW message.

When determining the memory capacity it was assumed that the spaces between the dots and dashes need to be programmed separately; after each dot or dash a space equal to one dot will automatically follow. Furthermore it is assumed that no separate place in the memory is needed for programming a letter space (length three dots). This letter space will, however, have to be programmed in some way.

The programming of dots and dashes can be achieved in a simple way: the apparatus transmits a dot unless a dash is programmed. Since the call generator must always produce the same sequence, a ROM (read only memory) is the obvious choice. Considering that programming is quite simple, this ROM can be a diode matrix. It can be scanned by means of a shift register.

For generating the dots and dashes the choice fell on two adjustable mono-



stable multivibrators, with a 1:3 ratio of the timing capacitors so that they produce pulses in the same time ratio. Monostable multivibrators are used because they offer the possibility of designing a kind of programmed oscillator which steps through the sequence at the correct rate despite the absence of a clock generator.

The final design consideration concerns the choice of ICs. Two IC families qualify.

It would seem attractive to make use of TTL ICs because of their low price. However, they do involve quite a number of drawbacks. The switching threshold is rather low (about 1 V), so that the sensitivity to interference is correspondingly high. Furthermore, the sensitivity to strong HF fields is also quite high. Another disadvantage in this particular application is the relatively high switching speed of TTL ICs, as this can easily give rise to spurious signals at very high frequencies.

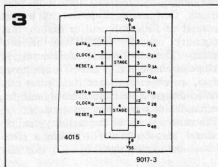
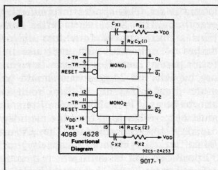
These drawbacks apply to a far lesser extent for the Cos-Mos family. The switching threshold is no less than 45% of the supply voltage. At a sufficiently high supply voltage the interference sensitivity can be one tenth of that for TTL ICs. Furthermore, the highest operating frequency is lower, so that the switching speed is correspondingly less. Another great advantage of the Cos-Mos ICs is their low current consumption. Of the two IC families mentioned, the Cos-Mos family is undoubtedly the best choice for this design.

The circuit

The heart of the circuit consists of two monostable multivibrators, which determine the length of dot and dash respectively. Both multivibrators are on one chip: the CD 4098 or the (MC 1) 4528 (see figure 1). Both types have the same pinning and show hardly any differences in specification. The prefixes CD and MC1 indicate the manufacturer, other prefixes also occur.

The pulse time of the multivibrators can be calculated fairly accurately with the formula $T_X = R_X \cdot C_X$, where R_X and C_X are the external time-determining elements. It is desirable to approach the dot/dash ratio of 1:3 as closely as possible. The high input impedance of the Cos-Mos IC means that a high resistance value can be used for the time-determining element. This has the advantage that the capacitors can be kept relatively small, so that no electrolytic capacitors (with their high tolerances, typically -10 and +60%) need be used. The deviation from the dot/dash ratio depends mainly on the external components: since the two monostable multivibrators are mounted on one chip, the differences between them will be negligible.

Even if the pulse times — and hence the transmitting speed — are variable, the ratio of 1:3 in pulse times must be maintained. This means that the ratio of the timing capacitors must always be 1:3, whilst the potentiometers which

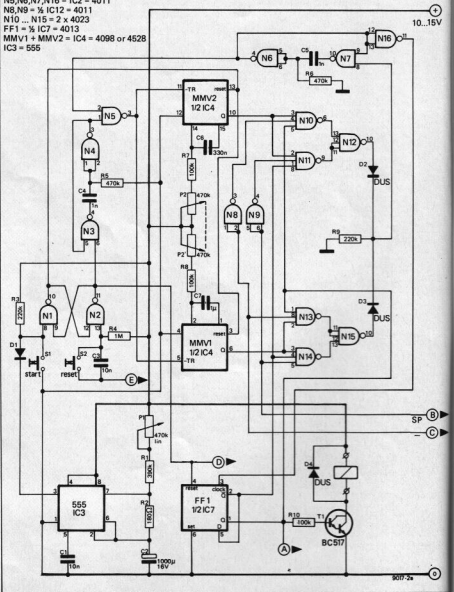


set the pulse widths must be coupled; a stereo potentiometer is the obvious choice. Since components with exactly the nominal value occur only in fairy tales, the ordinary commercial types will have to do. As regards the capacitors this means a tolerance of 5% and for the potentiometers a mistracking of less than 6 dB. In practice it is found that the ratio 1:3 can be reasonably well approached with these components, so they are obviously better than the specifications would lead one to expect! If necessary, the ratio of 1:3 can be very accurately approached by slightly altering one of the capacitor values (trimming).

The multivibrators are followed by simple selection logic (N8...N15, see figure 2a). Depending on the programming this logic will pass on a dot or a dash. Feedback via N7...N5 ensures retriggering of the multivibrators at the end of each dot/dash or space. Simultaneously FF1 receives a clock pulse from N16, so that this flipflop changes

2a

N1...N4 = IC1 = 4011
N5, N6, N7, N16 = IC2 = 4011
N8, N9 = 1/2 IC2
N1...N4 = IC1 = 4011
N5, N6, N7, N16 = IC2 = 4011
N8, N9 = 1/2 IC2 = 4011
N10...N15 = 2 x 4023
FF1 = 1/2 IC7 = 4013
MMV1 + MMV2 = IC4 = 4098 or 4528
IC3 = 555



state. Consequently dot or dash and space are produced in turn, as the relay is switched on and off via T1. The same output of the flipflop is used to shift the memory (figure 2b) one position further. Since this shift register responds only to positive-going edges, this implies that it can change position only after two MMV times. At the end of the total sequence the start flipflop (N1/N2 figure 2a) is reset via a differentiating network.

The timer (555) connected as an astable multivibrator with an extreme pulse/pause ratio triggers the start flipflop every five to ten minutes, after which the programmed call letters are automatically transmitted.

A more detailed explanation of the circuit can be given by investigating how one total sequence is completed.

Operation

The entire circuit consists of a closed loop: the call generator starts and stops itself.

Starting and stopping is controlled by the SR flipflop consisting of N1 and N2. The sequence can be started either automatically (by the timer) or manually. For manual operation S1 applies one (or several!) negative edge(s) to the input of N1. The output of N1 then becomes logic '1' and the output of N2 becomes logic '0'. The same happens when the timer (IC3) produces its very short negative pulse. The positive part of the five to ten-minute period of the timer (this is the charge time of C2 to the triggering point) is determined by the sum of P1, R1 and R2. The formula for this delay time is: $t = 0.693 (P1 + R1 + R2)C2$. The length of the negative starting pulse is determined by the discharge time of C2 via R2 to the second triggering point.

The time for this part of the period is given by the formula: $t = 0.693 R2 \cdot C2$. Considering the value of R2 the discharge time of C2 will be about 1/8 second. This is sufficiently short to ensure a reliable cycling of the programme.

are still '0' (all shift registers reset), N13 and N14 are still blocked. Furthermore FF1 is reset, so the Q output of this flipflop is also '0'. Consequently the oscillator (N17 + N18) and N10 are blocked. Thus the only signal that can be transmitted is a short space; the duration is determined by MMV2, and FF1 is reset. Because the output of N11 becomes logic '0', a '1'-level will appear across R9. This level changes back to '0' as soon as the period time of MMV2 has elapsed. The negative edge then occurring triggers the pulse shaper consisting of N7 and N6. The negative-going edge of this pulse triggers FF1 via N16 and the positive-going edge retriggers the MMVs via N5. The short delay between the end of the first MMV period and the start of the second has very little effect on the ratio of 1:3. The positive-going edge of the Q output of FF1, coinciding with the end of the MMV period, triggers the shift registers via line 'A'.

The shift registers are 4015s (see figure 3).

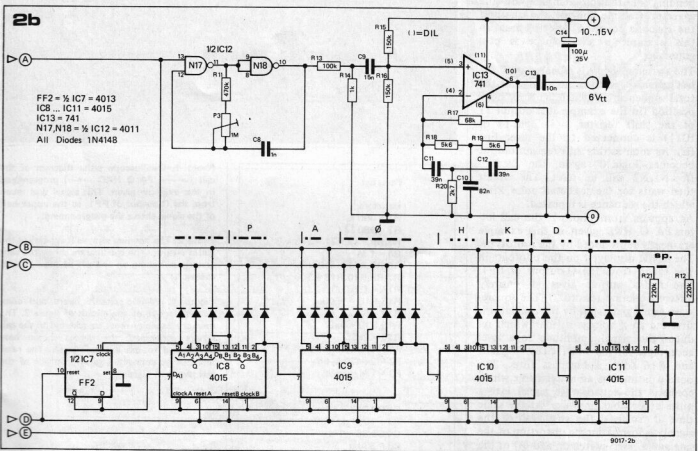


Figure 1. The heart of the circuit consists of two monostable multivibrators. The IC 4089 (or 4528) comprises two MMVs on one chip, so that the characteristics of the two MMVs are equal to within very close tolerances.

Figure 2. The complete diagram of the call generator. The abbreviation SP stands for space. The diode programming shown in figure 2b is given as an example.

Figure 3. The shift register is one of the most important parts of the memory. The type 4015 used here contains two four-bit shift registers.

As long as the SR-flipflop is in the 'stop' position, MMV1 and MMV2 are blocked by a logic '0'-level on the reset inputs. As soon as N1 becomes logic '1', the MMVs can be triggered with a negative edge at their 'TR' inputs. To avoid triggering problems the '0'-level from N2 is converted into a short negative pulse by N3 and N4. N5 inverts this signal so that the negative trailing edge will trigger the MMVs. The outputs Q1 and Q2 of the MMVs now change to logic '1'.

The selection logic determines what happens next. Since both programme lines (B and C)

The IC 4015 comprises two four-bit shift registers which must be triggered by a positive-going edge. The reset inputs are activated by a logic '1'-level. The shift registers are series-in/parallel-out types. A logic level on the data input is shifted to the A₁-output on the positive-going edge of the clock signal, and from there on down the chain. Since, initially, all shift registers are reset, IC9, IC10 and IC11 will only pass on '0'-information. The first shift register receives its data input from FF2. Initially, this flipflop is reset, so the Q output is logic '1'. This is the infor-

mation which is shifted to the A_1 -output on the positive-going edge of the first clock pulse. The positive-going edge then occurring at the A_1 -output of the shift register sets FF2 so that the information at the data input of IC8 goes from logic '1' to logic '0'.

As a result of the Q-output of FF1 becoming logic '1' the oscillator (N17/N18) is able to start. Furthermore the blocking of N10 and N13 is removed and N11 and N14 are blocked instead, so that now the programme line (C) determines what signal will be transmitted. Since the first signal to be transmitted in this example is a dash, the programme line becomes logic '1' via the diode from output A1 of IC8. N13 is now open and N10 remains blocked. A logic '1'-level occurs across R9, as before, but the duration is now that of a dash. At the end of this dash the cycle described above is repeated. The MMVs are retrigged again and the state of the output of FF1 changes. The oscillator is blocked and a space is transmitted. Depending on the programming on the space programme line (B), the length of the space is equal to a dot or dash. In this example a short space is programmed.

The switching cycle is repeated until the last memory position necessary for the total sequence is reached. This memory position (in the example it is output 31 of the shift register — i.e. pin 11 of IC11) is connected to the reset line (E). As soon as this shift register output becomes logic '0' again, the SR flip-flop N1/N2 will be reset. The circuit then waits for the next start pulse, after which the sequence is repeated.

As appears from photo 1, the call letters PA Ø HKD given in this example are neatly reproduced by the prototype. The signal displayed on the photograph was taken from the Q-output of FF1. The audio output gives an entirely different picture (photo 2). The square-wave signal generated by the oscillator is first fed to a voltage divider which reduces the signal amplitude to a level acceptable for the 741 (IC13). C9, R15 and R16 form a highpass filter. The opamp is used as an active filter which converts the square-wave signal into a quite acceptable sine wave. At the same time it 'softens' the switching of the signal. A low harmonic distortion of the sine and a 'soft' switch on and off of the signal are necessary to attain a narrow bandwidth. The results obtained with the given circuit are shown in photo 2. This clearly shows the gradual attack and decay characteristics of the signals. The dark lines in the center of the picture are due to residual distortion of the sine wave; remnants of the original square wave are seen as a kind of cross-over distortion. This distortion is a useful aid during initial trimming of the oscillator: when the oscillator is set to the correct frequency (with P3) the output amplitude is at its maximum and the cross-over is located at the zero crossing of the sine-wave. In the prototype the oscillator fre-

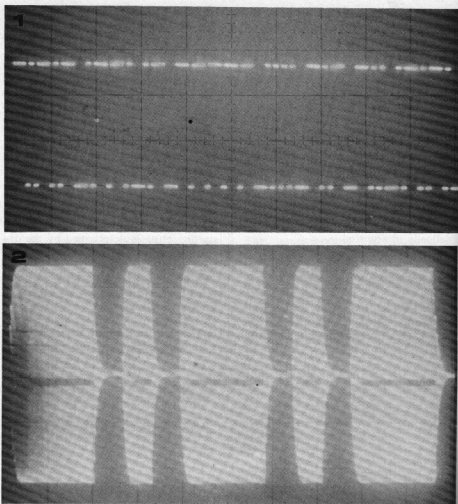


Photo 1. Oscilloscope pulse diagram of the call (----- PA Ø HKD ----) programmed in the example given. This signal was taken from the Q output of FF1, so the upper half of the signal shows the programming.

Photo 2. The opening sign, as it appears at the audio output. The oscillogram shows the very gradual switching on and off of the dots and dashes.

Figure 4. Printed circuit board and component layout of the circuit of figure 2. The memory capacity must be adapted to the call letters concerned; the diodes shown here correspond to the example given. The reset line can be connected to any output of the last two shift registers.

Parts list

Resistors:
 R1 = 390 k
 R2 = 180 Ω
 R3, R9, R12, R21 = 220 k
 R4 = 1 M
 R5, R6, R11 = 470 k
 R7, R8, R10, R13 = 100 k
 R14 = 1 k
 R15, R16 = 150 k
 R17 = 68 k
 R18, R19 = 5k6
 R20 = 2k7
 P1 = 470 k, lin.
 P2 = 2x 470 k, lin.
 P3 = 1 M, preset

Capacitors:
 C1, C3, C13 = 10 n
 C2 = 1000 μ, 16 V
 C4, C5, C8 = 1 n
 C6 = 330 n
 C7 = 1 μ
 C9 = 15 n
 C10 = 82 n
 C11, C12 = 39 n
 C14 = 100 μ, 25 V

Semiconductors:
 D1 ... D4 = DUS
 T1 = BC 517
 IC1, IC2, IC12 = 4011
 IC3 = 555
 IC4 = 4098 or 4528
 IC5, IC6 = 4023
 IC7 = 4013
 IC8 ... IC11 = 4015
 IC13 = 741

quency was 810 Hz with the component values shown and using standard components. Small variations due to component tolerances are possible, but the frequency will never exceed 1 kHz so that the bandwidth of the signal falls amply within the requirements.

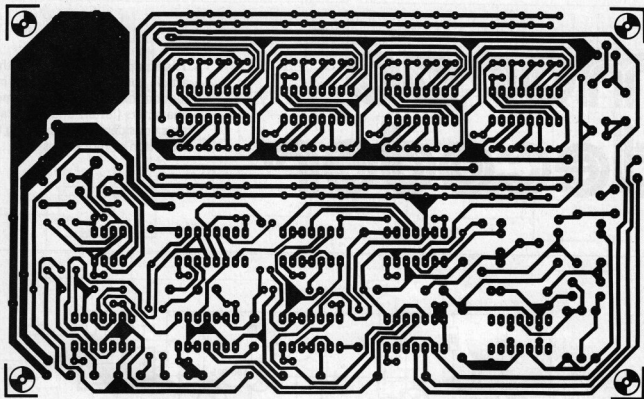
The printed circuit board

Figure 4 shows the p.c. board and component layout.

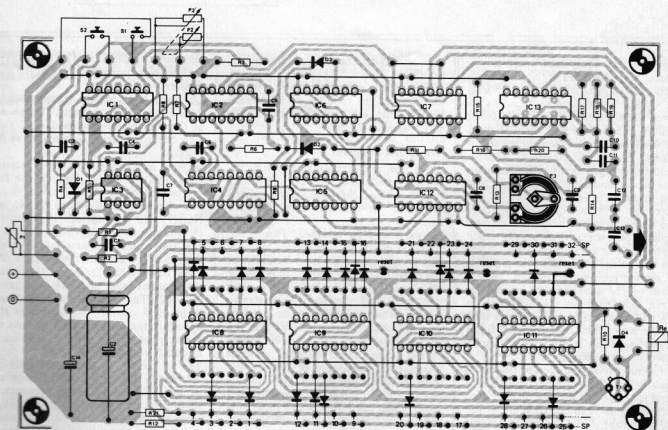
The board is designed for a memory with 32 positions. If necessary, the capacity can be extended or reduced as required. Extensions will, however, have to be mounted outside the p.c. board.

PA Ø HKD

4



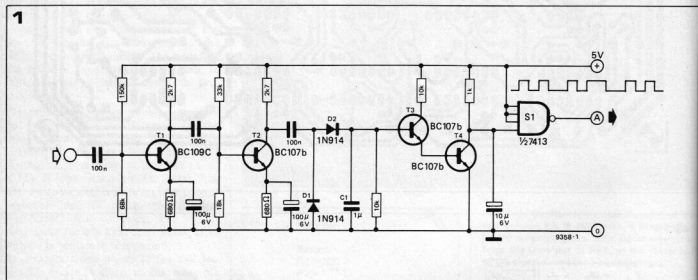
4



R. ter Mijtelen

morse decoder

The equipment described in this article converts morse coded information into normal alphanumeric characters (letters and numerals), thus considerably simplifying the reception of morse messages.



The decoding equipment receives the message to be decoded in the form of an audio frequency morse signal at the output of an existing communications receiver. Each incoming character is stored until it is complete and then decoded and displayed on a twelve-segment alphanumeric display. A number of displays could be arranged in a line so that complete words could be displayed as running script. The displays used in the prototype were home-made, but those who do not wish to construct their own displays could use a commercially-made display such as the Litronix Data Lit 16. The equipment comprises four sections. A signal processing section, which amplifies the audio output of the receiver, rectifies it and shapes the pulses into TTL compatible logic levels; a shift register into which the processed signal is fed to assemble it into parallel form; a memory, and a decoder.

The signal processing section (figure 1) operates as follows: the incoming audio signal is amplified by T1 and T2 and rectified by D1 and D2. C1 removes the A.C. component of the signal, leaving a series of D.C. pulses with some superimposed a.f. The pulse train is amplified and limited by T3 and T4, and finally a Schmitt trigger S1 produces a TTL com-

patible output. The result, at the output of S1, is thus a TTL pulse train, the lengths of the pulses being equal to the duration of the tone bursts that made up the dots and dashes of the morse audio signal.

The Shift Register

Since the morse characters are transmitted serially (i.e. the dots and dashes that make up a character are transmitted one after the other) it is necessary to assemble each character in parallel form before it can be decoded. This is the function of the shift register of figure 2. The morse pulse train from output A of the signal processor is fed into the input of a serial in-parallel out shift register and is clocked through the register to appear in parallel form at the outputs. The maximum number of bits that the shift register must store is determined by the longest morse character, which is numeral '0', consisting of five dashes. Starting with a dot as a basis (1 dot occupies 1 bit in the shift register) then a dash, which has a duration of three dots will occupy 3 bits in the shift register, and the spaces between dots and dashes, being of one dot duration, will occupy 1 bit. Thus the longest character, zero, consisting of five dashes with four spaces

between, requires a total of 19 bits. This is thus the required capacity of the shift register.

The shift is made up of three cascaded 74164 8-bit shift registers, though not all the available bits are used.

The circuit of figure 2 operates as follows:

As soon as a morse character is received then input A will go high on the first dot or dash of the character. Via N5 this sets the set/reset flip-flops N1/N2 and N6/N7. The output of N6 takes the clear inputs of the shift registers high so that they can accept new data. The output of N1 takes the reset inputs of a 7490 IC1 low so that it can then count clock pulses from the clock pulse generator S2. The 7490 is connected as a divide-by-5 counter, so the pulses that appear at the output of N4 to drive the clock input of the shift register are a one-fifth of the clock frequency.

The character is thus eventually assembled in the shift register as a sequence of logic '1's' and '0's'. A sequence of three '1's' corresponding to a dash, a single '1' corresponding to a dot and a '0' corresponding to a space between dots and dashes. During the space, when input A goes low the reset input of IC2 will go low and IC2 will count

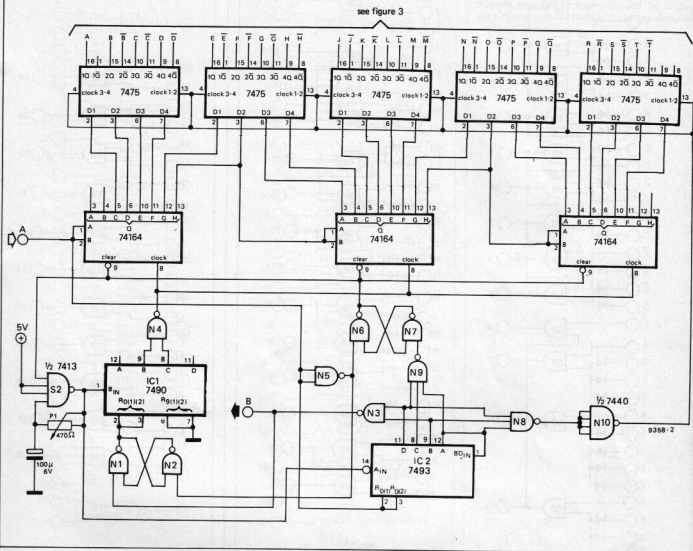


Figure 1. Signal processing stage of the decoder. The output, point A is connected to point A of figure 2.

Figure 2. Circuit of the shift register and memory.

clock pulses from S2. However, while dots and dashes are still appearing at input A IC2 will be reset every time input A goes high. At the end of the morse character, however, there will be a space of three dots duration before the start of the next character, and this space is recognised as an indication that the character is complete and may be stored in the memory and decoded. When input A goes low at the end of a character IC2 can then count clock pulses unhindered.

If no further data has appeared at input A by the time IC2 counts the 10th clock pulse then the output of N3 will go low, resetting flip-flop N1/N2 and thus IC1. With its reset inputs held high by N1 IC1 can no longer count, so no further pulses reach the clock input of the shift register. At this stage therefore, the morse character is held in the shift register, with a 2-bit space ('0's) on outputs A and B of the left-hand 74164 due to the 10 clock pulses counted after the completion of the character.

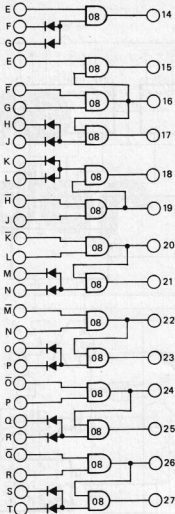
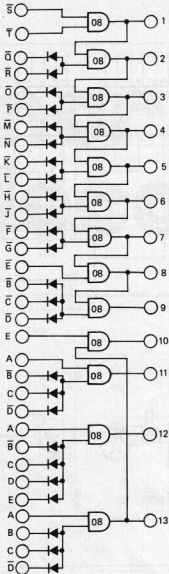
On the 11th clock pulse the output of N8 will go high and the data present on the register outputs will be entered in the memory, which consists of 5 7475 4-bit latches. On the 12th clock pulse the

output of N10 will go low again, disabling the clock inputs of the 7475's so that the data is stored in the memory. Finally, on the 13th clock pulse the output of N9 will go low, resetting flip-flop N6/N7. This clears the shift register, in preparation for the next character. The morse character stored in the memory is now decoded and displayed.

The Decoder

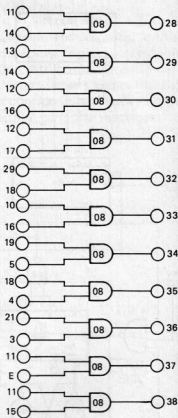
The latches in the 7475 have both Q and Q outputs, so both the data and its complement are stored. This is very useful as both the data bits and their complements are used in the decoder. The decoder is split into three sections. The outputs of the memory are first decoded into 'groups' (figure 3a,b). The groups are then decoded into one of 36 outputs for each character (figure 3c, d) and finally the 36 outputs are decoded into a 12 segment format to drive the display. Table 1 shows how each morse character appears at the outputs of the memory (complements not shown) with a cross representing a logic '1'. A group of three crosses, of course, represents a dash, a single cross a dot, and no cross, a space. It can be seen that there are groups of crosses common to several characters, where dots or dashes coincide in differ-

3a



all diodes DUS 9358 3a

3b

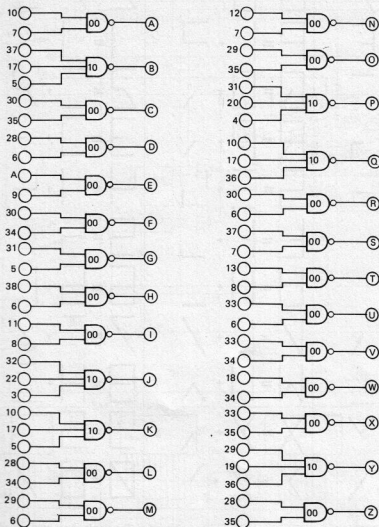


9358 3b

Table 1

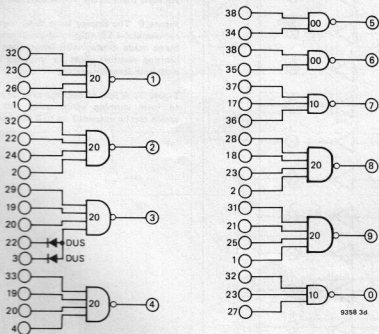
	A	B	C	D	E	F	G	H	J	K	L	M	N	O	P	Q	R	T		A	B	C	D	E	F	G	H	J	K	L	M	N	O	P	Q	R	T			
A	X	X	X	10	X														7	S	X	11	X	X												7				
B	X		X	11	X	17	X	X	X										5	T	X	X	X	13													8			
C	X	12	X	X	X	16	X	18	X	X	X								4	U	X	X	X	10	X	16	X										6			
D	X	11	X		X	14	X	X											6	V	X	X	X	10	X	16	X	19	X								5			
E	X																		9	W	X	X	X	13	X	14	X	X	19	X							5			
F	X	12	X	X	X	16	X	19	X										5	X	X	X	10	X	16	X	18	X	X	X						4				
G	X	12	X	X	X	17	X	X	X										5	Y	X	X	X	13	X	14	X	X	19	X	21	X	X	X			3			
H	X	11	X		X	15	X												6	Z	X	11	X		X	14	X	X	18	X	X	X					4			
I	X	11	X																8	1	X	X	X	13	X	14	X	X	18	X	X	X	23	X	X	26	X	1		
J	X	X	X	13	X	14	X	X	18	X	X	X	22	X					3	2	X	X	X	13	X	14	X	X	18	X	X	X	22	X	24	X	2			
K	X	X	X	10	X	17	X	X	X										5	3	X	X	X	13	X	14	X	X	19	X	20	X	22	X			3			
L	X	11	X		X	14	X	19	X										5	4	X	X	X	10	X	16	X	19	X	20	X					4				
M	X	X	X	13	X	14	X	X											6	5	X	11	X		X	15	X	19	X							5				
N	X	12	X	X	X														7	6	X	11	X		X	15	X	18	X	X	X					4				
O	X	X	X	13	X	14	X	X	18	X	X	X							4	7	X	11	X		X	17	X	X	X	21	X	X	X				3			
P	X	12	X	X	X	17	X	X	X	20	X								4	8	X	11	X		X	14	X	X	18	X	X	X	23	X	X	X	2			
Q	X	X	X	10	X	17	X	X	X	21	X	X	X						3	9	X	12	X	X	X	17	X	X	X	21	X	X	X	25	X	X	X	1		
R	X	12	X	X	X	16	X												6	0	X	X	X	13	X	14	X	X	18	X	X	X	23	X	X	X	27	X	X	X

3c



9358 3c

3d



9358 3d

08 = 1/4 7408
 00 = 1/4 7400
 10 = 1/2 7410
 20 = 1/2 7420

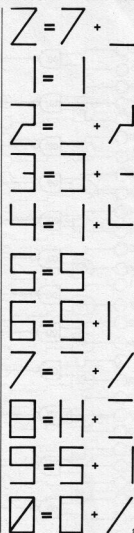
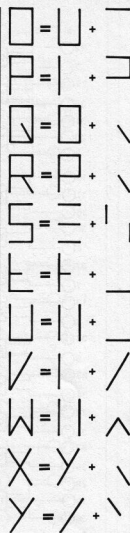
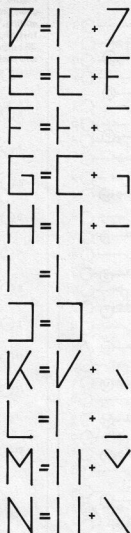
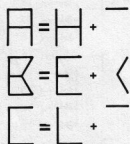
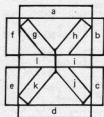
Figure 3. The decoder circuitry. The AND-gates in figures 3a and 3b are the group decoding. The group decoder outputs are further decoded in figures 3c and 3d to give 36 outputs, one for each letter of the alphabet and each numeral.

ent characters. These groups are identified by numbers corresponding to the outputs of figure 3a/b. For instance, numerals 1,2,3 and 0 all contain group 13.

There are in all 38 groups. The 27 basic groups shown in table 1 are decoded by the circuit of figure 3a; a further 11 combinations are decoded according to figure 3b. The relevant groups for each character are then combined by the circuit of figure 3c,d which gives 36 unique outputs, one for each character.

Note that in figures 3c and 3d the circled outputs are the decoded alphanumeric outputs. Uncircled outputs are the group outputs (all outputs of figures 3a and 3b). Where an input is marked with an uncircled letter this corresponds to a direct connection to the appropriate output of the memory. An uncircled number means a connection to the output of the appropriate group decoder. It can be seen that some of the group decoder stages require only inputs from the memory, others require inputs from the outputs of other group decoder stages, and still others require a combination of both. The same is true of the alphanumeric decoders. Decoder E

4



9356 4

(figure 3c), for example, requires inputs from group decoder 9 and also direct from output A of the memory. In figure 3a to 3d the numbers inside the gates refer to the type of gate required, thus 20 = 7420.

The final stage in the decoding is to change the 36 outputs of the alphanumeric decoder into 12 segment format. This is the function of the circuit of figure 5. Since the outputs of figure 3c and 3d are normally high (i.e. when an output is active it is low) figure 5 is designed to accept low inputs. Figure 4 shows the display font of the twelve-segment readout, and shows how certain characters are built up from simpler characters or segment groups.

The outputs of the circuit of figure 5 are connected to the lamp driver circuit of figure 6, which drives the display. If a commercial LED display is used rather than a home-made display then of course segment resistors must be included in series with the output of the inverters to limit the current.

Running Script

As mentioned earlier it is possible to arrange several displays in a line to form running script that travels to the left along the line of displays. The circuitry to do this is given in figure 7 and operates as follows. While a morse character is being received output B of figure 1 is

6

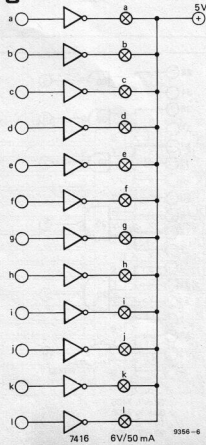
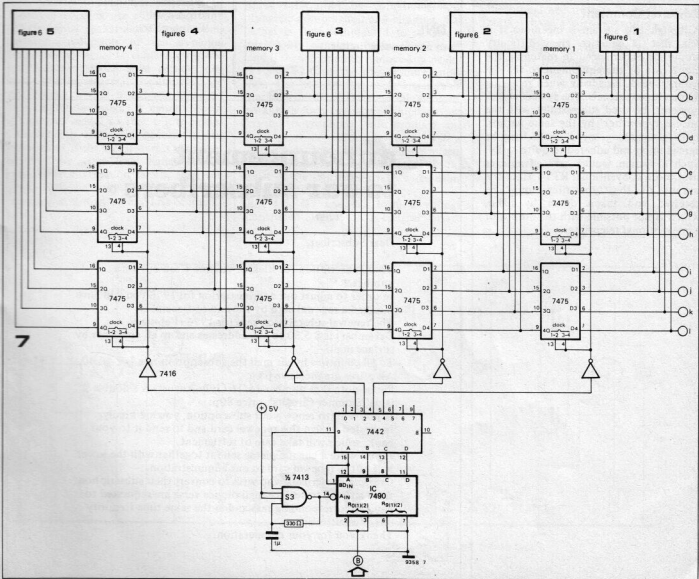
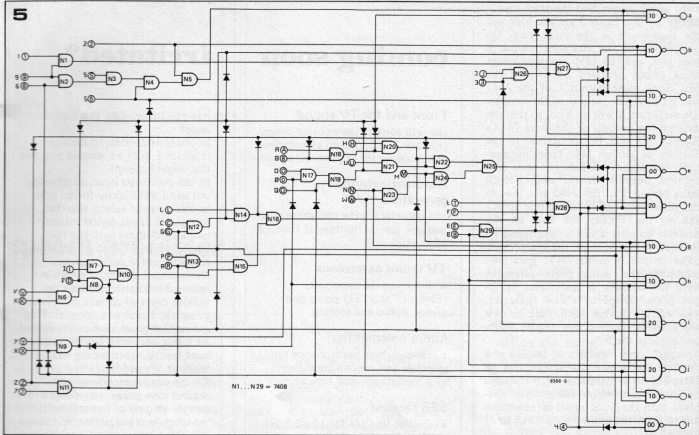


Figure 4. The display font used, showing how the more complex characters are achieved by combining simpler ones.

Figure 5. The final stage of the decoder takes the 36 outputs of figures 3c and 3d and converts them to the 12-segment format.

Figure 6. The display lamp drive circuit. If a commercial LED display is used instead of a home made display with lamps then current limiting resistors must be included in series with each inverter output.

Figure 7. A line of displays may be arranged to form running script using this circuit, which can be extended up to 8 displays.



high, which means that the reset inputs of the 7490 in figure 7 are also high and the counter is in the reset state. On completion of the character output B goes low, and the 7490 can now count clock pulses provided by S3. On the first clock pulse output 1 of the 7442 will go low. The output of the inverter connected to it will go high, so that the data on the outputs of the three 7475's labelled M3 will be transferred to the outputs of latches M4. Thus, momentarily the latches will have the same data on their outputs. On the second clock pulse output 2 of the 7442 goes low, so the data from M2 is transferred to M3 and so on. Finally the data on the decoder outputs a to l is transferred to the outputs of M1. On the ninth clock pulse output 9 of the 7442 goes low, inhibiting the clock pulse generator until the counter is again reset by input B on receipt of a new character. The effect is that each time a new character is received the display shifts one place to the left.

Although only five sets of latches and displays are shown the system can be extended to a maximum of 8 displays by connecting extra latches and displays with the clock inputs of the latches driven from the unused outputs (5 to 8) of the 7442.

Editorial Comment

Although this system is ingenious it is felt that in practice great difficulty would be experienced in matching the clock rate of the equipment to the signalling speed, especially when receiving manually sent signals. The system could, however, be used successfully with the 'morse typewriter' by the same author, since a signalling speed could then be agreed upon and adhered to quite easily. Such a system would have advantages over more conventional RTTY since the output of the typewriter could be received and taken down by hand, which is not possible with the output of a conventional teleprinter. ■

coming soon

Front-end for TV sound

this will convert the existing design (Elektor 2, p.236) into an independent receiver for tv (and fm) sound.

Automatic rhythm generators

add-on units for the minidrum that will give several rhythms at the flick of a switch.

TV tennis extensions

additions to the basic game (Elektor 7, p.1111) giving new games, noises and scoring.

Audio preamplifier

a low-cost, high performance pre-amplifier and control amplifier with 'remote control' capability.

SSB receiver

a sensitive (0.5 μ V for 12 dB S/N) receiver for single sideband transmissions.

DNL

dynamic noise limiter.

irritated?

Are you irritated by this digital issue?

In our introduction to Elektor (Elektor 1, p.5) we warned you that this might happen!

In this particular issue, admittedly, our hand was slightly forced: the 'morse-designs' belong together, and part 2 of the digital master oscillator follows part 1 in the previous issue. This does not leave much room for anything else.

However, we do try to maintain a reasonable balance between the various types of circuits (simple or complex, digital or analogue). This means that those who are overjoyed with this issue may well be irritated next month, when we try to do without '0's and '1's.

On the continent, where our readers have grown accustomed to a certain amount of unpredictability, we often hear the phrase 'Wir lassen uns gerne überraschen!' - which can be roughly translated as 'Go on, surprise us!'. We intend to.

announcement to our subscribers

Dear Subscriber,

Your subscription for Elektor volume 1 ran out with number 9.

In order to adjust our administration for 1976 you will have received a renewal card by the end of December.

The renewal-subscription rate for 1976 (February-December) is £ 5.80 to UK addresses and to all countries by surface mail.

To all countries by air mail the subscription rate is £ 10.40. All prices are inclusive p&p.

Please note that number 15/16 (July-August) is a double issue 'Summer Circuits', price 80p.

If you wish to renew your subscription, you are kindly requested to sign this renewal card and to send it to your bank, which will take care of settlement.

If you write a cheque please send it together with the lower half of the renewal card to our administration.

Overseas subscribers who wish to convert their subscription from air mail to surface mail or vice versa are requested to pay the corresponding rate and at the same time to notify our administration.

Thank you for your co-operation.

speech processor

To obtain the maximum efficiency when modulating a transmitter the modulation depth must be kept as high as possible for as much of the time as possible. This means that the modulating signal amplitude must be kept reasonably constant. Since speech most definitely does not have a constant amplitude some form of processing is called for.

The most commonly used methods of speech processing are clipping (cutting off the signal peaks) and dynamic compression (reduction of the dynamic range of the signal to achieve a reasonably constant signal level without distorting the waveform). The disadvantage of clipping is that it operates only on the amplitude peaks. It cannot boost a low level signal so that a low modulation depth may still occur. On the other hand, if the signal level is increased so that even low level signals give a reasonable modulation depth, then the peaks will be very severely clipped, resulting in distortion and loss of intelligibility.

Dynamic compression effectively boosts low level signals and cuts high level signals, thus achieving a fairly constant mean signal level. Unfortunately, due to the relatively slow response time of dynamic compressors, transient peaks may not be effectively suppressed, and overmodulation may occur.

The circuit described here overcomes these difficulties by combining both dynamic compression and clipping. The signal is first compressed to achieve a reasonably constant mean signal level, and is then clipped to remove any peaks. T1 and T2 form the microphone amplifier. The gain of this stage depends on the impedance of the microphone used, so that a high impedance, high output crystal microphone will produce the same sort of output levels as a low impedance, low output dynamic microphone. This avoids large variations in the level of the signal fed to T3 when using different types of microphone.

R5, C5, D1 and D2 form a voltage controlled attenuator. A control voltage

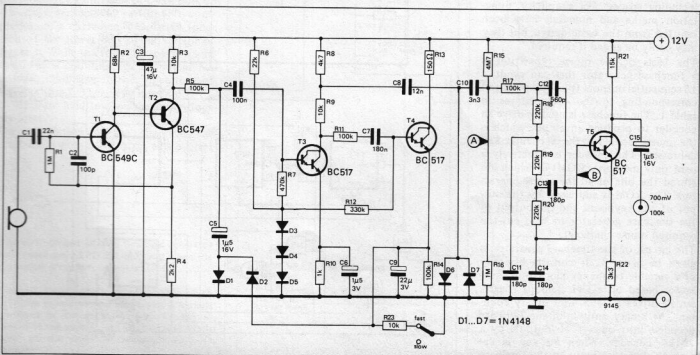
is fed back from the emitter of T4 to vary the forward bias voltage on D1. If the base voltage of T4 exceeds the voltage at the anode of D3 by about 0.5 V then the signal fed to the base of T3 is attenuated by R5, C5 and D1. R23 may be switched in or out to vary the compressor time constant. The compressed signal is taken from T3 via C8 and C10. Any peaks are clipped by D6 and D7. The degree of clipping depends on the ratio R8 : R9.

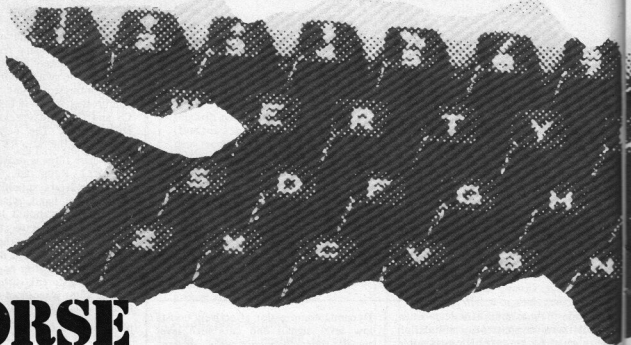
A low-pass filter is provided comprising T5, R17-R20 and C11-C14. The values given are suitable for operation in the 80 m band, where from 3 kHz upwards there should be a roll-off of at least 14 dB/octave. For working in other bands where the filter is not required points A and B may be joined and the passive filter components omitted. If a different turnover frequency for the filter is required then the capacitance values C11 - C14 should be multiplied by the factor $\frac{3}{f}$, where f is the

required turnover frequency in kHz.

Thus, for a frequency of 6 kHz, the capacitance values would need to be halved.

As a final constructional point it must be stressed that diodes D1 to D7 should be of reputable manufacture. Many of the 'unmarked untested' diodes on the market have a forward voltage drop of up to 1 V, and the circuit will not operate satisfactorily with these. When using the specified 1N4148, the voltage at the anode of D3 should be about 1.5 V to 1.7 V.



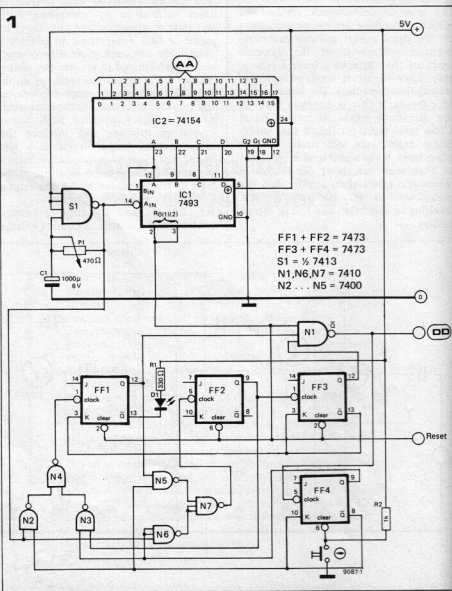


MORSE TYPEWRITER

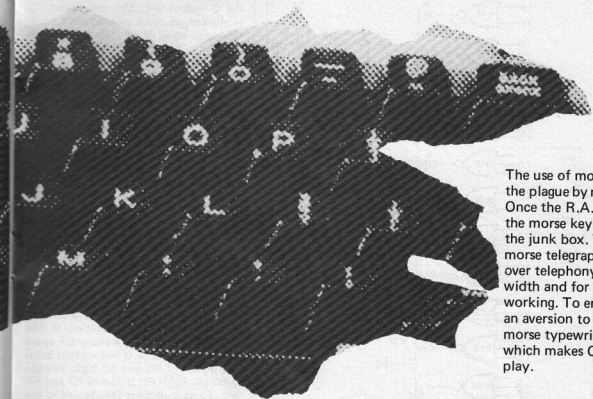
A morse signal, of course, consists of dots and dashes. The duration of dots, dashes, and the spaces between them bear fixed time relationships to one another. Starting with the dot as a basis, a dash has a duration of three dots. The space between dots and dashes has a duration of three dots. The space between complete letters three dots, and the space between words has a duration equal to six dots. On this basis it is easy to work out a time scale for the duration of each letter of the alphabet, in morse. This is shown in table 1. One cross represents a dot, and a row of three crosses, a dash. The longest duration letters are J, Q and Y, which have a duration of 13 dots, including spaces. For simplicity, punctuation marks and numerals have been omitted from the basic design, but they may easily be added if required.

The basis of the morse typewriter is a timebase generator that can produce 15 sequential outputs (plus rest position) corresponding to the 15 positions in table 1. The timebase is used to drive an encoder to produce an output which is the morse code for the particular key depressed. The encoder is effectively a read only memory (ROM) in which are stored the bits of all the morse characters. The ROM is addressed by the output of the keyboard and the output of the timebase generator to read out the required morse character.

The circuit of the timebase generator is given in figure 1. It consists basically of a variable frequency clock pulse generator based on a TTL Schmitt trigger, which drives a 7493 4-bit binary counter. The binary outputs of the 7493 are decoded into one of 16 outputs by a 74154 decoder. When no key is depressed the reset input to the timebase



R. ter Mijtelen



The use of morse is avoided like the plague by most radio amateurs. Once the R.A.E. has been passed the morse key is often relegated to the junk box. This is a pity as morse telegraphy has advantages over telephony, in terms of bandwidth and for long-distance working. To encourage those with an aversion to 'key-bashing' the morse typewriter was developed, which makes CW operation child's play.

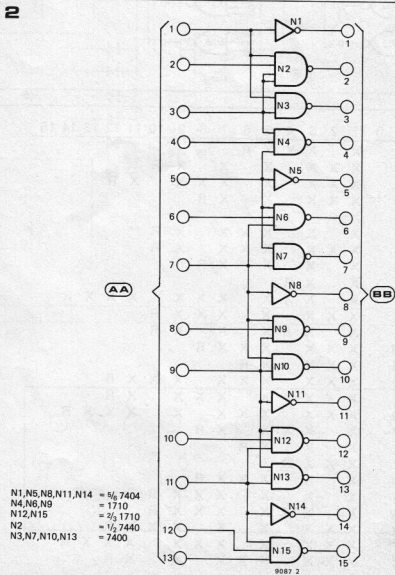
is high (this function will be explained in the discussion of keyboard operation). When a key is depressed the reset input goes low and the 7493 counts clock pulses. On completion of the morse character the counter is reset. Where in the count this occurs depends upon the length of the character. This is denoted by the letter R in table 1. For instance, the shortest character, E, requires only a single dot, so the counter is reset on the second clock pulse, whereas the longest characters, J, Q and Y, have a duration of 13 dots, so the counter is reset on the 14th clock pulse.

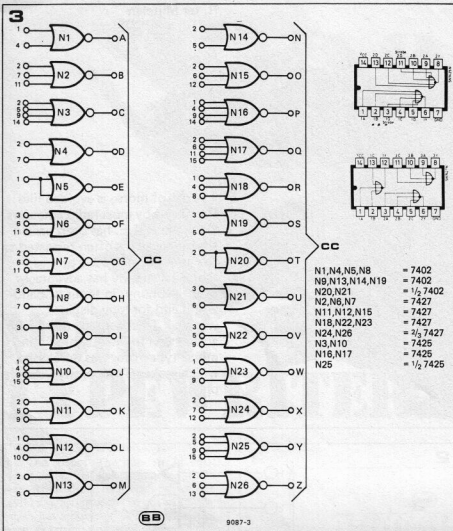
In order to produce letter spaces and word spaces it is necessary to inhibit the keyboard for a duration of three dots or six dots respectively after the completion of a character. This is the function of the lower part of the circuit of figure 1. While the reset input is low and the 7493 is counting, the output of N1 is high, inhibiting further operation of the keyboard. The clear inputs of FF1 to FF3 are held low, so these flip-flops are reset.

On completion of the character the reset input goes high. After this a letter

Figure 1. Circuit of the timebase generator with space key. LED D1 indicates when the typewriter is ready for the next letter.

Figure 2. Circuit of the group encoder, which produces groups of dots and dashes at various positions in the counter cycle. By combination of the appropriate groups using NOR-gates all the letters may subsequently be formed.





space is produced automatically. The Q output of FF4 is normally high and the Q output low. This means that N2 is blocked, so clock pulses cannot reach the clock input of FF1. However, clock pulses can pass through N6 and N7 to the clock input of FF2. Thus, on the next clock pulse after completion of the character IC1 is reset. On the second clock pulse the output of FF2 goes high. The Q output of FF2 is connected to the clock input of FF3 direct, and to the clock input of FF1 via N3 and N4, since one input of N3 is held high by the Q output of FF4, and one input of N4 is held high by the output of N2. On the third clock pulse, therefore, the Q output of FF2 goes low, and the Q outputs of FF1 and FF3 go high. All the inputs of N1 are now high, so the output is low and the keyboard is active once more. There is thus a space of three dots duration after completion of the character.

To obtain a word space it is necessary to depress the space key. This initiates a space of six dots duration in the following manner. Depressing the space key resets FF4. The Q output thus holds the inputs of N2 and N5 high, and the Q output holds the inputs of N3 and N6 low. Clock pulses are thus routed to the clock input of FF1 via N2 and N4, and the Q output of FF1 is routed to the clock input of FF2 via N5 and N7. FF1 to FF3 now function as a three-bit counter, and on the sixth clock pulse after completion of a character the Q outputs of FF1 and FF3 are both high, so the output of N1 goes low, activating the keyboard. It also clocks FF4 into the set condition (Q output high) where it will remain until the space key is next depressed. LED D1 indicates that the typewriter is ready for entry of the next character.

Of course the letter and word spaces only have any effect if the operator is typing very fast when they inhibit sending of the next character until the appropriate pause has elapsed. For proper operation the space key must be depressed before the preceding character has finished, and the next letter key must be depressed before the termination of the letter or word space. Of course, if one is a very slow typist then the pauses will be longer than those determined by the space circuitry anyway.

Encoding

The necessary encoding of the characters into morse can be considerably simplified by forming groups of dots and dashes that are common to several letters. These can easily be derived from table 1. For example, the letters B, C, D, G, K, M, N, O, Q, T, X, Y, and Z all begin with a dash, and the three longest letters J, Q and Y all terminate with a dash. Of course it is only possible to form common groups for several letters where these groups coincide in time, i.e. where they are directly above one another in table 1.

It is a relatively simple matter to design

Table 1

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	X	X	X	X	R											
B	X	X	X	X	X	X		X		X	R					
C	X	X	X	X	X	X	X	X	X			X	R			
D	X	X	X	X	X	X	X	R								
E	X	X	R													
F	X	X	X	X	X	X	X	X		X	R					
G	X	X	X	X	X	X	X	X		X	R					
H	X	X	X	X	X	X	X	R								
I	X	X	X	R												
J	X	X	X	X	X	X	X	X	X	X		X	X	X	R	
K	X	X	X	X	X	X	X	X	X	R						
L	X	X	X	X	X	X	X	X	R							
M	X	X	X	X	X	X	X	R								
N	X	X	X	X	X	R										
O	X	X	X	X	X	X	X	X	X	X	R					
P	X	X	X	X	X	X	X	X	X	X	R					
Q	X	X	X	X	X	X	X	X	X	X	X	R				
R	X	X	X	X	X	X	X	R								
S	X	X	X	X	X	R										
T	X	X	X	R												
U	X	X	X	X	X	X	R									
V	X	X	X	X	X	X	X	X	R							
W	X	X	X	X	X	X	X	X	R							
X	X	X	X	X	X	X	X	X	X	R						
Y	X	X	X	X	X	X	X	X	X	X	R					
Z	X	X	X	X	X	X	X	X	X	R						

4

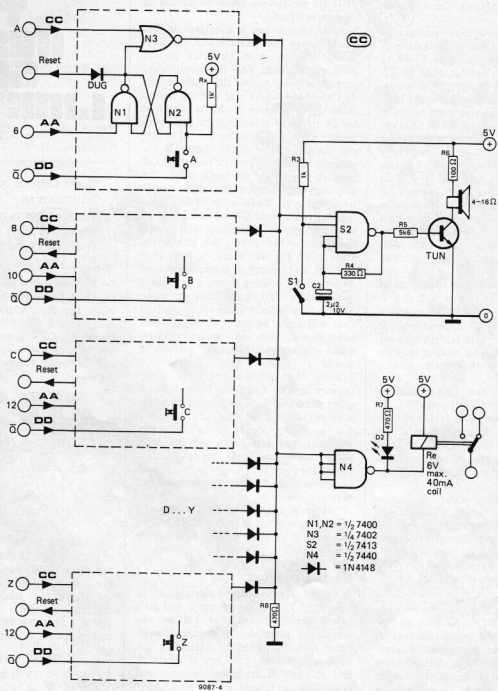


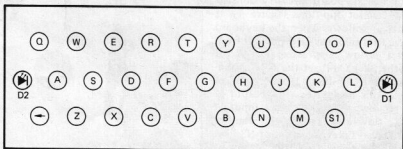
Figure 3. The 26 NOR-gates in which are combined the groups that make up each letter of the alphabet. The complete dot dash sequence for a letter is available at the appropriate NOR-gate output.

Figure 4. The circuit of the keyboard, which performs two functions. Depressing a key activates the counter cycle and also routes the appropriate letter output to control the transmitter relay and the audio oscillator. LED D2 provides a visual indication of the letter output.

Figure 5. Keyboard layout based on a standard typewriter format.

Table 1. Showing the duration of each morse character along the time axis. Each step corresponds to a duration of one 'dot'. Dashes have a duration equal to three dots, and spaces are equal to one dot.

5



an encoder to produce these groups. The groups may then be combined in various patterns to form the different letters.

The circuit of the group encoder is shown in figure 2, and its operation is fairly simple. The inputs 1 to 13 (AA) are connected to the outputs 1 to 13 (AA) of the 74154 in figure 1. Remembering that the 74154 has normally high outputs i.e. when an output is active it goes low, the circuit operates as follows: initially inputs 1-13 are all high, so the outputs 1 to 15 (BB) are all low. However, when the 7493 counts clock pulses each of the inputs AA will go low in turn. Looking now at N1 in figure 2, it is apparent that on the first clock pulse input 1 goes low, so output 1 goes high for the duration of one clock pulse. Output 1 therefore corresponds to a dot, and may be used in any letter starting with a dot.

Looking at N2 we see that the inputs of N2 are connected to inputs 1, 2 and 3. On the first, second and third clock pulses inputs 1, 2 and 3 respectively will go low, so output 2 will remain high for three clock pulses. This output may be used in any letter that starts with a dash.

It is easy to see how the inputs are combined in the NAND-gates N1 to N15 to produce dots and dashes at various points in the count sequence. All that now remains to be done is to take out the relevant groups of dots and dashes and combine them to form letters.

This is accomplished using NOR-gates (figure 3). Thus for a letter A, for example, outputs 1 and 4 from figure 2 are combined in N1 (figure 3) to give 'dot-dash'. Since N1 to N26 are NOR-gates, the outputs are, of course, inverted after passing through them.

The keyboard

Since NOR-gates N1 to N26 are all permanently connected to the outputs of the group encoder, each time a letter key is depressed every one of these gates will give an output as the counter cycles, irrespective of which letter key is depressed. The keyboard thus performs two functions. It activates the counter cycle and also selects the required letter from the relevant NOR-gate and routes it to the output of the typewriter to control the transmitter and also a small a.f. oscillator which provides an audible signal. The keyboard circuitry consists of 26 set-reset flip-flops (figure 4). It operates as follows. When the keyboard is active (not inhibited) output DD from figure 1 is low. Depressing key A (or any other key) will set the corresponding set-reset flip-flop. In the case of letter A this means that the output of N1 goes low, taking the reset input of figure 1 low and starting the counter cycle. It also takes the input of N3 low, allowing the signal from the output of N1 (figure 3) to be routed through N3 and the diode OR-gate connected to its output. Via N4 the signal controls a relay to switch the transmitter, and also

switches on and off the oscillator built around S2, to provide an audible signal. LED D2 provides a visual indication of the morse signal.

Since letter A has a duration of five clock pulses the counter and the keyboard flip-flop must be reset on the sixth clock pulse. This is accomplished very simply by taking the sixth output of the 74154 (AA) and feeding it into point AA in figure 4. Since different letters have different lengths the counter and keyboard must be reset at different points in the cycle. Letter B for example, occupies 9 clock pulses, so the counter is reset on the tenth pulse. The necessary reset inputs can all be found from table 1. While a letter is being transmitted output DD of figure 1 is, of course, high, so depressing a key will have no further effect. An interesting feature of the keyboard is that it is possible to transmit a continuous chain of letters by holding down a key, since immediately DD goes low on completion of a letter + letter space the flip-flop will again be set if the key is still held down. This also makes possible quick typing of repeated letters in words.

For the most efficient operation of the typewriter the frequency of the clock pulse generator (and hence the speed of sending) should be matched to one's typing ability, since, if the characters are sent too fast there will be long pauses while one finds the next letter, and if they are sent too slowly one will be attempting to type faster than the machine can send. The operator should, of course, also take account of the ability of the person on the receiving end, at any rate if he is taking down the message by hand!

Keyboard layout

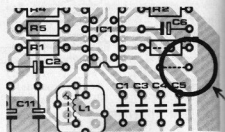
A layout for the keyboard is given in figure 5. This is based on a standard typewriter keyboard, but has no numerals or punctuation marks, though these may be added by extending the keyboard and the circuitry of figures 2 and 3. Suitable keyboard switches and complete keyboards are manufactured by firms such as C.P. Clare, Alma Components and Cherry, or it is often possible to obtain surplus, ex-computer keyboards relatively cheaply. ■

THE MISSING LINK

Modifications to
Additions to
Improvements on
Corrections in
Circuits published in *Elektor*

CA 3090 AQ stereo decoder

One link is missing on the layout of the p.c.b. for the CA3090AQ, as published in *Elektor* 5, p. 747, no. 88. The connection: C2 (negative end)/pin 13/pin 5/C6 (negative end)/wire links from pin 3 and pin 4 should be connected to ground.



Feedback PLL for FM

(*Elektor* 9, p. 110). An extra decoupling capacitor (C47) has been included on the p.c. board and component layout, but it was not included in the circuit diagrams or parts list. The value is 100 n, and it can be included in the circuit diagram in parallel with C7 (figure 7).


Capacity relay

In the component layout for this circuit (*Elektor* 9, p. 138), the connections to diode D1 are reversed. The cathode should be connected to the junction: C2/R3/R7/R2/T1 (drain); the anode is connected to ground. The circuit diagram is correct.

Apologies!

Owing to some problems with the computer which handles our subscriber administration, the printing of a large number of the address labels for *Elektor* 8 (December 1975) was held up for several weeks. We offer sincere apologies to those subscribers who were affected by this.

DIGITAL WRIST WATCH



With the introduction of new devices and the consequent competition the price of components for digital watches has fallen rapidly in recent months. Whereas a couple of years ago a digital watch was available only as a two-chip design costing around £ 40 for the two IC's, it is now possible to obtain a single IC that will perform all time-keeping functions, and will display date as well as time, for around £ 10. It is possible to construct a complete watch module (excluding case and strap) for under £ 25. Two watches are in fact described in this article. A low-cost, relatively easy to construct version, and a more miniature version for the advanced constructor.

It must be stressed at the outset that construction of a watch is a difficult project, which should not be attempted by the beginner as it involves the use of extremely miniature components and requires skillful soldering.

After considering the various watch IC's available the choice fell on the Intersil ICM72-- series. There are four IC's in this series, all of which are pin compatible, and which differ only in the type of display. They are:

ICM 7200, which displays hours, minutes, seconds, day and date with a 12-hour format.

ICM 7202, which displays hours, minutes, seconds and date with a 12-hour format.

ICM 7203, as 7200 but with 24-hour format.

ICM 7204, as 7202 but with 24-hour format.

These IC's are capable of driving LED-displays directly without the use of buffer transistors, and require little in the way of external components as will be seen later. Due to the high current consumption of LED displays the display is not illuminated continuously but must be activated when the time is to be read to avoid depleting the batteries too quickly. This may be thought to be a disadvantage, but in fact the system has considerable advantages over the more common liquid-crystal displays:

- can be seen in the dark.
- display is multiplexed therefore only 12 connections are needed to the display as opposed to 29 for an equivalent liquid-crystal display, thus making for simpler board layout.
- LED displays can be soldered direct into the circuit, whereas liquid-crystal displays require special (expensive) connectors.

A block diagram of the ICM72-series of IC's is given in figure 1. The oscillator frequency is determined by a 32.768 kHz crystal. The active components of the oscillator are contained on the chip and the only external component required apart from the crystal is a trimmer capacitor to fine tune the oscillator frequency.

The oscillator frequency is divided down to 1 Hz by a sixteen-stage binary divider. Some of the divider stage outputs are used to generate the multiplex drive waveforms for the display. The 1 Hz output is then used to drive seconds, minutes, hours, day (where applicable) and date counters. The outputs of these counters are multiplexed, decoded and fed to the display drivers. The control section implements time setting and display activate functions. There is also a light sensor input which may be used to adjust the display brightness to suit ambient lighting, but for reasons of simplicity it is not used in this design.

Basic version of the watch

It was felt that the basic version of the watch should be the cheapest and simplest to build, though not necessarily the most compact version. How-

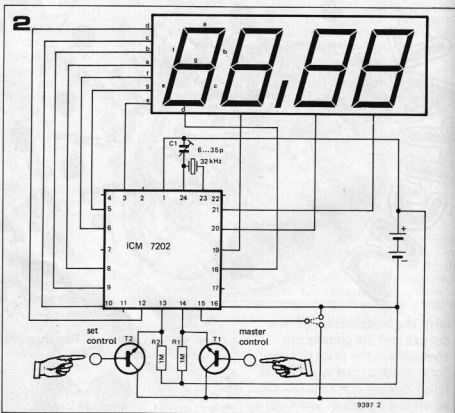
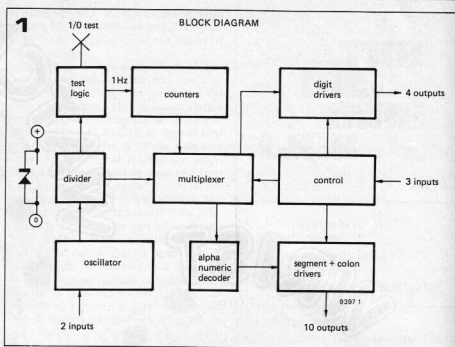


Figure 1. Block diagram of ICM 72-- series of watch IC's.

Figure 2. Circuit of basic version of watch.

Figure 3. Printed circuit board and component layout for figure 2.

ever, it will fit into a 30 mm internal diameter ($1\frac{1}{2}$ ligne watchmaker's measurement) case, with an internal depth from front to back of 8 mm.

The circuit diagram of the watch is given in figure 2. To keep costs down and to simplify construction it was decided to use a standard 4-digit multiplexed display in a DIL-package, rather than a special watch display, although one of these is used in the more advanced version. The DL34M, being a DIL-package, is much easier to solder than a watch display, and is also about half the price. There are, however, certain disadvantages:

- the display is more bulky, thus increasing the case size.

- the display is only seven-segment, so alphanumerics cannot be displayed. This limits the choice of IC's to the ICM 7202 and ICM 7204, which display the date but not the day.
- special watch displays have a colon between the hours and minutes digits. This has separate anode and cathode connections (i.e. it is not connected to the digits in any way) and the watch circuitry is designed so that the colon is off for A.M. and on for P.M. during timesetting. The DL34M does not have a colon; it does have a decimal point, but this is part of the normal multiplexed display. As this does not have an independent cathode connection it is not possible to use it to display A.M. and P.M.

Time setting and display demand

These functions are performed by the set control and master control inputs, and the exact procedures will be detailed later. Suffice it to say that these inputs are normally held at V_{SS} by R1 and R2, and to activate these inputs it is necessary to take them to V_{DD} (ground). In true Elektor tradition, this is accomplished by TAP's. T1 and T2 are normally turned off, but grounding the base of either of these transistors to the case by touching it will turn the transistor on. So that the set control is not activated accidentally it is suggested that it should be recessed in the side of the case where it can only be reached with a probe. The master control can be a raised button.

Construction

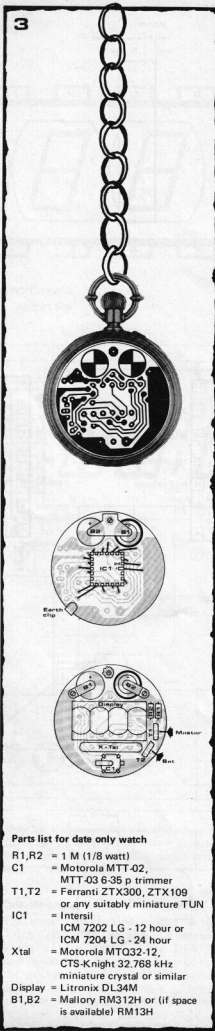
The printed circuit board and component layout of the watch are given in figure 3. Details of the IC pin configuration, package style, and dimensions of the battery clips are given in figure 4. Before construction commences it is essential to open out the battery holes to the correct diameter, and to file notches to accept the clips.

It is essential to ensure that the negative battery clip is recessed sufficiently far that the case (positive) of the battery cannot make contact with it, or the battery will be shorted out. This does not apply to the positive battery clip as this is in contact with the case of the battery anyway.

The bridge between the two batteries is held in position with a 12 B.A. nut and bolt. The nut is mounted on the display side of the board and is secured with a spot of epoxy adhesive. The top edge of the board between the batteries should be filed flat so that the flange on the bridge can overhang the edge of the board, thus preventing it from turning. It is essential that this bridge does not touch the case of the watch.

An earth clip is soldered to the edge of the board to ensure that battery positive (V_{DD}) is in contact with the watch case, so that the TAP's will operate reliably.

All components except the IC can now be mounted on the board. The crystal



Parts list for date only watch

- R1,R2 = 1 M (1/8 watt)
 C1 = Motorola MTT-02,
 MTT-03 6-35 p trimmer
 T1,T2 = Ferranti ZTX300, ZTX109
 or any suitable miniature TUN
 IC1 = Intersil
 ICM 7202 LG - 12 hour or
 ICM 7204 LG - 24 hour
 Xtal = Motorola MTQ32-12,
 CTS-Knight 32.768 kHz
 miniature crystal or similar
 Display = Litronix DL34M
 B1,B2 = Mallory RM312H or (if space
 is available) RM13H

should be mounted on a foam pad to provide shock resistance. As the IC is mounted on the back of the board it is essential to ensure that the component leads project the minimum distance through the board, to keep the module depth as small as possible. The IC is the final component to be mounted.

It is mounted upside down i.e. with the side bearing the type number facing the board. A thin piece of card should be glued to the back of the board to insulate the IC. The IC can then be held in place with a piece of modelling clay while the first wires are soldered into place, remembering to ensure correct orientation of the IC, i.e. pin 1 facing to the right of the board. Relatively thick wire should be used so that there is no tendency for the wires to sag and short out on the back of the board. When the IC is soldered into position the module is ready for testing.

Light sensor input

As mentioned earlier the light sensor option is not used for reasons of simplicity. It is, however, possible to select two brightness levels for the display. Connecting pin 15 to V_{DD} gives a maximum brightness display, while connection to V_{SS} gives a less bright display, thus increasing battery life. These options are shown dotted on the board layout.

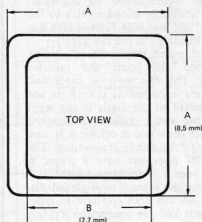
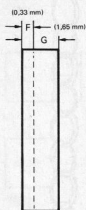
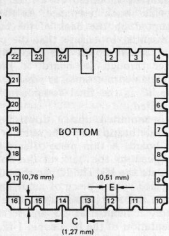
Assembly into case

As stated earlier the module will fit into a case 30 mm diameter by 8 mm deep. However, if a screwback case is used the dimensions must be slightly larger as otherwise the screwed rim of the back might make contact with the board. Before assembling the watch into the case the touch contacts must be fixed into place. For this two holes are required in the side of the case, one of which can be the existing winder hole. The master control contact can be made from a small brass tack or screw. The shank of this should be insulated with sleeving and the whole assembly fixed in the hole with epoxy adhesive. The shank can then be cut off so that about 1 mm projects outside the case. To avoid accidental activation the set control should be recessed. This can be accomplished by using a similar brass tack, but the shank must be cut short before insertion in the sleeving so that it does not project, and may only be reached with a (metallic) probe.

The edge of the board must have notches filed in it to clear the heads of the tacks. The touch contact wires can now be soldered to the heads of the tacks and the board may then be fitted into the case. If a three-piece case is used this procedure is much simpler. Since the watch should never require servicing the module can be secured into the case with a few spots of epoxy adhesive around the edge of the board.

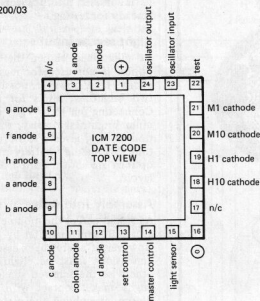
To enhance the display contrast, a filter made from red celluloid may be inserted behind the watch glass.

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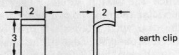
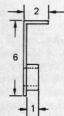
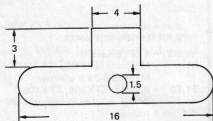
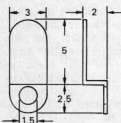
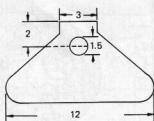
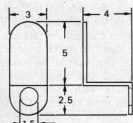
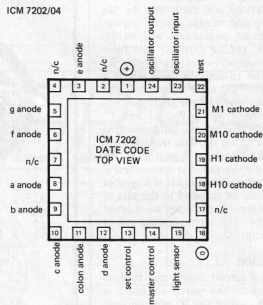


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CONNECTION DIAGRAM
ICM 7200/03

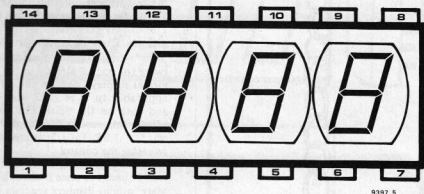


CONNECTION DIAGRAM
ICM 7202/04



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PIN	DL-34, DL-34M FUNCTION
1	NC
2	Anode E
3	Anode D
4	Anode C
5	D.P. Anode
6	Anode G
7	Cathode 4
8	NC
9	Anode B
10	Cathode 3
11	Anode F
12	Cathode 2
13	Anode A
14	Cathode 1

6

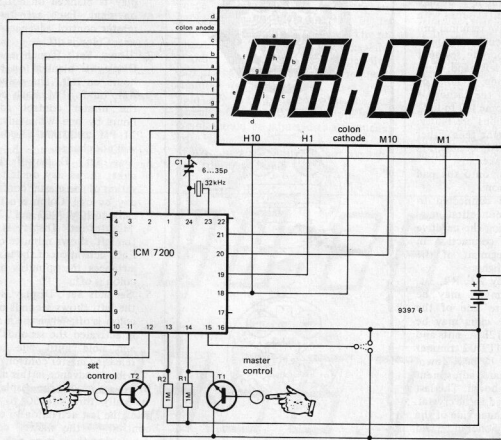


Figure 4. Package dimensions and pinouts of watch IC's, and details of battery clips.

Figure 5. Pinout of DL34M display.

Figure 6. Circuit of more sophisticated day/date watch.

Most of the above remarks also apply to the construction of the more sophisticated version of the watch, which is described next.

Construction - Day/Date watch

The more sophisticated version of the watch (figure 6) employs a special watch display, the Litronix DL5175 (see figure 8 for details). Because of this the module is thinner and the overall dimensions are smaller. This display has an alphanumeric capability in the two left-hand positions, and may thus be used with the ICM 7200 or 7203, which

have a day as well as date display (see figure 9). Of course, if day display is not required this version of the watch may be used with the ICM 7202 or 7204, with a consequent saving of some £ 5 on the IC cost.

Assembly should proceed as follows: the board must first be filed to fit the case and the battery holes must be opened up as for the other version of the watch. The first (and most difficult) component to mount is the display. The technique used is known as reflow soldering. The display pads on the board are first lightly tinned, ensuring that the thickness of solder is reasonably even on

all the pads. Next the solder bumps on the back of the display are cleaned by rubbing them lightly over a piece of very fine emery paper. The display may now be placed in position on the board and held there with a piece of modelling clay at either end. The pads along the top edge of the display may now be heated up with a soldering iron, melting the solder and thus making the joint. A magnifying glass is a useful aid during this procedure. If any joints appear not to have made a small additional quantity of solder may be run onto the pad, taking extreme care not to form bridges between tracks. The joints along the top edge of the display having been made, the modelling clay may be removed and the procedure repeated for the end pads.

Before proceeding further it is essential to test the display to ensure that all the joints are good. Using a 9 V battery in series with a 2k2 resistor (or a 4.5 volt battery in series with a 1 k) proceed as follows: connect the negative terminal of the battery to the 'cathode 1' display pad. Connect a test prod (in series with the resistor) to the positive terminal and touch each of the segment anode pads in turn, when the appropriate segment should light up on the left-hand digit. Test also the colon anode. If none of the segments lights then the cathode 1 connection is faulty. If some fail to light then the anode connections are faulty. If the colon does not light then either the colon anode or cathode connection may be at fault. Remake any faulty joints by running solder onto the pad whilst heating with the iron.

With the positive prod connected to anode 'a' the cathode connections may now be tested by touching the negative prod to each cathode connection in turn, when the 'a' segment of the appropriate digit should light.

Having tested the display R1, R2, T1, T2, IC1 and the trimmer may be mounted on the reverse side of the board, and the battery clips may be fitted and secured with 12B.A. nuts and bolts. Note that if the MTT 02 trimmer is used the leads should be bent downwards so that the square adjustment hole faces out from the board. The last component to be mounted is the crystal. This is mounted on the same side of the board as the display, and should be laid on a thin layer of silicone rubber, which will perform three functions:

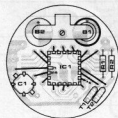
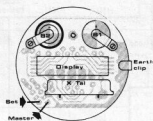
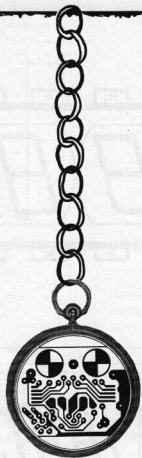
1. securing the crystal to the board.
2. providing a resilient, shock-resistant mounting.
3. insulating the crystal can from the copper tracks.

Leadout wires should then be soldered to the bases of T1 and T2, after which the watch module is ready for testing.

Use and adjustment

Activation of the Master and Set controls is accomplished by grounding the base of T1 or T2 to V_{DD} . When the watch is in normal use V_{DD} is connected to case, and hence to the wearer's body, so touching the appropriate contact

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Parts list for day/date watch.

- R1, R2 = 1 M (1/8 watt)
 C1 = Motorola MTT-02
 MTT-04 6.35 p trimmer
 T1, T2 = 2N4286, 2N3794 or any suitably miniature TUN
 IC1 = Intersil
 ICM 7200 LG - 12hour or
 ICM 7203 LG - 24hour
 Xtal = Motorola MTQ32-12,
 CTS-Knight 32.768 kHz
 miniature crystal or similar
 Display = Litronix DL5175
 B1, B2 = Mallory RM312H or (if space is available) RM13H

with a finger will activate the required function.

The master control operates as follows:

1. 'Time': touch once and time is displayed, hours on the left, colon in the middle and minutes on the right. The colon is always on in this mode. The display stays on for 1.25 to 1.5 seconds after the control is released.
2. 'Date': touching the master control twice (or once if already in the 'time' mode) displays day on the left (not applicable to ICM 7202 and 7204) and date on the right. The colon is off in this mode. The display stays on for 1.25 to 1.5 seconds after releasing the control.
3. 'Seconds': touching the master control 3 times (or once if already in the 'date' mode) displays seconds on the right. The colon is off in this mode and the display stays on for 50 to 60 seconds after releasing the control.

The set control operates as follows:

1. 'Date Set': Touch control once. Display is blanked on left, shows date on right. Each activation of the master control advances the date by one. Colon is off.
2. 'Hours Set': Touch control twice. Display is blanked on right, shows hours on left. The colon is off for AM, on for PM. Each activation of the master control advances the hours by one. When advancing from 11 PM to 12 AM the day and date will not change.
3. 'Day Set': Display is blanked on right, shows day on left. Each activation of the master control advances day by one. Colon is off. Not applicable to ICM 7202 and 7204.
4. 'Minutes set': Display is blanked on the left, shows minutes on the right. Each activation of the master control advances the minutes by one. The colon is off.
5. 'Seconds Set': Display is blanked on the left, shows seconds on right. The colon is off. When the master control is activated the seconds reset to 00 and hold until one second after releasing master control. The minutes will not advance in this mode.

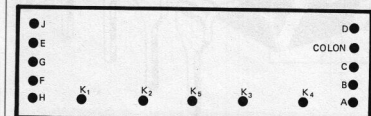
In all set modes the display will automatically turn off 50 to 60 seconds after the last activation of either the set control or the master control. This means that there is no risk of depleting the batteries, and the watch automatically returns to its normally time-keeping mode even if all the setting operations have not been carried out. Alternatively the user can cycle through all the set modes, and on the sixth activation of the set control the display will extinguish and the watch is in the normal timekeeping mode.

When setting the watch after battery replacement the manufacturers advise the following sequence:

1. touch set control once, advance to correct date.
 2. touch set control once, advance to correct hour.
- Colon is off for AM, on for PM.

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DL-5175



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- touch set control once, advance to correct day.
- touch set control once, advance to the next minute.
- touch set control once, activate master control and hold until time signal is heard for next minute, then release master control.
- touch set control once.

Timekeeping adjustment

This is carried out using the trimmer capacitor. A trimming tool is required

and this may be made by filing a small piece of brass rod to a square end cross-section of 0.76 mm, to fit the adjustment hole in the trimmer. The rod should then be mounted in an insulated handle, so that hand capacitance does not affect the frequency. If a frequency counter is available the test point (pin 22) may be used with the test circuit of figure 10. The output at this point should be adjusted to a frequency of 1 Hz.

If a frequency counter is not available the trimmer should initially be set to

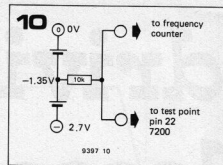


Figure 7. Printed circuit board and component layout for figure 6.

Figure 8. Pinout of DL5175 display.

Figure 9. Alphanumeric display font of DL5175 display.

Figure 10. Test circuit for frequency adjustment.

maximum capacitance. This occurs when the semicircular vane of the trimmer (visible between the two plates) is in the half of the trimmer opposite the brass contact finger that makes connection to the vane. The watch will now run slow, and turning the trimmer in either direction will make it run faster. This adjustment can be carried out over a period of time, always remembering which direction the trimmer was last turned, and what the result was. It should be possible to obtain a final accuracy of a few seconds a month.

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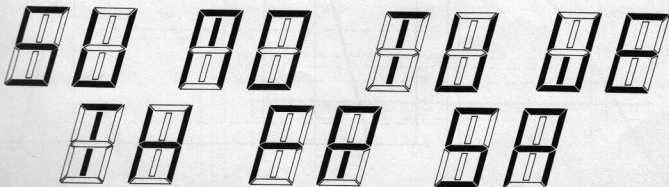
DISPLAY FRONT



NUMBERS

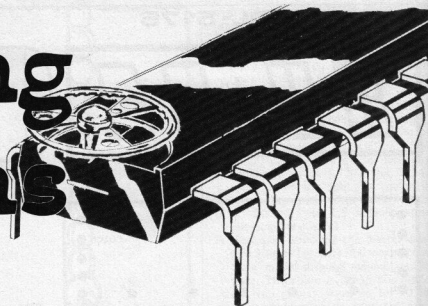


LETTERS



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driving lessons



A title that needs some further explanation. When transistor-transistor or CMOS logic circuits are driven from 50 Hz mains pulses, unsatisfactory behaviour can be expected since the exact pulse shape requirements for proper functioning of the gates cannot, usually, be met by pulses derived straight from the sinusoidal mains.

This article discusses those requirements and, taking standard TTL devices as an example, establishes a few basic principles in connection with digital logic driving pulses.

Input and Output Pulse Shapes Definitions

The typical pulse shape in figure 1 shows the rise time t_r (defined as the time the driving pulse requires to rise from 10% to 90% of its maximum level). Likewise, the fall time t_f is defined as the time in which the signal drops from 90% to 10% of its maximum level.

Close adherence to t_r and t_f specifications is important when gates without switching hysteresis are driven; slow risetime pulses can cause spurious oscillations when the incoming pulse level coincides with the gate threshold level.

A further important characteristic shown in the figure is the pulse width t_w , defined as the duration of the pulse between the two points of 50% maximum pulse level. For satisfactory performance of the logic device, t_w must not be less than a specified value as shorter pulses will result in erratic output signals or complete loss of signal.

TTL Gate Input Specifications

Figure 2 shows the specified t_r , t_f and t_w values as they apply to standard TTL gates. Logic "0" level is specified to be not more than 0.8 V, which level is defined as the 0% level. Logic "1" level is specified to be not less than 2 V, defined as the 100% level.

The input t_r and t_f values apply between these two limits and are, therefore, measured between the 10% and 90% levels, that is to say, 0.92 V and 1.88 V respectively.

With these TTL gates the t_w duration is measured at the 50% signal level according to the above definition. In practice this switching level is situated at 1.5 V.

Input Signal Requirements

These TTL requirements are closely specified.

The safe maximum positive input signal level is 5.5 V. The safe negative level is -1.5 V. Rise and fall times must be less

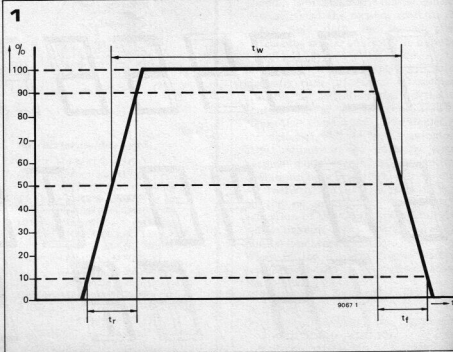


Figure 1. Defining the pulse width t_w , rise time t_r and fall time t_f .

Figure 2. Showing a pulse diagram with a well defined pulse width, rise time and fall time. The voltages indicated apply to standard TTL equipment only.

Figure 3. This circuit might be used for deriving 50 Hz driving pulses from 50 Hz AC mains but is not suitable since t_r and t_f are incompatible with standard TTL integrated circuitry.

Figure 4. Showing the rectified AC appearing across the zener diode of figure 3.

than 1 microsecond.

Even with these t_r and t_f figures, a separate specification is required for the edge steepness at the turn-on and turn-off switching points, since the edge slope may not be constant over its entire sweep. Thus, the figure of 0.5 microsec/V is specified for the points in question.

In order to obtain a well defined output signal, the TTL driving input pulse width must be at least 29 nanosec.

Numerical Examples

These examples illustrate the practical problems to be dealt with in the design of mains driven TTL equipment.

In figure 3, zener diode D clips the drive signal to prevent it from surpassing the safe positive level. When forward biased the diode limits the negative signal to -0.7 V.

In this example we will now consider if such a diode-resistor network will perform satisfactorily.

Figure 4 shows the rectified sinusoidal voltage. In this graph, t_r and t_f must be found between the 10% and 90% points of the potential difference between the logic "0" and "1" levels, i.e. 0.92 and 1.88 V respectively.

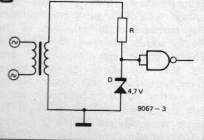
Figure 4 shows that

$$t_r = t_f = t_3 - t_1 \quad (1)$$

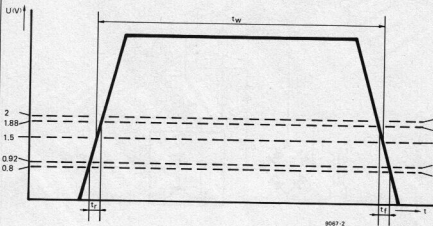
Points t_1 and t_3 are evaluated by the equation

$$v_t = \sin \omega t \times \hat{v} \quad (2)$$

3



2



which, for $t = t_1$, gives

$$v_{t_1} = \sin \omega t_1 \times \hat{v} \quad (3)$$

It is assumed that a 5 V rms mains transformer is used to power the TTL equipment, this being about the lowest voltage possible for obtaining a sufficiently stabilised 5 V DC supply. \hat{v} will then be 7.07 volts. Equation (3) can now be evaluated as follows:

$$0.92 \text{ V} = \sin(2\pi \cdot 50 \cdot t_1) \times 7.07 \text{ V} \quad (4)$$

which gives

$$t_1 = 0.42 \text{ millisecc.} \quad (5)$$

Point t_3 is found by evaluation of

$$v_{t_3} = \sin \omega t_3 \times \hat{v}$$

$$1.88 \text{ V} = \sin(2\pi \cdot 50 \cdot t_3) \times 7.07 \text{ V} \quad (6)$$

from which follows

$$t_3 = 0.86 \text{ millisecc.} \quad (7)$$

Equations (5) and (7) give the rise and fall times

$$t_r = t_f = (0.86 - 0.42) \text{ millisecc} = 0.44 \text{ millisecc.}$$

This numerical example proves that the signal across the zener diode of figure 3 shows rise and fall times greatly exceeding those specified for driving TTL circuitry and is, therefore, quite unsuitable.

The edge slope at the switching points can be evaluated by differential calculus.

We will thus consider if the specification of 0.5 microsec/V can be held.

The turn-on threshold level of 1.5 V (see figure 2) is reached at the point

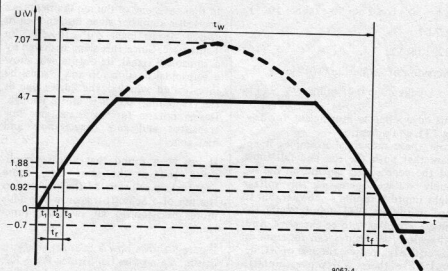
$$v_{t_2} = \sin \omega t_2 \times \hat{v}$$

$$1.5 \text{ V} = \sin(2\pi \cdot 50 \cdot t_2) \times 7.07 \text{ V} \quad (8)$$

from which follows:

$$t_2 = 0.68 \text{ millisecc.} \quad (9)$$

4



5

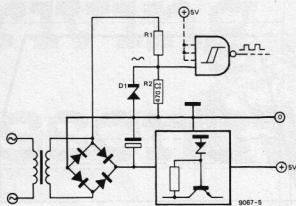


Figure 5. Showing how a Schmitt trigger can be driven by rectified AC via a potential divider.

6

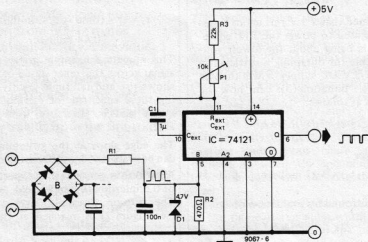


Figure 6. Minimising the effect of mains borne interference by including a monostable to follow the Schmitt trigger.

The edge slope at this point is found by differentiation of

$$v = \sin \omega t_3 \times \hat{v}$$

$$\frac{dv}{dt} = \omega \cos \omega t \times \hat{v}, \text{ evaluated:}$$

$$= 2\pi \cdot 50 \cdot \cos(2\pi \cdot 50 \cdot 0.68 \cdot 10^{-3}) \times 7.07$$

$$= 2221.09 \text{ V/s} \quad (10)$$

Inversion of equation (10) gives the edge slope 0.45 millisecc/V (11)

This edge slope is insufficient for driving TTL equipment.

From these numerical examples it appears that both the rise and fall times and the edge slopes depend on the AC supply voltage. Increasing this voltage might improve results somewhat, but to cope with the TTL requirements the voltage would have to be excessive. And, although cosmos gates can function on slower driving pulses, the use of AC derived drive there will prove impracticable too.

The one requirement that is fully met by AC derived drive is the pulse width

of 29 nanosec. This means that the circuit of figure 3 could be used if a way were found in which the leading and trailing edges could be steepened. This can be performed by amplification of the sine signal, which multiplies the slope by the amplifier gain.

In that case, one of the requirements is a transistor amplifier stage fast enough to switch from logic "0" to "1" in 1 microsec. Since this stage is driven by a sinusoidal signal, its output will show a sinusoidal portion too and it must be investigated whether the edge slope at the switching point is steep enough. Design criteria for this stage are: low transistor and gate capacitances and high gain.

It has been found that a less complicated and, at the same time, more economical solution of the problem is the use of a Schmitt trigger, which adds more precision to all switching functions.

Figure 5 shows how a Schmitt trigger is driven, via a potential divider R1 + R2, by a signal derived from a rectified sinusoidal voltage. In TTL circuits R2 must not exceed 470 ohms, in cosmos

applications it can be as high as 10 megohms. R1 must be high enough to keep the voltage across R2 below the trigger power supply voltage, which is 5 V for TTL, somewhere between 3 and 15 V for "A" range cosmos, and between 3 and 18 V for "B" range cosmos applications.

The resistance of R1 can be evaluated by the equation

$$R_1 = \frac{R_2 \cdot \hat{v} - V_B \cdot R_2}{V_B}$$

in which V_B stands for the DC power supply voltage. It will be safe practice to have a zener diode in parallel with R2 to clip high input levels. The diode voltage must approximately equal the power supply voltage. Excessive input levels can also be prevented by connecting the R1/R2 junction to the DC power supply via a germanium diode (cathode to +). In both cases the R1 resistance can be reduced by some 20%, which stabilises the drive voltage despite mains voltage fluctuations.

Since it cannot be expected that the power supply is free from mains borne interference, which may upset reliable functioning of the logic, suitable measures must be taken. Very effective suppression is obtained by the insertion of a pre-set monostable to follow the Schmitt trigger. The pre-set monostable interval must be slightly under the AC mains period of 20 millisecc; in this way, after the monostable has been triggered, it will be impervious to external interference. For the best effect, the monostable must be pre-set in a way that its interval is only just under the AC supply period.

Figure 6 shows how this has been realised with TTL integrated circuits. The monostable in question is the 74121, which possesses an additional Schmitt trigger input pin (5). P1 pre-sets the monostable to just below 20 millisecc; this is best carried out by first setting P1 to its maximum value, then slowly reducing it until a 50 Hz square wave appears at the Q output.

DIGITAL MASTER OSCILLATOR

Following last month's discussion of methods of producing the top octave of an electronic organ (or other keyboard instrument) using a single master oscillator, two practical designs for such an oscillator are presented this month. One is based on a commercially available master oscillator IC, and the other is designed around standard logic IC's.

A digital master oscillator based on the principle of frequency synthesis by the addition of partial frequencies is complex and fairly expensive, as a glance at the board layout of figure 14 will show! However, the method does have the advantage of good accuracy compared with the single IC version which will also be described. To help retain the overall picture while describing the various sections of the circuit, the block diagram arrived at in last month's discussion is reproduced in figure 1.

The Oscillators

The master oscillator circuit uses three oscillators. A clock generator, which drives all the divider circuits, plus vibrato and tremolo oscillators. Since all the notes are produced from the clock generator, this must be very stable. LC tuned oscillators are very

common in organs because of their stability. However, coils must be wound for such oscillators and it was found in the Elektor laboratories that comparable stability could be achieved using RC tuned oscillators based on TTL logic IC's. The final circuit arrived at (figure 2) uses two cross-coupled monostables, with the Q output of the other monostable, and hence the frequency of the oscillator, is determined by the time constants of the monostables, C2, R1, R2, R3 and P1. Since the circuit is symmetrical the frequency ratio of the waveform is 1:1. The frequency of the clock generator can be adjusted over a wide range



by using a 1 k pot. with a 470 Ω series resistor in place of R3, which means that the organ can transpose into any key, or may be tuned for playing with other instruments, simply by adjusting the pot. If this facility is not required R3 may be retained and P1 used to fine tune the oscillator.

The oscillator is provided with three 'effects' inputs, A, B, and C. If, for example, a slowly varying D.C. level is applied to point A a glissando effect is produced. This means that the pitch changes slowly, and the effect is similar to the sound of a Hawaiian guitar. Input B is a low frequency vibrato input. If a low level, low frequency (say 0.8 Hz) signal is applied to input B the clock frequency is modulated and the effect is similar to a conventional pipe organ. It is important that the control signal amplitude is not too high as the effect will then develop into an objectionable rise and fall in pitch.

Input C is the normal vibrato input. An RC phase-shift oscillator (figure 3) is used to provide the vibrato control signal. Its frequency, and hence the vibrato rate, can be adjusted with P3 from about 4 to 7 Hz. Its amplitude, and hence the pitch deviation, can be adjusted with P2. If the value of P3 is increased the vibrato frequency may be reduced still further, but it may then be necessary to increase the value of C10 to 1000 μ or even more so that there is then sufficient gain around T2 for the oscillator to function at such low frequencies.

Octave Tremolo

The so-called 'octave tremolo' effect mentioned last month can be achieved very simply in the case of a digital master oscillator. 'Tremolo' in this case is a misnomer, as a true tremolo involves amplitude modulation, but the term is in common use. The effect is obtained by switching a flip-flop in and out of circuit between the clock generator and the dividers, so that the pitch of the whole organ jumps up and down by an octave. Figure 5 shows a simple method of switching the octave tremolo flip-flop. If point A is at logic '1' then T1 is turned on and the input signal B bypasses the flip-flop via T1 and D1 to appear at C. If A is at logic '0' T1 is turned off and T2 is turned on. The frequency of input B is divided by 2 in the flip-flop and the signal is taken from the Q output to C via T2.

The control signal for the octave tremolo may be derived from a simple multi-vibrator based on a TTL Schmitt trigger, as shown in figure 4. P4 allows the tremolo rate to be adjusted from about 3 to 6 Hz.

Frequency Synthesis

As discussed in last month's article, the twelve notes in the octave are obtained by the addition of partial frequencies. Thus, for example, if a 1 kHz pulse train were mixed with a 500 Hz pulse train then the resulting frequency would be 1.5 kHz, subject to the proviso that none

of the pulses coincide, as they would then be indistinguishable from one another.

The partial frequencies are obtained by dividing down from the clock frequency in a series of flip flops (block A in figure 1). Each frequency in the octave can then be expressed in terms of its partial frequencies as a binary number (table 1) so that where a '1' appears in table 1 a contribution is required from the corresponding partial frequency. To synthesise a particular frequency it is necessary to OR together all the relevant partial frequencies.

To ensure that no pulses coincide the symmetrical output waveforms of the flip-flops in block A must be modified into shorter pulses. This is achieved by ANDing the lower frequency outputs with the complements of the higher frequencies, as shown in figure 6. This is the function of block B in figure 1.

A cheap method of achieving the multiple-input OR function required to add the pulse trains is the use of open-collector inverters, with a 'wired-OR' function performed at their outputs (figure 7).

As explained in last month's article the frequency synthesis takes place at frequencies several octaves above the actual frequencies of the notes in the top octave of the instrument. Once the correct frequency ratios have been obtained by synthesis each note thus obtained must be divided down through several flip-flops to remove the inevitable jitter which arises during synthesis. The outputs of the anti-jitter stages are the actual notes of the top octave. This is the function performed by block D in figure 1.

The complete circuit of the master oscillator is given in figures 8a and 8b. In the top left-hand corner is the clock generator, next to it the vibrato oscillator, and below that the octave tremolo oscillator. The flip-flops used for octave tremolo and generation of the partial frequencies are actually contained in three 7493 4-bit binary counters. The outputs of the 7493's are inverted to obtain the complements, then fed into the AND gating, at the outputs of which appear the modified duty-cycle pulse trains ready for ORing together.

The 11 partial frequency bus lines on the right of figure 8a are connected to the corresponding points on the left of figure 8b. The required partial frequencies for each note are picked off these and fed into the inverters in the middle of the diagram. The wired-OR outputs are then fed into the anti-jitter stages, consisting of two cascaded 7493's for each note, at the outputs of which appear 11 of the notes of the top octave. As explained last month, note C does not require synthesis but is simply divided down from the clock frequency and appears at the output of the 2^{-7} partial frequency divider.

MOS version

The advantage offered by the above system is extremely good accuracy of the

Table 1

	2 ¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰
c ⁵	1	0	0	0	0	0	0	0	0	0	0	0
b [#]	1	1	1	0	0	0	1	1	0	1	0	0
a [#]	1	1	1	0	0	1	0	0	0	0	1	0
a [#]	1	1	0	1	0	1	1	0	1	0	1	0
g [#]	1	1	0	0	1	0	1	1	0	1	0	0
f [#]	1	0	1	1	1	1	1	1	1	1	0	0
e [#]	1	0	1	0	1	0	1	0	1	0	0	0
d [#]	1	0	0	1	1	1	1	1	1	0	1	0
c [#]	1	0	0	0	1	1	1	1	1	0	1	0
c	1	0	0	0	0	0	0	0	0	0	0	0

Table 1. The frequencies of the notes in the octave expressed as binary numbers compared to the lowest note (C⁵ = 1.000000000).

Figure 1. Block diagram of a master oscillator using the principle of frequency synthesis, which was arrived at during last month's discussion.

Figure 2. Clock generator using a 74123 dual monostable, which is used in both versions of the master oscillator. The frequency is variable over a wide range by means of a potentiometer, which means that transposing facilities may be built into the instrument. Voltage control may also be applied to the three inputs for various effects.

Figure 3. An RC phase-shift vibrato oscillator. The vibrato rate may be varied by means of P3, and the amplitude by means of P2.

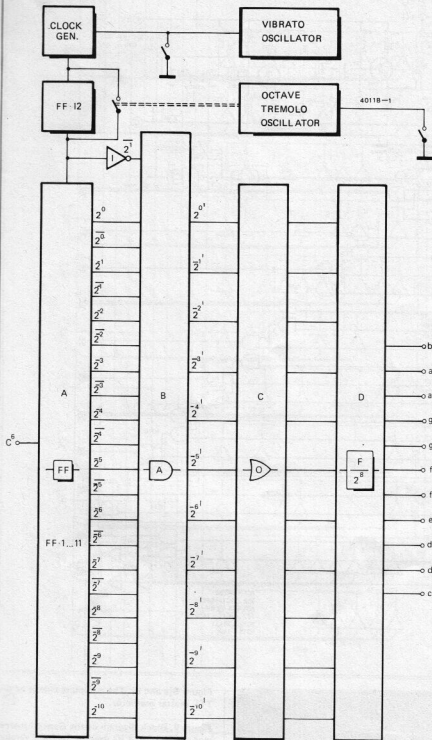
Figure 4. TTL Schmitt trigger astable multi-vibrator for octave tremolo switching.

Figure 5. The octave tremolo flip-flop and associated switching.

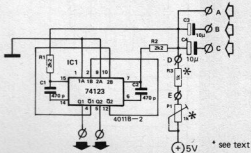
Figure 6. Modifying the duty-cycle of the partial frequencies ensures that no pulses coincide.

Figure 7. The partial frequencies are added, using open-collector inverters with a wired-OR function at their outputs.

1

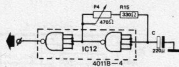


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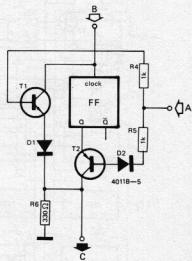


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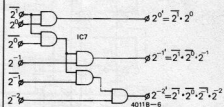
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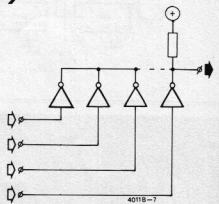
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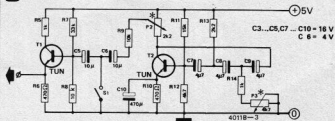
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7



3



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8a

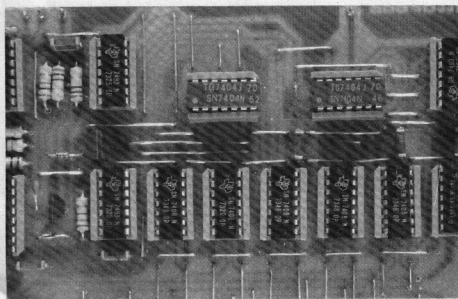
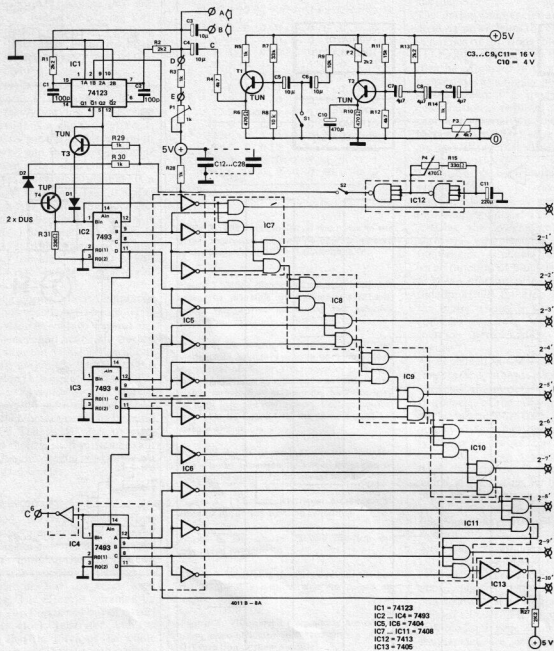


Figure 8(a and b). The complete circuit of the TTL master oscillator.

Figure 9. Block diagram of the General Instruments AY-10212 IC used in the MOS version of the master oscillator.

Figure 10. The odd-numbered division ratios in the IC produce asymmetric output waveforms.

8b

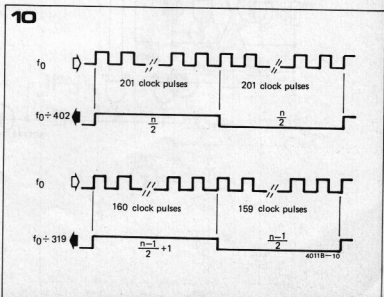
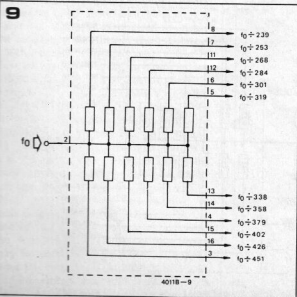
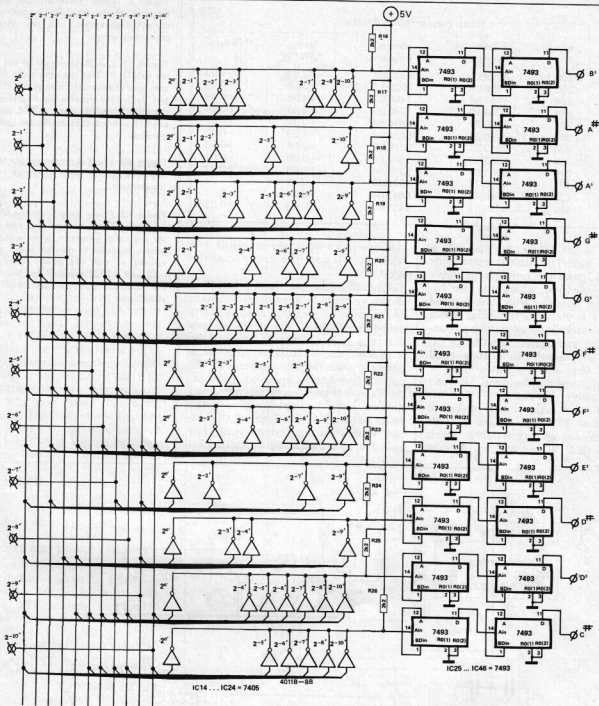


Table 2. Input frequency 2000240 Hz

note	divider	output frequency	correct frequency	error (Hz)	% error
c ⁶	239	8369.21	8372.02	-2.80	-0.03
b ⁵ #	253	7906.09	7902.13	+3.96	+0.05
a ⁴ #	268	7463.58	7458.62	+4.96	+0.07
a ⁵ #	284	7043.10	7040.00	+3.10	+0.04
g ⁴ #	301	6645.32	6644.88	+0.44	+0.01
f ⁴ #	319	6270.34	6271.93	-1.59	-0.03
f ⁵ #	338	5917.87	5919.91	-2.04	-0.03
e ⁵	358	5587.26	5587.65	-0.39	-0.01
e ⁴ #	379	5277.68	5274.04	+3.64	+0.07
d ⁴ #	402	4975.72	4978.03	-2.31	-0.05
d ⁵ #	426	4695.40	4698.64	-3.24	-0.07
c ⁵ #	451	4435.12	4434.92	+0.20	+0.01

intervals in the octave, but the cost is relatively high. The General Instruments AY-1-0212 uses the principle of direct frequency division, which was also discussed last month. With this method each note is individually divided down from the clock frequency, using a counter of the appropriate length. As explained last month, to achieve good accuracy large division ratios must be employed, typically between 500 and 1000. However, in the AY-1-0212 the largest division ratio is only 451, and the smallest 239. This means that the maximum relative error is 0.07%, which occurs with D, E and A sharp. Against

this one must weigh the simplicity and relatively low cost of a circuit using the AY-1-0212.

The block diagram of the AY-1-0212 is shown in figure 9, but further discussion of the mode of operation of the dividers cannot be made, as the manufacturer's literature gives no internal circuit of the IC. Table 2 shows the output frequencies obtained with the IC, compared to the correct frequencies, and also the error, both absolute and percentage. Since odd division ratios are used for some of the notes in the AY-1-0212 not all the output waveforms are symmetrical. For example, as shown in figure 10 the out-

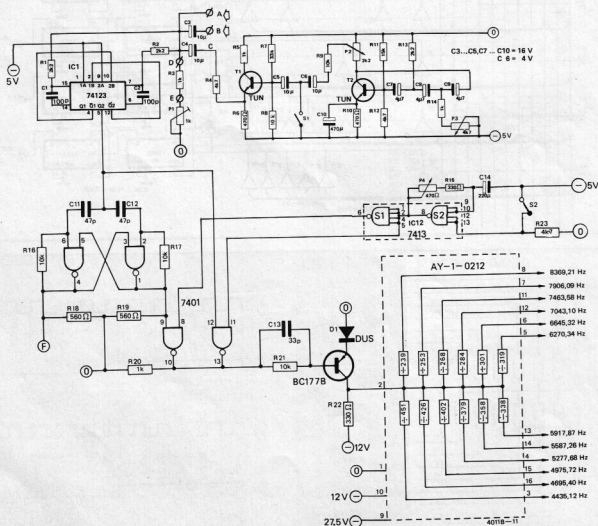
Table 2. Table showing the output frequencies of the AY-1-0212 compared to the correct frequencies, and the absolute and percentage error.

Figure 11. Complete circuit of the MOS master oscillator. This uses the same clock generator and vibrato oscillator as the TTL version, but the octave tremolo flip-flop and switching are different as there are no TTL dividers with spare flip-flops that could be used for this purpose.

Figure 12. 5 V 2 A power supply for the TTL master oscillator with extensive interference suppression.

Figure 13. Power supply for the MOS master oscillator. Three voltages are required. -5 V for the clock generator, vibrato oscillator and octave tremolo is derived using a modified version of the TTL power supply, and the -12 and -27 V supplies for the AY-1-0212 are obtained using simple, single transistor stabilisers.

11



put of the divide-by-402 stage is symmetrical, as the output waveform is high for 201 clock pulses and low for 201. In the case of the divide-by-319 stage, however, the output is high for 160 clock pulses and low for 159. This will, of course, only affect the top octave as the lower octaves of the instrument will be obtained by dividing down using flip-flops, when the asymmetry will disappear.

The AY-1-0212 is available in a 16-pin dual-in-line package in two versions, plastic and ceramic. All inputs of the IC are protected against overvoltage and static charges by zener diodes. The impedance of the outputs is 3k Ω .

The complete circuit of an oscillator using the AY-1-0212 is given in figure 11. The ancillary circuits are identical to those of the synthesiser version, with the exception of the octave tremolo flip-flop and switching, there being no spare flip-flop available since 7493 input dividers are not used. Instead the flip-flop and switching are built around a 7401 IC. Since the voltage levels within the AY-1-0212 are all negative, for simplicity of power supply design the TTL sections of the circuit are operated from a +0, -5 V supply rather than a +5, -0 V supply. This also means that the TTL logic levels (which swing between about -0.6 and -4.5 V) can be translated into the 0 to -10 V swing required to drive the AY-1-0212 using a single BC177B transistor.

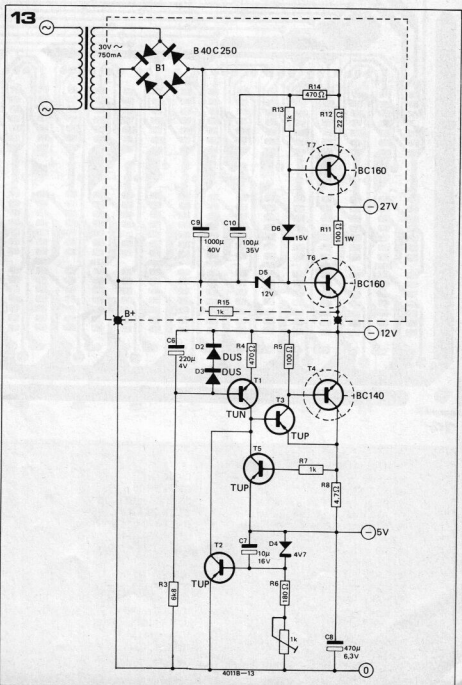
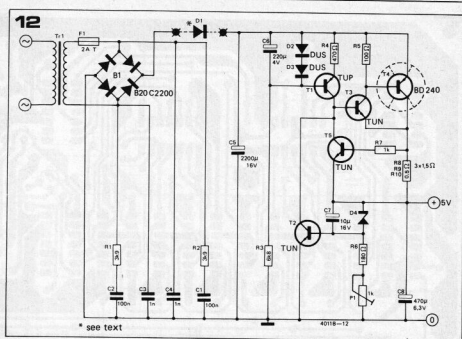
Like the synthesiser version the clock generator of the AY-1-0212 version has 'effects' inputs, as described earlier.

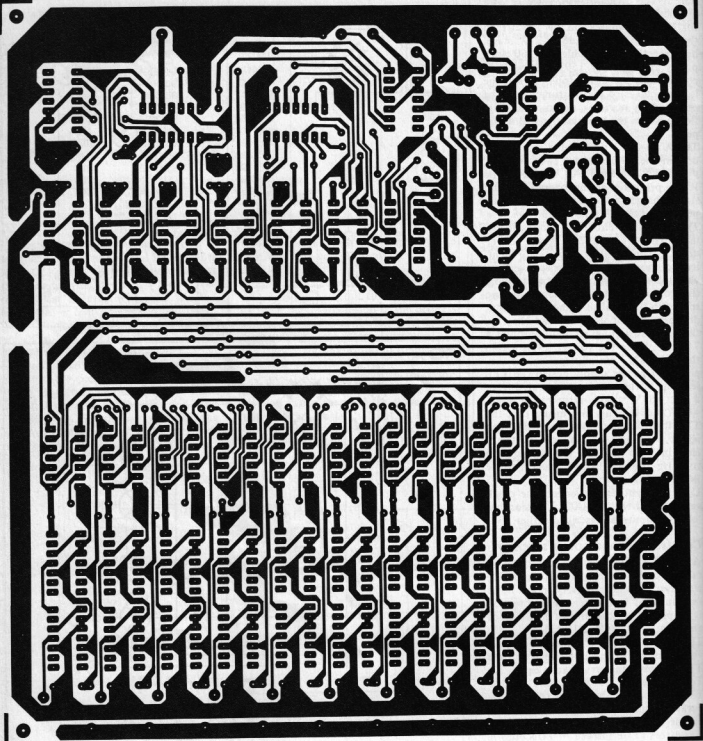
Construction and power supplies

A 5 V 2 A power supply for the TTL master oscillator is given in figure 12. Because of the relatively poor noise immunity of TTL extensive suppression is employed on the unregulated side of the circuit (C1 - C4, R1, R2).

The power supply for the AY-1-0212 version of the circuit is derived from the TTL power supply as shown in figure 13. To provide the -5 V required for the TTL sections of the circuit (oscillators, octave tremolo flip-flop etc) the same circuit is used but with different polarity transistors (TUP instead of TUN etc). A stable -5 V supply is required to ensure the frequency stability of the oscillators which operate from this supply, but in this case the current drawn is only about 100 mA, as against the 2 A of the TTL version. The -12 V and -27 V supplies required by the AY-1-0212 do not need to be so well regulated, and are simply supplied from T6 and T7, with D5 and D6 providing the reference voltages.

A p.c. board layout for the TTL master oscillator is given in figure 14, and that for the MOS version in figure 15. The clock generators must be screened in each case to avoid r.f. radiation. In the case of the TTL circuit the area around the top left-hand corner of the board may be screened with pieces of copper laminate board, or indeed the whole printed circuit may be mounted in a metal box. The p.c. board for the MOS





14

Parts list for figures 8 and 14

Resistors:

R1, R2, R13, R16 to R27 = 2k2
 R3, R5, R14, R28, R29, R30 = 1 k
 R4, R12 = 4k7
 R6, R10 = 470 Ω
 R7 = 33 k
 R8, R9 = 10 k
 R11 = 15 k
 R15, R31 = 330 Ω
 P1 = 1 k, multiturn preset
 P2 = 4k7, lin.
 P3 = 4k7, lin.
 P4 = 470 Ω , lin.

Semiconductors:

T1, T2, T3 = TUN
 T4 = TUP
 D1, D2 = DUS

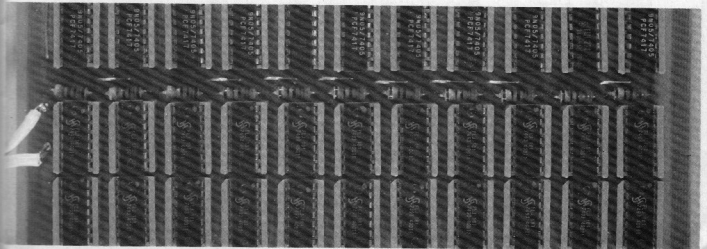
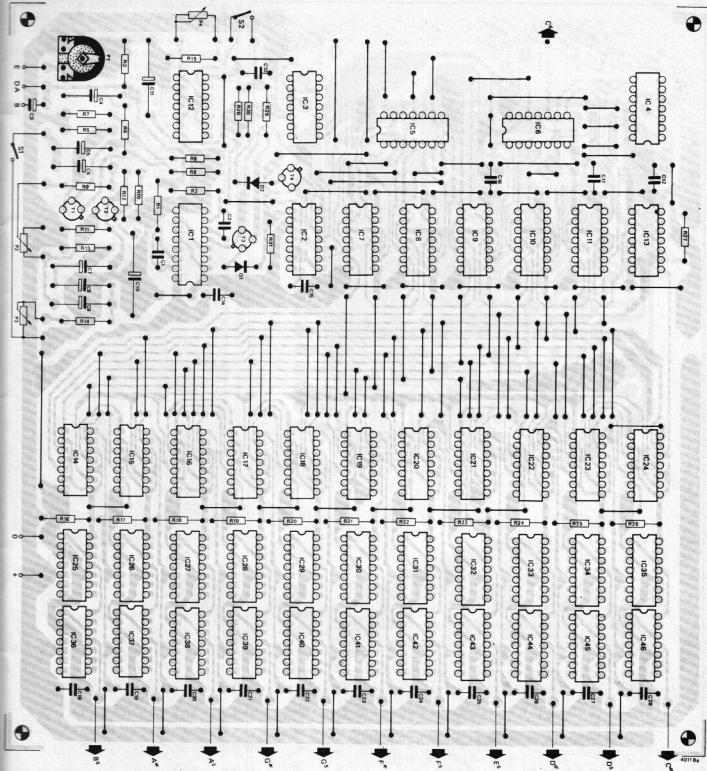
Capacitors:

C1, C2 = 100 p
 C3 to C6 = 10 μ , 16 V
 C7, C8, C9 = 4.7 μ , 16 V
 C10 = 470 μ , 4 V
 C11 = 220 μ , 16 V
 C12 to C28 = 100 n

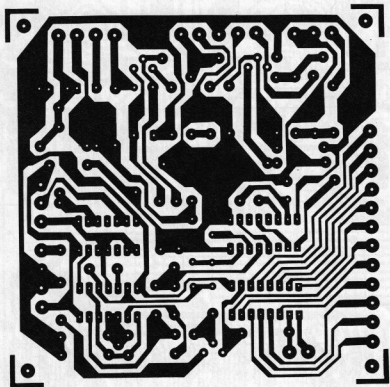
IC's:

IC1 = 74123
 IC2 ... IC4, IC25 ... IC46 = 7493
 IC5, IC6 = 7404
 IC7 ... IC11 = 7408
 IC12 = 7413
 IC13 ... IC24 = 7405

Figure 14. P.c. board layout for the TTL master oscillator.



15



Parts list for figures 11 and 15

Resistors:

R1, R2, R13 = 2k2
 R3, R5, R14, R20 = 1 k
 R6, R10 = 470 Ω
 R7 = 33 k
 R8, R9 = 10 k
 R11 = 15 k
 R12, R23 = 4k7
 R15, R22 = 330 Ω
 R16, R17, R21 = 10 k
 R18, R19 = 560 Ω
 P1 = 1 k, multiturn preset
 P2 = 4k7, lin.
 P3 = 4k7, lin.
 P4 = 470 Ω, lin.

Capacitors:

C1, C2 = 100 p
 C3 to C6 = 10 μ, 16 V
 C7, C8, C9 = 4μ7, 16 V
 C10 = 470 μ, 4 V
 C11, C12 = 47 p
 C13 = 33 p
 C14 = 220 μ, 16 V

Semiconductors:

T1, T2 = TUN
 T3 = TUP
 D1 = DUS

IC's:

IC1 = 74123
 IC2 = 7413
 IC3 = 7401
 IC4 = AY-10212

Parts list for figures 12 and 16

Resistors:

R1, R2 = 3k9
 R3 = 6k8
 R4 = 470 Ω
 R5 = 100 Ω
 R6 = 180 Ω
 R7 = 1 k
 R8, R9, R10 = 1.5 Ω
 P1 = 1 k, preset

Capacitors:

C1, C2 = 100 n
 C3, C4 = 1 n
 C5 = 2200 μ, 16 V
 C6 = 220 μ, 4 V
 C7 = 10 μ, 16 V
 C8 = 470 μ, 6.3 V

Semiconductors:

B1 = B20 C2000 bridge rectifier
 D1 = omitted
 D2, D3 = DUS
 D4 = zener 4.7 V, 400 mW
 T1 = TUP
 T2, T3, T5 = TUN
 T4 = BD 240 or equ.

Miscellaneous:

F1 = fuse 2 A slo blo
 Tr1 = 8 V, 2 A transformer

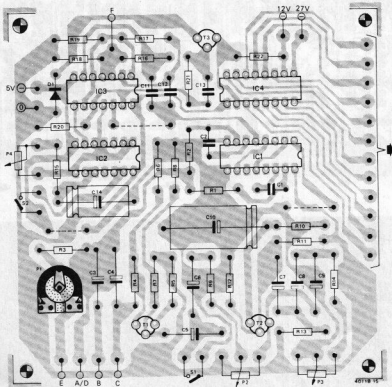
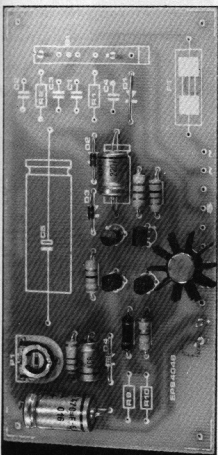
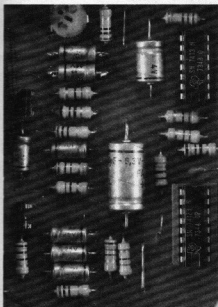
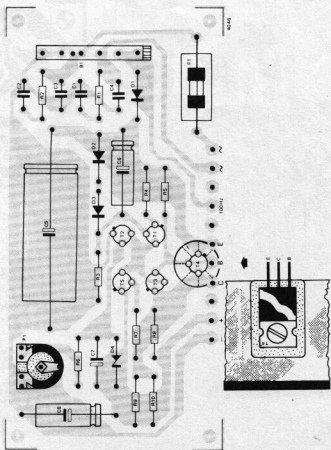
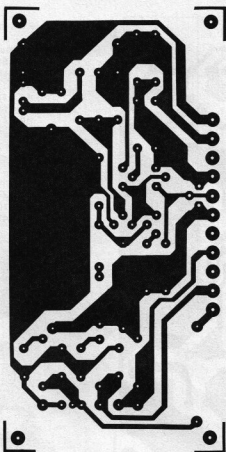


Figure 15. P.c. board and component layout for the MOS master oscillator (EPS no. 4011 B-2).

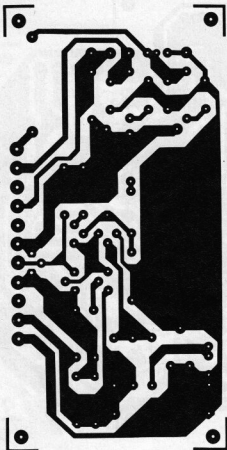
Figure 16. P.c. board and component layout for the TTL oscillator power supply.



16



17



Parts list for figures 13 and 17

Resistors:

R3 = 6k8
 R4, R14 = 470 Ω
 R5 = 100 Ω
 R6 = 180 Ω
 R7, R13 = 1 k
 R8 = 4.7 Ω
 R11 = 100 Ω , 1 W
 R12 = 22 Ω
 (R15 omitted)

Capacitors:

C6 = 220 μ , 4 V
 C7 = 10 μ , 16 V
 C8 = 470 μ , 6.3 V

C9 = 1000 μ , 40 V
 C10 = 100 μ , 35 V

Semiconductors:

B1 = B40 C250 bridge rectifier (40 V
 250 mA)
 D2, D3 = DUS
 D4 = zener 4.7 V, 400 mW
 D5 = zener 12 V, 400 mW
 D6 = zener 15 V, 400 mW
 T1 = TUN
 T2, T3, T5 = TUP
 T4 = BC 140
 T5, T6 = BC 160

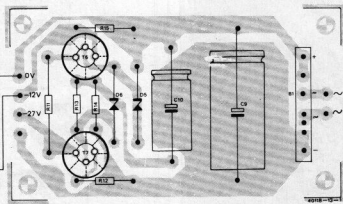
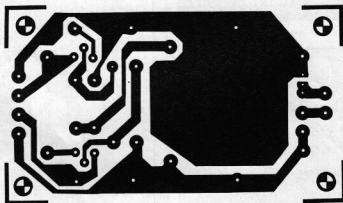
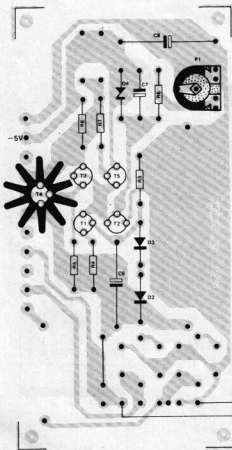
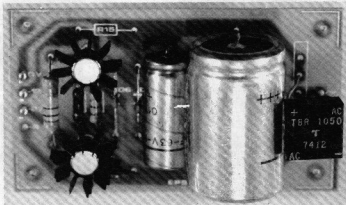
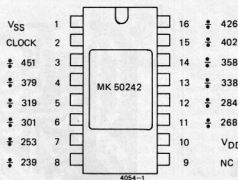


Figure 17. Showing how a modified TTL power supply board is interconnected with an ancillary board to provide the three voltages required for the MOS master oscillator (EPS no.s 4046 and 4011 B-13).

Figure 18. Pinning of the MK50242. This is identical to the pinning of the AY-10212, with the exception of pin 9: NC for the former, -27.5 V for the latter.

Figure 19. Modifications to the power supply circuit for use with the MK50242. D6 and T7 are omitted (bridged), D5 is a 15 V type and the transformer secondary voltage can be reduced to 15 V.

18



19

version, being smaller, is easily mounted in a small metal box for screening.

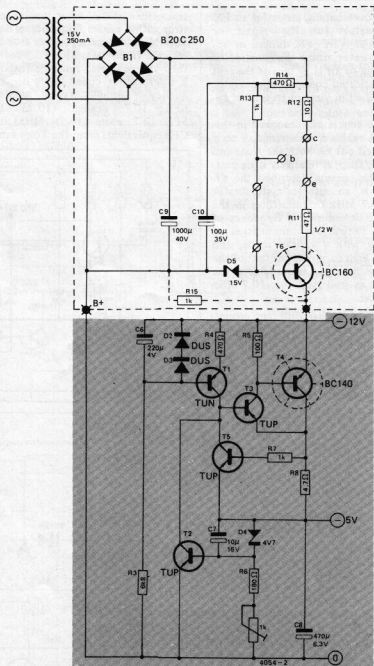
A printed circuit board and layout for the 5 V power supply for the TTL oscillator is given in figure 16. As T4 dissipates several watts it must be mounted external to the board on an adequate heatsink. The power supply for the MOS version uses the board of figure 16 (with different polarity transistors) plus an ancillary board to derive the negative supplies for the AY-10212. In this case the load current is only about 100 mA, so T4 is a T05 device mounted on the board in a cooling clip (as are T5 and T6). The suppression components required to protect the TTL dividers against noise on the supply lines are omitted from this version, as are the bridge rectifier and smoothing capacitor, which are mounted on the ancillary board.

Alternative MOS IC

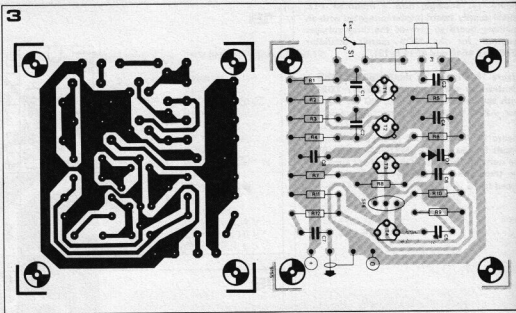
An alternative IC for the AY-10212 is the MK50242 (Mostek). This IC is pin compatible with the AY-10212, see figure 18, so it can be mounted on the same printed circuit board. It has the advantage that only one (negative) supply voltage is required: -12 V. The -27.5 V supply is not necessary for this IC.

This results in a minor simplification of the power supply circuit (figures 13 and 17): zenerdiode D6 and T7 are omitted, as shown in figure 19. Two wire links are needed on the board, one in place of D6 and one to bridge the original collector and emitter connections of T7.

The nominal supply voltage for the MK50242 is -15 V, so that it is advisable to use a 15 V zener for D5. The originally specified 12 V type could also be used, however: this is within the permissible supply voltage range of the IC.



simple fm test generator



The need occasionally arises for an FM test generator for the repair or alignment of VHF FM tuners or receivers. However, unless the constructor is something of an H.F. fanatic the cost of a sophisticated commercial generator is not justified in view of its limited applications.

The simple generators described in this article will enable a wide range of tests to be carried out on both the front end and the i.f. strip, at relatively little cost. In both the circuits described the r.f. oscillator is an astable multivibrator with a 10.7 MHz ceramic filter in the coupling to determine the frequency of oscillation. Frequency modulation is carried out with a varicap diode, and due to the high harmonic content of the output a useful signal is available in the VHF band as well as at the 10.7 MHz fundamental.

The two circuits have different properties. The generator of figure 1 has good frequency stability and oscillates at the exact frequency of the filter. The oscillator comprises T1 and T2 with T3 as an output buffer. Frequency modulation is accomplished by feeding the modulating signal to the BB109 varicap diode, which varies its capacitance and hence the frequency of the h.f. oscillator.

The frequency deviation of this generator is small, typically 1.3 kHz at 10.7 MHz, and 13 kHz at the 10th harmonic (107 MHz). A good i.f. strip should be capable of noise-free handling of an FM signal even with this small deviation, so this is a useful test.

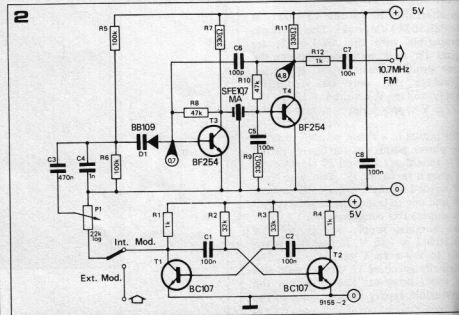
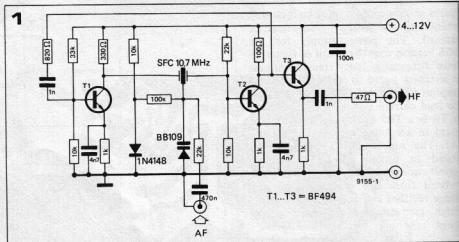
The circuit of figure 2 uses a different method of modulation which permits a much larger deviation of some 75 kHz at the 10th harmonic. This is the normal maximum deviation used in FM broadcast transmitters. An astable multivibrator T1/T2 provides the modulating signal, or external modulation may be used.

A side effect of this method of modulation is that the centre frequency of the h.f. oscillator is about 40 kHz lower than the resonant frequency of the cer-

amic filter. Thus, when testing an i.f. strip with a centre frequency of exactly 10.7 MHz (for example, one fitted with ceramic filters type SFE 10.7 red spot) then the generator must be fitted with a filter colour coded for a higher frequency. Suitable types would be SFE 10.7 orange (10.73 MHz), SFE 10.7 white (10.76 MHz) or the CFS equivalents from the Toko range.

A printed circuit layout for the second circuit is given in figure 3.

Although, as mentioned earlier, the generators are primarily intended for testing and alignment of i.f. strips, their high harmonic content makes them suitable for testing front ends. For this application the 8th (85.6 MHz), 9th (96.3 MHz) and 10th (107 MHz) harmonics are of interest.



MARKET MARKET MARKET

Motorola CMOS 2-of-8 Tone Encoder

Motorola have just introduced the MC14410 2-of-8 tone encoder, another member of their CMOS digital subsystem family. This tone encoder is designed to accept inputs from a 16 button keyboard which is connected in a 4 x 4 matrix. It has two outputs which give digitally synthesized high and low band sinewaves as specified for telephone tone dialling systems. Applications of the MC14410 also include radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

The master clocking is provided by an on chip oscillator which may be controlled by either an external crystal or an external clock source, typically at a frequency of 1 MHz. This controls two separate sinewave generators, the output stages of which have

NPN bipolar structures on the same substrate allowing a low output impedance of 80 ohms. The output frequencies are for low band: 697, 770, 852, 941 Hz, and for high band: 1209, 1336, 1477, 1633 Hz, all with an accuracy of $\pm 0.2\%$ (not including crystal tolerance). Harmonic distortion is low with 2nd to 14th harmonics inclusive typically more than 30 dB below the fundamental frequency. When a key is depressed one frequency from each band is produced, the actual combination depending on the key chosen. Multiple key lockout is incorporated in the design to eliminate the need for mechanical lockout in the keyboard. The MC14410 has fast oscillator turn on and turn off times - typically 8 ms to turn on after application of 5 Vdc supply. Noise immunity is typically 45% of supply voltage which can lie within the range 4.4 to 6.0 Vdc. *Motorola Ltd.*

Semiconductor Products Division, York House, Empire Way, Wembley, Middlesex.

Two-timing watch

The exact time in any two zones can be kept simultaneously by a new 6-function CMOS watch circuit which is now available in quantity from National Semiconductor Corp. for hybrid assembly into LED (light-emitting diode) wrist watches.

Known as the model 'MM5880', the new watch circuit provides all the control signals that are needed by a four-digit LED watch. The circuit provides hours, minutes, seconds, and month-with-date under control of a single push-button.

A second push-button controls the display of seconds, minutes, and hours in a different time zone. This feature permits travellers to keep track of the time in the home zone while maintaining local time. Businessmen will find

this feature useful when communicating long-distance. Resetting the second time zone does not affect the time kept for the first zone. This insures a accurate calibration at all times. Also available is a second version of the watch circuit the MM5860, which is designed to present calendar information in the European format of date-and-month. (The American format presents the month first.)

Both models may be connected to display time in either a 12-hour or 24-hour format. The 12-hour version provides an a.m. indication, which is useful in setting the calendar.

Outputs interface directly with currently available standard bipolar segment-driver and digit-driver circuits.

The circuits operate from any d.c. source that supplies a voltage between 2.4 and 4.0 volts. Circuit chips are furnished in a form suitable for hybrid assembly in modules.

National Semiconductor GmbH, Industriestraße 10, D 808 Fürstenfeldbruck.

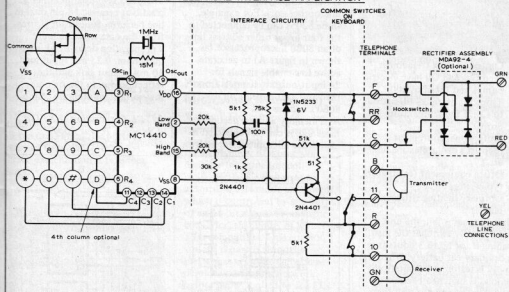
16-pin and 22-pin 4K RAMS

AMI Microsystems have introduced two 4K random access memories featuring small chip size, single transistor cell design and N-channel processing. The AMI S4021 series of 4096-word by one-bit arrays, is available in four different performance capabilities to meet a variety of applications: for example, the maximum data access time for the S4021-4 is 200ns which compares with 400 ns for the 'basic' S4021. The S4021-4 also features a minimum cycle time of 400ns and minimum read/modify/write cycle time of 510ns. The circuit includes a unique sense amplifier, which consumes minimal power while maintaining a high noise immunity. Typical current consumption is 30 mA. The S4021 series is initially available in production quantities in the 22-pin ceramic DIP, and is pin-compatible with the Texas TMS 4060 and Intel 2107B.

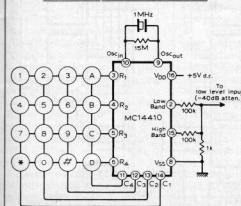
In the AMI S4096, a 16 pin 4K RAM, the same memory cell structure and process is employed as in the S4021 series. Maximum data access time ranges from 250ns to 400ns, while the minimum read/write and read/modify/write cycle times are 375ns and 520ns respectively. It is pin-compatible with the Mostek MK4096, and is currently available in development quantities.

AMI Microsystems Ltd., 108A Commercial Road, Swindon, Wilts.

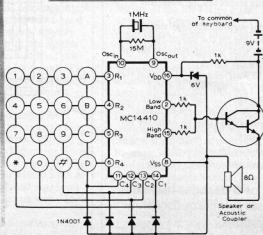
TYPICAL TELEPHONE INTERFACE APPLICATION



LOW-LEVEL OUTPUT TONE GENERATOR APPLICATION



BATTERY POWERED OPERATION (DRIVING AUDIO SPEAKER)

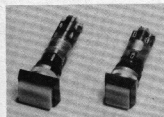


MARKET MARKET

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Low-cost illuminated push-button switches

Roxburgh Electronics Ltd. announce a new range of illuminated push-buttons. The 4000 series are rated at



5 A/250 V a.c. or d.c., and feature either momentary or alternate action in changeover versions of up to three poles. They have been designed for panel-mounted applications, and require a panel aperture of 16.2 mm diameter. A choice of seven opaque coloured, or six translucent coloured lens types is available, and these may be square, rectangular or circular according to application requirements. The lens can be illuminated by either a filament or a neon lamp, and the lens can be captioned either by surface engraving or by applying a transfer to the inside surface. Typical prices for the 4000 series, in 100 off quantities, are from £1.60 in the case of a single-pole momentary action, and from £1.69 for alternate action single-pole versions.

Roxburgh Electronics Ltd.,
22 Winchelsea Road, Rye, Sussex.

New 'jewelled' LED

Norbain Electronics Ltd. announce a new LED indicator. This low-current bright green or red LED uses a flattened 'jewelled' lens to provide distinct signals in high-ambient light levels with a 90° included view angle. The i.c. compatible LED's are particularly useful for switchboards, monitor panels, telecommunication consoles and computer industries where indi-



cations must be seen by staff not directly in front of the indicator. National Semiconductors Ltd. can produce specialised arrays of these lamps to customer requirements.

The special surface provides pinpoints of high intensity light (2500 cd/m² at 10 mA) which

catch the eye in a way that identifies that the indicator is internally lit, not ambient lit. This avoids the confusion that often occurs with simple LED packages in bright environments.

Norbain Electronics Ltd.,
Norbain House,
44 London Street,
Reading, Berks.

Battery-operated AC generator

Jermyn now offer their well known invertors in an all silicon transistor version giving increased reliability with a one year guarantee.

When the mains electricity supply fails, due to strikes/power cuts/or failures this unit can be used as an emergency supply for:



- Central heating (remember even Gas and Oil have electric pumps and thermostats)
- Tropical fish tanks (disastrous to fish if the temperature drops)
- Professional equipment (dentist's drill, telex machines etc.)
- Office equipment (calculators, typewriters etc.)
- Ordinary lighting (filament lamps)

When the mains fail, the unit automatically switches the load, running it for up to 3 hours from an ordinary car battery. When the supply is restored, automatically the load is switched back to the normal mains and the unit then acts as a battery charger, keeping the battery topped up until the next mains failure, even if it is months later!

Two versions are available depending on the size of the load: 150 Watt version running on one 12 V car battery
300 Watt version running on two 12 V car batteries in series. Also the unit can be used to run any normal household mains equipment from an ordinary car battery.

Jermyn Manufacturing,
Sevenoaks, Kent.

1 of 8 decoder has many uses in microprocessing systems

Intel have introduced a high-speed

Schottky bipolar 1 of 8 decoder which has been designed primarily as an adjunct to their range of microprocessors, but which is also useful in conventional logic circuits.

The new i.c., type 8205, contains a three-input, eight-output, gating network which causes one output to go 'low' for each of the eight, three-bit, binary input codes that can be fed to the input. An on-chip three-input gate inhibits the decoded output unless the three enable inputs are in the required logic condition (two low, one high). This feature allows 8205s to be connected, without additional logic, to form decoders up to 1 of 24 in 8 line increments without sacrificing speed. The addition of a simple inverter or two enables decoders up to 1 of 64 to be constructed. Obviously, the low propagation delay (typically 20 ns) enables 8205s to be cascaded to produce decoding networks of virtually any size.

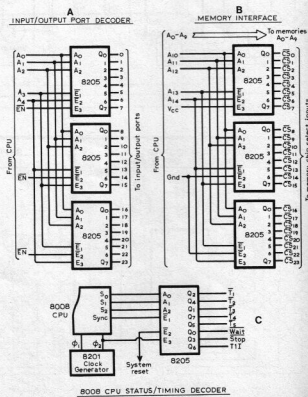
The prime application for the 8205 is in microprocessing systems employing Intel and other microprocessors. For example, three 8205s can be connected to the four lower order address lines of an 8080 microprocessor (as shown in figure A) to generate active low enable signals for 24 input/output channels from the word that appears on the 8080's address bus.

As a memory address decoder, three 8205s can be connected to high-order microprocessor address

lines (A10 to A14) and the 24 8205 outputs can each be used to enable a 1K block of read only or random access memory. With this arrangement (shown in figure B) low-order address lines (A0 to A9) are connected to all the memory chips in the memory array to select the required location. Thus, the three 8205s provide enable signals for a memory of 24K. The technique can, of course, be expanded. A single 8205 can be connected to an 8008 cpu (figure C) to decode the three status outputs (S0 to S2) and, at the same time, gate these signals with phase two of the clock and the 'sync' output. As a result, the single device, in addition to providing status information, produces strobe pulses that can be connected directly to 8212s for latching address information; also generating timing signals to control the system data bus, memory timing, interrupt control and automatically inhibiting strobes during 'reset'.

The 8205 is housed in either a plastic or ceramic 18-pin dual-in-line package. Significant figures from the data sheet include: a propagation delay of 18 nsec maximum, 0.25 mA input load, 10 mA output sink and low reflection due to the on-chip low-voltage input diode clamps.

INTEL Corporation (UK) Ltd.,
4 Between Towns Road,
Cowley, Oxford OX4 3NB.



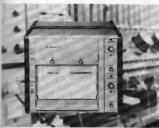
MARKET MARKET MARKET

RETURNS RETAINS RETURNS

Exceptional frequency response in multichannel analogue recorder

The new Gould Brush 2400 direct-writing chart recorder offers channel widths of 100 mm and 50 mm, and uses a servo-controlled pen motor to give exceptional frequency response: 30 Hz at 100 mm, 50 Hz at 50 mm and up to 100 Hz at lower amplitudes. The recorder is available in 12 configurations to meet a variety of requirements, it can be used in 2-channel, 3-channel or 4-channel form (two 100 mm channels; one 100 mm and two 50 mm channels; or four 50 mm channels), and with or without interchangeable plug-in preamplifiers. Portable or rack-mounted versions are available. A plug-in control board (with programmable timer) and plug-in drive amplifiers are standard. The recorder is electrically compatible with all Gould Brush preamplifiers and signal conditioners. The pen motor incorporates a non-contact servo feedback system known as Metrisite, which gives a high stiffness (100 g/mm) and a linearity of 99.65% over the entire channel width.

Rise time is less than 8ms for 100 mm amplitude and 5ms for 50 mm amplitude. Overshoot is less than 1% on square waves and transients, and electronic limiters in the drive amplifier prevent pen damage from off-scale inputs. Trace presentation is true rectangular.



The high resolution obtained with full-scale signals on the 100 mm channels simplifies trace analysis. Built-in ± 5 V pen position controls enable the pens to be positioned anywhere on the channels, and provide up to 5 V of zero offset. This feature, together with the electronic limiters, allows a bipolar signal to be displayed up to 200 mm wide on adjacent channels. A pressurised-fluid writing system provides smudge-free traces of uniform width, and allows the recorder to be operated in any position. Twelve chart speeds between

0.05 mm/s and 200 mm/s are provided. The drive may be started and stopped, and the speed selected, by front-panel pushbuttons or remote control. A paper-supply indicator shows when a new roll is required, and an interlock mechanism stops the recorder when the paper runs out. Plug-in preamplifiers provide a choice of signal conditioners, and offer a wide range of input sensitivities to cover most signal sources. Calibrated zero suppression and selectable low-pass filtering are available. Fully floating input circuits provide up to 500 V isolation at any sensitivity and high common-mode noise rejection. A plug-in d.c. bridge preamplifier is available for use with strain-gauge transducers. The recorder also accepts direct inputs from external signal conditioners or signal sources between 0 and 5 V d.c. The 2400 recorder measures 362 x 311 x 305 mm, and weighs about 30 kg (depending on the number of channels and preamplifiers).

Gould Advance, Data Products Division, Raynham Road Bishop's Stortford, Herts.

Precision Digital Microwave Attenuator

Walmore Electronics Ltd., the recently-appointed UK agents for Anaren Microwave Inc., announce the availability of a precision digital attenuator (model No 61060). The unit uses an absorptive PIN diode attenuator which is controlled by the output of an 11-bit digital-to-analogue converter, the inputs of which are TTL compatible. This control voltage is passed through a linearising network and a temperature correction network before being applied to the PIN diode.

The model 61060 attenuator is specifically designed for applications requiring remote control, low phase shift, high speed and excellent setting repeatability under either static or dynamic conditions. It will provide precision RF signal level control in computer-controlled test setups, radar and communications systems.

The attenuation ranges from 0 to 64 dB above the insertion loss, which is a maximum of 5 dB. Resolution is commensurate with the 11 bit control input. Attenuation linearity is within ± 0.5 dB over the attenuation range and the temperature range of -20 to $+65^\circ\text{C}$.

The frequency response is flat within ± 0.3 dB over the fre-

quency range of 8.5 to 9.6 GHz for all settings of the attenuator. Maximum operational RF power is 100 mW (1 W for survival) and power supply requirements are ± 15 Vdc at $\pm 3\%$ regulation and 100 mA maximum. The impedance of the attenuator is 50 ohms and the phase shift with attenuation lies within $\pm 10^\circ$. The attenuator is supplied in a rugged, lightweight box 5.15" x 4.00" x 1.38" and stripline integrated circuitry is used to ensure high reliability at low cost.

Walmore Electronics Ltd., 11-15 Betterton St, London WC2H 9BS.

Low-cost plug-in power supply units

Coutant Electronics' new SU Series are genuinely low-cost plug-in pcb-mounted power supply units that have been developed for systems and instruments designers who need economical and compact regulated power sources for such components as digital IC's, operational amplifiers, MOS registers, D/A and A/D converters and semiconductor memory units. Suitable for chassis mounting, these single and dual output units are all contained on compact 40 x 80 x 140 mm printed-circuit boards. Connection is made via the gold-plated edge connections or to the board-mounted solder posts, and power input to the units can be applied either through the edge connector or directly to the transformer terminal panel, depending on user preference.

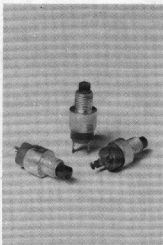
Single output models are available for 5 to 6 V at 1.5 A, 12 to 15 V at 0.5 A, and 24 to 30 V at 0.25 A. A dual output model, which can be connected in an independent or tracking mode, provides two outputs, each variable between 5 and 15 volts. A significant and invaluable feature of the SU Series is the 'over-power' protection that they enjoy thanks to the incorporation of a unique 'thermal foldback' current limiting (TFCL) circuit. The units contain a temperature sensor which ensures that the power dissipation of the series element is contained within defined limits; if these limits are exceeded, the available output current is cut back automatically. By using TFCL protection, the SU Series may therefore be used in a more versatile manner than similar units that just provide overcurrent protection. For example the SU8/5, which is normally a 5-V unit providing 1.5 A, may be transient loaded up

to 4 A with no significant loss of regulation; furthermore, a continuous operation at 2 A is available at all but extremes of mains voltage and ambient temperatures less than 50°C . All units in the SU Series operate from 100 to 264 V 45-60 Hz supplies, have line and load regulations of 0.05%, exhibit a ripple and noise level of less than 1 mV peak to peak, and feature self-resetting overcurrent and thermal protection. Their operating temperature range is 0 to 55°C (70°C with derating), but higher temperature versions are available to special order; temperature coefficient is better than 0.01% per $^\circ\text{C}$.

Coutant Electronics Ltd., 3 Trafford Road, Reading RG1 8JR.

Microminiature push-button switches

Roxburgh Electronics Ltd have extended the range of C & K switches they distribute throughout the U.K., with two series of subminiature and microminiature push-button switches. In the case of the subminiature series, of which two normally-open and two normally-closed versions are available, the contacts are rated from 0.5 A at 250 V a.c. to 1 A at 120 V a.c. or 28 V d.c.



Three different types of microminiature switch are available, two with normally-open contacts, and one, normally-closed. Their contacts are rated from 0.125 A at 250 V a.c. to 0.5 A at 120 V a.c. or 28 V d.c.

Both the subminiature and microminiature switches contain silver contacts and terminals as standard, and can be supplied with circular-section push-button caps in six standard colours.

Roxburgh Electronics Ltd., 22 Winchelsea Road, Rye, Sussex.

Motorola LED sentries never die.

Unlike filament indicator lamps, Motorola Light Emitting Diodes don't die.

They come in three colours—red, yellow and green—and in viewing angles to suit all applications.

We're so confident of your determination to be up-to-date, that we've invested heavily to give you the LEDs you want, when you want them.

Use indicator lamps that are worthy of your equipment. Use Motorola LEDs as sentries to watch over it.

To find out more about the design possibilities of these high-reliability products, just send for the new

Motorola Opto Electronics brochure, which gives you information about our light detectors and couplers too.

You'll find it profitable reading.



MOTOROLA Semiconductors

Motorola Semiconductors Ltd., York House,
Empire Way, Wembley, Middlesex. Telephone: 01-902 8836.
European manufacturing facilities at Toulouse and East Kilbride.
Distributors: Celdis Ltd., Reading, East Kilbride;
GDS (Sales) Ltd., Slough, Dublin; Jermyn, Sevenoaks;
Lock Distribution, Oldham; Semcomps Ltd., Wembley.