



# CHROMASONIC electronics

Dept. 9 56, Fortis Green Road,  
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## C-MOS

## 74 TTL

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CD4001AE	23p	19p	15p
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CD4006AE	£1.59	£1.33	£1.06
CD4007AE	23p	19p	15p
CD4008AE	£1.75	£1.46	£1.17
CD4009AE	Use	CD4049	
CD4010AE	Use	CD4050	
CD4011AE	23p	19p	15p
CD4012AE	23p	19p	15p
CD4013AE	69p	58p	46p
CD4014AE	£1.75	£1.46	£1.17
CD4015AE	£1.75	£1.46	£1.17
CD4016AE	69p	58p	46p
CD4017AE	£1.75	£1.46	£1.17
CD4018AE	£2.51	£2.09	£1.67
CD4019AE	80p	66p	53p
CD4020AE	£1.97	£1.64	£1.31
CD4021AE	£1.75	£1.46	£1.17
CD4022AE	£1.83	£1.53	£1.22
CD4023AE	23p	19p	15p
CD4024AE	£1.26	£1.05	84p
CD4025AE	23p	19p	15p
CD4026AE	£2.79	£2.33	£1.86
CD4027AE	98p	82p	65p
CD4028AE	£1.53	£1.28	£1.02
CD4029AE	£1.12	£1.76	£1.41
CD4030AE	71p	59p	47p
CD4035AE	£1.75	£1.46	£1.17
CD4040AE	£2.01	£1.68	£1.34
CD4042AE	£1.49	£1.24	99p
CD4049AE	69p	58p	46p
CD4050AE	69p	58p	46p
CD4051AE	£2.78	£2.32	£1.85
CD4052AE	£2.78	£2.32	£1.85
CD4056AE	£2.12	£1.76	£1.41
CD4060AE	£2.51	£2.09	£1.67
CD4066AE	£1.13	94p	75p
CD4068AE	28p	24p	19p
CD4069AE	28p	24p	19p
CD4070AE	28p	24p	19p
CD4071AE	28p	24p	19p
CD4077AE	71p	59p	47p
CD4081AE	28p	24p	19p
CD4082AE	28p	24p	19p
CD4085AE	£1.28	£1.06	85p
CD4086AE	£1.28	£1.06	85p
CD4093AE	£1.56	£1.20	£1.04
CD4099AE	£2.95	£2.46	£1.96

	1-24	25-99	100+
7400	14p	12p	10p
7401	14p	12p	10p
7402	14p	12p	10p
7403	15p	12p	10p
7404	16p	13p	11p
7408	16p	13p	11p
7409	16p	13p	11p
7410	16p	13p	11p
7413	29p	24p	20p
7417	27p	22p	20p
7420	16p	13p	11p
7427	27p	22p	18p
7430	16p	13p	11p
7432	27p	22p	18p
7437	27p	22p	18p
7441	75p	62p	50p
7442	65p	55p	43p
7445	85p	71p	57p
7447	95p	83p	67p
7447A	95p	83p	67p
7448	85p	71p	57p
7470	30p	25p	20p
7472	25p	21p	17p
7473	30p	25p	20p
7474	32p	26p	21p
7475	47p	39p	31p
7476	32p	26p	21p
7482	75p	62p	50p
7485	£1.30	£1.09	87p
7486	32p	26p	21p
7489	£3.56	£2.80	£2.10
7490	49p	40p	32p
7491	65p	55p	45p
7492	57p	46p	36p
7493	49p	40p	32p
7495	67p	55p	45p
74100	£1.08	89p	72p
74107	35p	28p	22p
74121	34p	28p	22p
74122	47p	39p	31p
74141	78p	63p	53p
74145	68p	58p	48p
74154	£1.75	£1.48	86p
74174	£1.00	83p	67p
74180	£1.06	88p	71p
74181	£3.20	£2.50	£1.90
74192	£1.35	£1.14	90p
74193	£1.35	£1.14	90p
74196	£1.64	£1.34	99p

555 (8 pin dip) V	55p
555 (TO-99) T	81p
556 (14 pin dip)	£1.29
703 (RF/IF Amp)	68p
709 (8 pin dip)	38p
709 (TO-99)	45p
709 (14 pin dip)	39p
710 (8 pin dip)	39p
710 (TO-99)	45p
710 (14 pin dip)	44p
711 (TO-99)	51p
711 (14 pin dip)	44p
720 (A.M. Radio)	£1.76
723 (TO-99)	£1.09
723 (14 pin dip)	74p
741 (8 pin dip)	35p
741 (TO-99)	43p
741 (14 pin dip)	36p
747 (14 pin dip)	£1.04
748 (8 pin dip)	42p
748 (TO-99)	46p
748 (14 pin dip)	49p
753 (F.M. 1st. I.F.)	£1.08
75491	88p
75492	£1.10

BHA0002	£3.01
CA2111	£1.19
CA3045	£1.69
CA3046	88p
CA3053	59p
CA3065	£1.60
CA3075	£1.64
CA3078	£1.26
CA3080	59p
CA3081	£1.86
CA3082	£1.86
CA3089E (TDA1200)	£2.43
CA3097E	£1.67
CA3123E	£1.76
CA3401E (LM3900)	68p
CA3600E	£1.44
CT7001	£5.34
L00511 (TO.3)	£1.46
L03611 (TO.3)	£1.46
L03711 (TO.3)	£1.46
L129 (SOT-32)	85p
L130 (SOT-32)	85p
L131 (SOT-32)	85p
LM301 T (TO-99)	65p
LM301 S (E.pin dip)	59p
LM301A T (TO-99)	67p
LM301A S (8 pin dip)	59p
LM307 T (TO-99)	59p
LM307 S (8 pin dip)	57p
LM308 T (TO-99)	£1.96
LM308 S (8 pin dip)	98p
LM308A T (TO-99)	£1.92
LM308A S (8 pin dip)	£6.90
LM309K	£2.34
LM339	£2.25
LM370N	£2.85
LM371	£2.08
LM372N	£1.99
LM373N	£2.99
LM377N	£2.71
LM380	£1.25
LM381	£1.85
LM382	£1.66
LM703	68p
LM1820	£1.03
LM2111	£1.12
LM3900	69p
MCI303L	£1.84
MCI306P	80p
MCI310P	£2.39
MCI312	£2.42
MCI314	£4.13
MCI315	£4.62
MCI327	£1.12
MCI330P	83p
MCI339P	£1.52
MCI350	64p
MCI351	88p
MCI352	88p
MCI357	£1.52
MCI455 (555T)	62p
MCI456CG	£1.68
MCI458CPI	84p
MCI468G	£2.18
MCI495L	£4.24
MCI496G	96p
MC3302P	£1.50
MC3401P	74p
MFC4000B	87p
MFC4060A	79p
MFC4030A	79p
MFC6040	96p
MFC6070	£1.66
MM5314	£4.80
MM5316	£9.99
MVRSV (TO-3)	£1.45
MVR12V (TO-3)	£1.45
MVR15V (TO-3)	£1.45
NE540L	£1.25
NE546A	£1.16
NE555V	73p
NE556	£1.29
NE560B	£5.06
NE561B	£5.06
NE562B	£5.06
NE563	£2.96
NE565N	£2.63
NE566V	£1.87
NE567V	£2.63
SL414A	£2.09
SL415A	£2.75
SL437D	£7.50
SL440	£2.84
SL610C	£2.03
SL611C	£2.03
SL612C	£2.03
SL613C	£4.31
SL620C	£3.06
SL621C	£3.06
SL622C	£7.62
SL623C	£5.57
SL624C	£2.84
SL630C	£1.87
SL640C	£3.75
SL641C	£3.75
SL645C	£3.75
SL650C	£9.85
SN75491N	88p
SN75492N	£1.10
SN76001N (TAA611)	£1.82
SN76003N	£3.30
SN76013N	£1.98
SN76023N	£1.98
SN76227N (MCI327)	£1.89
SN76532N	£1.88
SN76544N	£1.81
SN76550-2 (TAA550)	89p
SN76552-2	81p
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TAA263	£1.50
TAA300	£2.16
TAA310A	£1.87
TAA320	£1.44
TAA350	£2.43
TAA370	£3.45
TAA550	75p
TAA570	£2.74
TAA700	£5.03
TBA1205	£1.25
TBA231	£1.02
TBA281 (723)	£2.59
TBA500Q	£3.16
TBA520Q	£3.85
TBA530Q	£3.27
TBA540Q	£3.72
TBA550Q	£5.29
TBA560CQ	£5.29
TBA625A	£1.03
TBA625B	£1.03
TBA625C	£1.03
TBA651	£1.87
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ULN2111A	£1.52
ZN414	£1.26

## SIEMENS LCD's

## LINE-O-LIGHT

LIQUID CRYSTAL DISPLAY complete with socket and removable reflective backing. Ref AN4132R 13mm character height. Can be directly driven by National Semiconductors Alarm Clock chip MMS316. £13.99



NEW LED Linear Cursors each device contains 10 light emitting diodes in a 20pin dual-in-line package. Ideal for solid state analogue meters or dials. Type 101 RED £2.26



## PHOTO-DARLINGTON

## SPECIAL PURCHASE

## SEVEN SEGMENT DISPLAYS

**2N5777**  
V<sub>ceo</sub>, V<sub>ceo</sub> 25v, V<sub>ebo</sub> 8v  
V<sub>ceo</sub>, V<sub>ceo</sub> 25v, V<sub>ebo</sub> 8v  
h<sub>fe</sub> 2500; I<sub>c</sub> 250 mA **35p.**

enables  
LIT707 90p; LIT747 £1.99  
0.3" 0.6"

**litronix**  
**Xelton**  
**Monsanto**

**I.C. SOCKETS**

	Dual-in-line				TOS				
Pins	8	14	16	24	28	36	40	8	10
Price	13p	15p	15p	26p	30p	39p	44p	31p	35p

**NEW**  
Litronix Double Digit Displays  
0.5"; Common Anode \* 2 R/H  
D.P.'s  
DL727 gives +1.9  
DL727 gives 0.0 to 9.9  
Suitable for Clocks; Instruments;  
T.V. Channel Indicator  
Our Price £4.75 each.

**L.E.D.'s**  
Free snap-on plastic retainer

	0.125" dia. lens (TIL209)			0.16" dia. lens			0.2" dia. lens (MLED 650)		
	1+	10+	100+	1+	10+	100+	1+	10+	100+
Red	16p	15p	13p	27p	24p	22p	18p	16p	14p
Green	27p	24p	22p	33p	30p	27p	30p	27p	25p
Orange	27p	24p	22p	33p	30p	27p	30p	27p	25p
Yellow	34p	31p	29p	35p	32p	29p	35p	33p	30p

**NOTICE**  
Postage & Packing Charges

With the recent increase in postal charges and a continuing increase in packaging cost, we have been forced to review our policy.

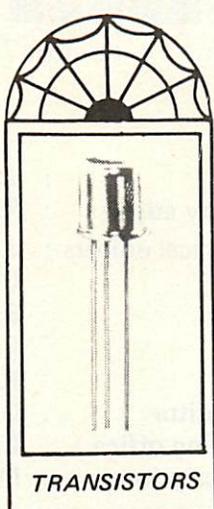
Henceforward:  
1. Orders valued at £5 or 1. more will be post free.  
2. All U.K. 'small package' orders will go first class mail.  
3. Minimum postage & packing charge will increase to 20p.

NEW Opto-isolators  
ILI (4N25 or TIL116)  
6 pin industry standard package.  
2.5KV isolation £1.00

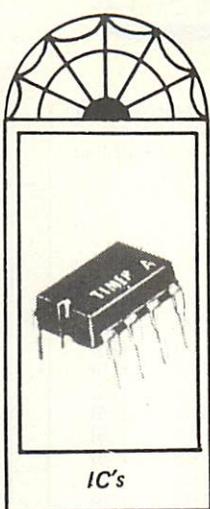
	COMMON ANODE R/H Dec. Pt.	COMMON ANODE L/H Dec. Pt.	COMMON ANODE - 1 Dec. Pt.	COMMON ANODE R/H Dec. Pt.	Our Price
<b>0.3"</b>	RED DL707R	DL707	DL701	DL704	£1.82
	GREEN MAN51	MAN52	MAN53	MAN54	£1.82
	RED MAN71	MAN72	MAN73	MAN74	£1.82
	YELLOW MAN81	MAN82	MAN83	MAN84	£1.82
	ORANGE MAN3610	MAN3620	MAN3630	MAN3640	£1.82
<b>0.4"</b>	GREEN XAN51	XAN52	-	XAN54	£1.49
	RED XAN71	XAN72	-	XAN74	£1.49
	YELLOW XAN81	XAN82	-	XAN84	£1.49
<b>0.6"</b>	GREEN MAN4510	MAN4520	MAN4530	MAN4540	£2.32
	RED MAN4710	MAN4720	MAN4730	MAN4740	£2.32
	YELLOW MAN4810	MAN4820	MAN4830	MAN4840	£2.32
	ORANGE MAN4610	MAN4620	MAN4630	MAN4640	£2.32
	C.A. L/H Dec. Pt.	C.A. - 1	C.C. L/H Dec. Pt.	C.C. - 1	



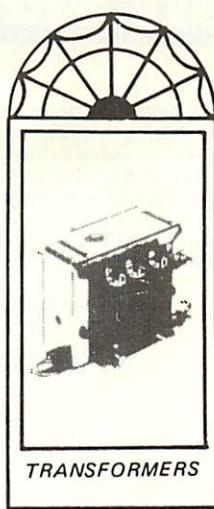
CAPACITORS AND RESISTORS



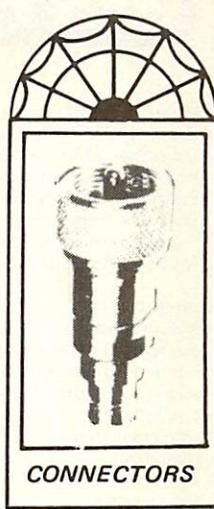
TRANSISTORS



IC's

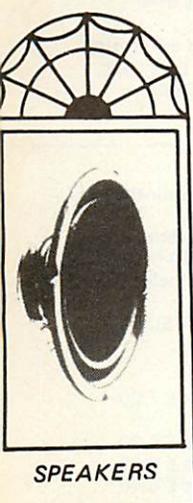


TRANSFORMERS

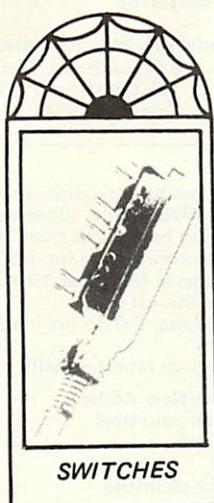


CONNECTORS

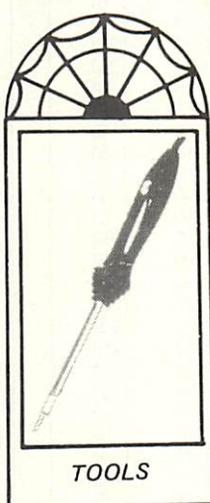
## Use DORAM components for your project



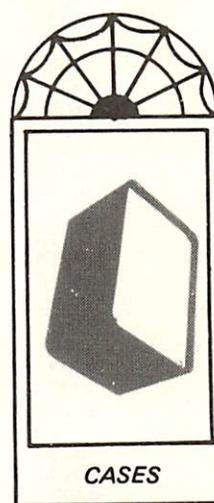
SPEAKERS



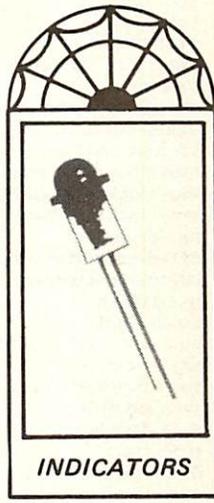
SWITCHES



TOOLS



CASES



INDICATORS

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The doorway to amateur electronics

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# 60<sup>p</sup>

# EPS PRINT SERVICE

Many Elektor circuits are accompanied by designs for printed circuits. For those who do not feel inclined to etch their own printed circuit boards, a number of these designs are also available as ready-etched and predrilled boards. These boards can be ordered from our Canterbury office. Payment, including £ 0.15 p & p, must be in advance. Delivery time is approximately three weeks. Bank account number: A/C No. 11014587, sorting code 40-16-11 Midland Bank Ltd, Canterbury.

circuit	number	issue	price	% VAT
edwin amplifier	97-536	6	1.20	(25)
austereo 3-watt amplifier	HB11	5	1.10	(25)
austereo power supply	HB12	5	0.55	(25)
austereo control amplifier	HB13	5	1.50	(25)
austereo disc preamp	HB14	5	0.65	(25)
universal frequency reference	HD4	5	1.10	( 8)
distortion meter	1437	1	1.65	( 8)
a/d converter	1443	3	0.90	( 8)
tap sensor	1457	1	0.60	( 8)
minidrum gyrator	1465A	2	0.80	(25)
minidrum mixer/preamp	1465B	2	0.55	(25)
minidrum noise	1465C	2	1.05	(25)
miniature amplifier	1486	6	0.55	(25)
light dimmer	1487	6	0.45	( 8)
beetle	1492	4	2.20	( 8)
equa amplifier	1499	1	1.20	(25)
electronic loudspeaker	1527	2	0.50	(25)
mostap	1540	2	1.05	( 8)
car power supply	1563	4	1.25	( 8)
digital rev counter (control p.c.b. only!)	1590	1	0.55	( 8)
car anti-theft alarm	1592	4	1.40	( 8)
mos clock 5314 clock circuit	1607A	1	1.15	( 8)
mos clock 5314 display board	1607B	1	0.85	( 8)
mos clock timebase	1620	4	0.70	( 8)
minidrum tap	1621A	2	0.70	(25)
minidrum ruffle circuit	1621B	3	1.10	(25)
automatic bassdrum	1621C	3	0.55	(25)
microdrum	1661	2	0.95	(25)
aerial amplifier	1668	1	0.95	(25)
coilless receiver for MW and LW	3166	5	0.80	(25)
tap preamp	4003	4	1.80	(25)
twin minitron display	4029-1	2	1.40	( 8)
twin led display	4029-2	2	1.40	( 8)
twin decade counter	4029-3	2	1.40	( 8)
recip-riaa	4039	2	0.50	( 8)
disc preamp 76131	4040A	3	0.95	(25)
maxi display	4409	2	1.50	( 8)
versatile digital clock	4414B	6	1.10	( 8)
dil-led probe	5027A+B	2	1.85	( 8)
big ben 95	5028	2	1.25	(25)
compressor	6019A	3	1.20	(25)
tv sound	6025	2	1.40	(25)
car clock (2 boards)	7036	6	1.75	( 8)
car clock front panel (transparent red plastic)	7036-3	6	0.90	( 8)
tup/tun tester	9076*	4	1.70	( 8)
tup/tun tester front panel	9076/2A	4	1.90	( 8)
p.c.b. and wiring tester	9106*	5	0.55	( 8)
rhythm generator M 252	9110*	5	0.80	(25)
7400 siren	9119*	5	0.75	(25)
CA3090AQ stereo decoder	9126*	5	0.80	(25)
kitchen timer	9147*	5	0.75	( 8)
capacitance meter	9183*	5	0.75	( 8)

## NEW:

circuit	number	issue	price	% VAT
tap preamp front panels:				
power	1626A	7	1.55	(25)
input	1626B	4	1.55	(25)
volume	1626C	4	1.55	(25)
tone	1626D	4	1.55	(25)
width	1626E	4	1.55	(25)
clamant clock, alarm	4015-13	7	1.30	( 8)
clamant clock, time signal	4015-16	7	0.85	( 8)
ota pll	6029	7	1.10	(25)
tv tennis, main pcb	9029-1A*	7	3.80	( 8)
tv-tennis, modulator/oscillator	9029-2*	7	0.90	( 8)
frequency counter	9033*	7	1.30	( 8)
tap power	9072*	7	1.90	(25)
tv tennis 5-volt supply	9218A*	7	0.80	( 8)

\* with solder mask

All prices include VAT at the rate shown in brackets.

# ELEKTOR

Volume 1 — number 7

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Editorial offices, administration and advertising:  
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Elektor has been published every two months until August 1975; it now appears monthly.

Copies can be ordered from our Canterbury office. The subscription rate for 1975 is £ 3.60 (incl. p & p); the first issue (Nov/Dec 1974) will be included in this at no additional cost.

Single copies: £ 0.35 (incl. p & p; £ 0.45).

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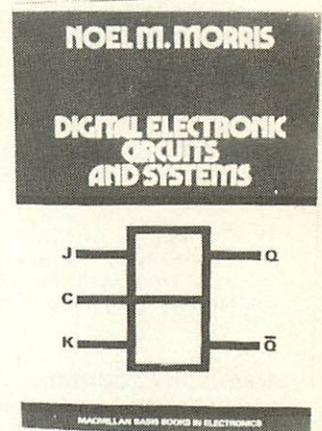
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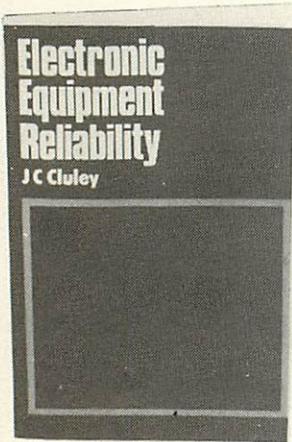
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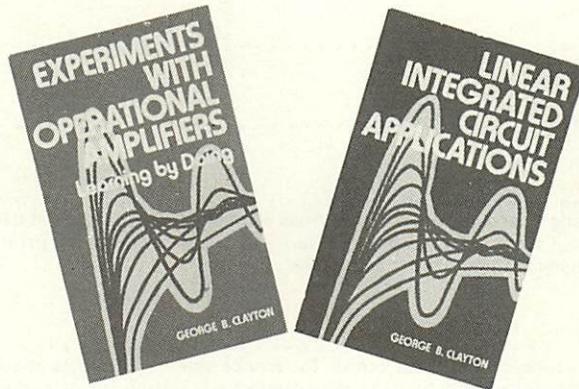
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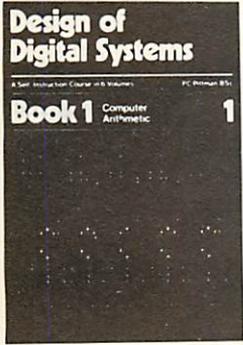
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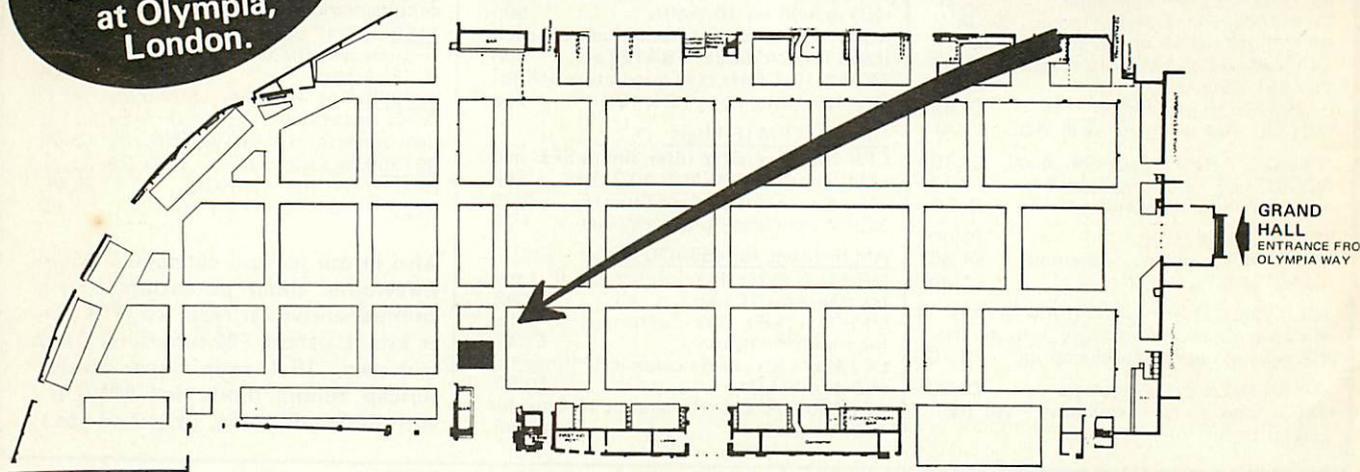
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To distinguish sync. pulses from video information, sync. pulses are negative-going and confined to a voltage below that required for zero beam current (black level). Video information occupies a range of voltages above black level up to the voltage required to saturate the TV tube phosphor (peak white level). Circuitry in the TV distinguishes between sync. pulses and video information. Field sync. pulses

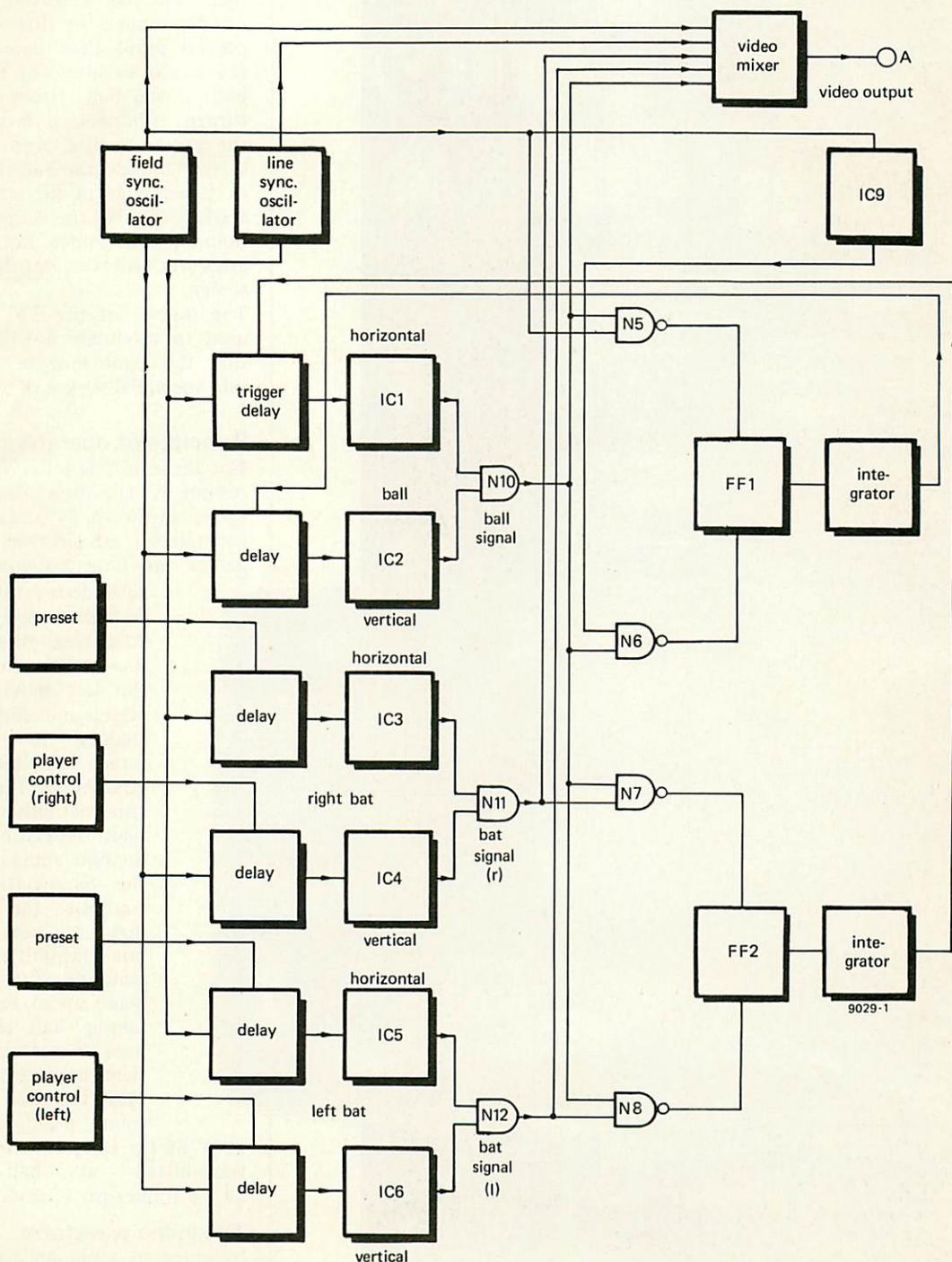
also have a longer duration to distinguish them from line sync. pulses. From the foregoing some of the requirements for the circuit become apparent. Firstly, the circuit must contain oscillators capable of generating field and sync. pulses at the appropriate frequencies (50 Hz and 15625 Hz respectively). Secondly, circuitry for generating the bat and ball waveforms, and for controlling the movement of these, is required. Fortunately, since we are concerned only with white bats and ball on a black background the only modulation required is peak white level or black level, so analogue circuitry is not needed to produce these waveforms, and digital logic circuits can be used to generate the rectangular pulses necessary.

### Block Diagram

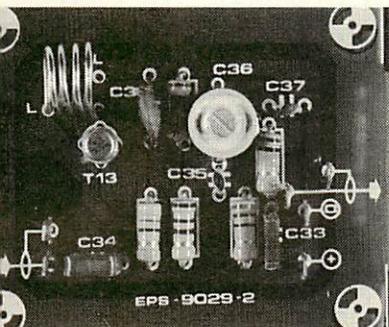
The operation of the circuit is better understood with the aid of a block diagram (figure 1). Sync. pulses from the field and line oscillators are mixed in the video mixer and then fed to the modulator. They are also used to control the timing of the other waveform

All the video waveforms are generated using monostable multivibrators and the generation of the 'bats' is simpler; this will be considered first. The left hand player's horizontal bat generator IC5 is triggered continuously from the line sync oscillator. A presettable trigger delay is incorporated so that the pulse appears a little time after the line sync pulse. This ensures that the bat appears some way in from the left hand edge of

1



screen. The right-hand player's horizontal generator IC3 incorporates a larger delay so that this bat appears on the right-hand edge of the screen. Once the triggering occurs after every sync pulse the result would be a vertical band of white the full height of the screen. This is where the vertical bat generator (IC6 left, IC4 right) comes in. Its monostable is triggered from the field sync pulses via a delay which is continuously variable by the player. This determines the vertical position of the bat. The delayed pulse from the vertical bat generator gates the pulses from the horizontal oscillator so that they are only allowed through for the duration of this pulse. The result is thus a vertical bar on the screen whose vertical position can be varied by the player and



its height (length of the bat) is determined by the duration of the vertical pulse. The same applies for both left- and right-hand bats.

The ball is generated in a similar manner with two monostables (IC1 and IC2). However, since the ball is continuously moving this in effect means that for movement to the right the horizontal trigger delay is increasing all the time, and for movement to the left it is decreasing.

For downwards movement the vertical trigger delay is increasing, while for upwards movement it is decreasing. Of course it is necessary to reverse the direction of ball travel when the ball strikes a bat or the upper and lower boundaries. This part of the circuit operates as follows:

The horizontal ball pulse generator (IC1) is triggered via a delay by the line sync pulses. The delay, and therefore the horizontal position of the ball on the screen, is controlled by the output of an integrator, which is fed with a ramp voltage and therefore generates a pulse which varies the trigger delay accordingly. The slope of the ramp (positive-negative-going) and hence the direction of ball travel is determined by the state of flip-flop FF2. If FF2 is initially reset the ball will travel to the right. However, should the 'ball' output and the right-hand 'bat' output both be high at the same time (i.e. the ball strikes the right hand bat) then the output of N7 goes low, resetting FF2 and reversing the horizontal direction. When the ball strikes the left-hand bat the output of N8 goes low, resetting the flip-flop and causing the ball

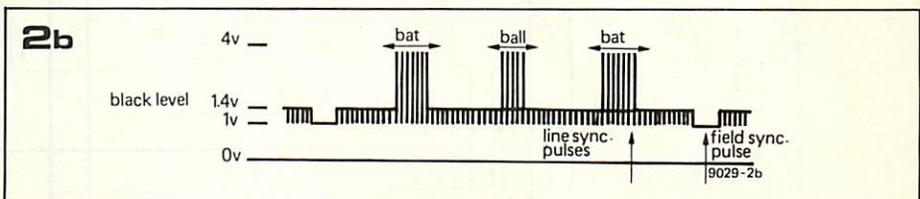
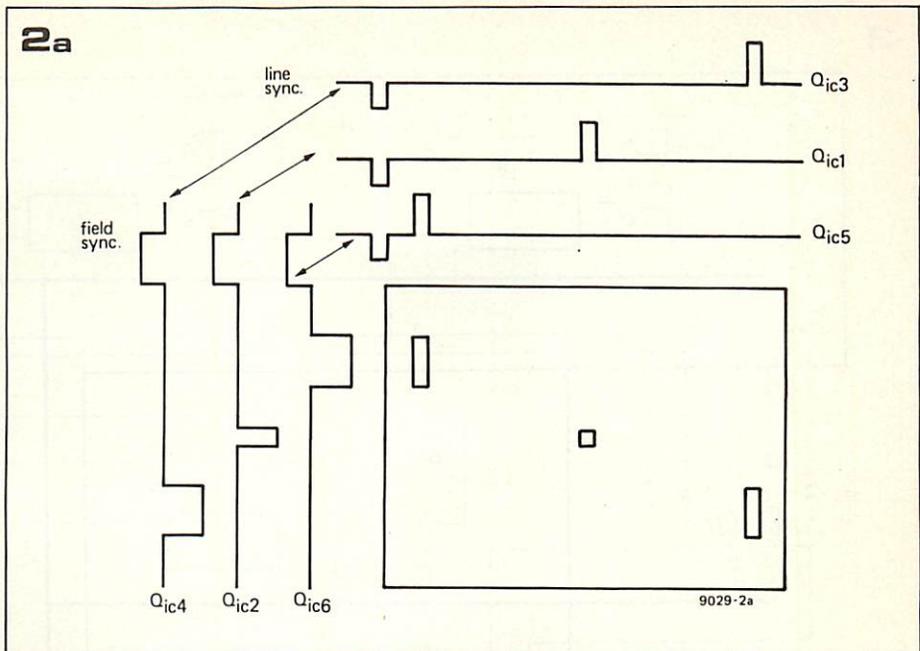


Figure 1. Block diagram of TV Tennis game (excluding modulator/oscillator).

Figure 2a. The horizontal and vertical waveforms are gated together as shown to produce the bat and ball display.

Figure 2b. The complete video waveform as seen on an oscilloscope.

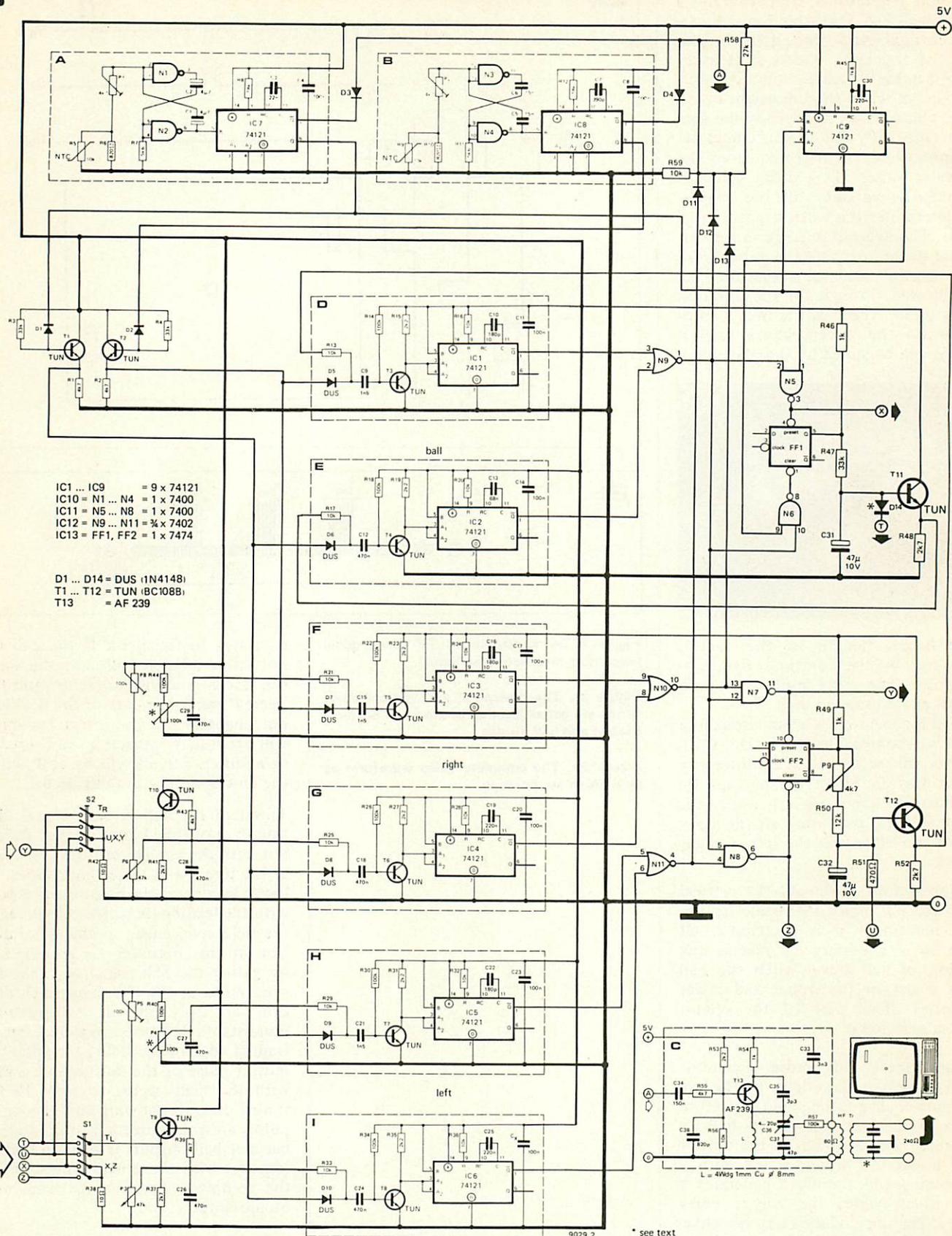
to travel to the right. If the ball does not strike a bat it will leave the side of the screen and will not return until it is 'served', since the state of the flip-flop is not changed and the integrator output will eventually saturate in one direction or another. Service will be dealt with in the description of the full circuit.

Travel of the ball in the vertical direction is controlled in a similar fashion, but here the change of direction occurs at the upper and lower boundaries. The lower border of the picture corresponds with the leading (negative-going) edge of the field sync pulse, so change of direction at this boundary is accomplished by gating the ball signal with the field sync pulse in N5. To change ball direction at the top of the picture a monostable (IC9) is triggered by the trailing edge of the field sync pulse. The output pulse of the monostable is gated with the 'ball' signal to reset FF1. A timing diagram showing how the various pulses are gated together to produce the bat and ball outputs is given in figure 2, together with the general appearance of the complete waveform as seen on an oscilloscope.

### Complete Circuit

The complete circuit is given in figure 3. Field sync pulses are produced by the circuitry in box A, which consists of an astable multivibrator driving a monostable to produce pulses of the correct length. Box B contains similar circuitry, but operating at a much higher frequency, to produce line sync pulses. The Q outputs of these monostables (to produce the negative-going sync pulses) are fed via D3 and D4

3



3a

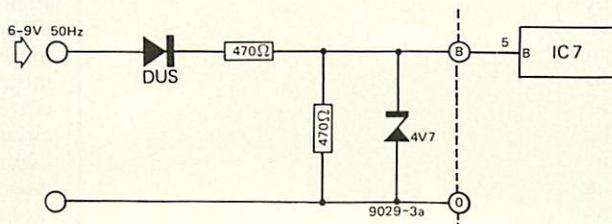
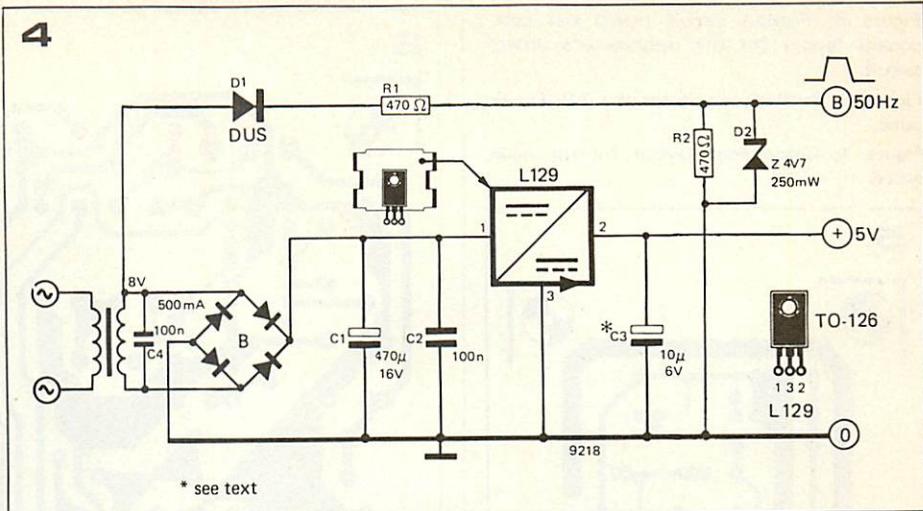


Figure 3. The complete circuit of the TV tennis game. The modulator/oscillator circuit is shown inset at the bottom right-hand corner.

Figure 3a. Suggested modification to derive field sync pulses from the mains for mains only versions of the game. This should give a more stable picture than the free-running field oscillator.

Figure 4. Circuit of the mains power supply for TV Tennis.



#### Parts list for figures 3, 5 and 7

##### Resistors:

R1,R2,R39,R43,R55 = 4k7  
 R3,R4,R47 = 33 k  
 R5,R9 = 10 k NTC  
 R6,R10 = 820 Ω  
 R7,R11 = 5k6  
 R8,R12 = 18 k  
 R13,R16,R17,R20,R21,R24,R25,  
 R28,R29,R32,R33,R36,R56,R59  
 = 10 k  
 R14,R18,R22,R26,R30,R34,R40,R44,  
 R57 = 100 k  
 R15,R19,R23,R27,R31,R35,R53 = 2k2  
 R37,R41,R48,R52 = 2k7  
 R38,R42 = 10 Ω  
 R45 = 1k8  
 R46,R49,R54 = 1 k  
 R50 = 12 k  
 R51 = 470 Ω  
 R58 = 27 k  
 P1,P2 = 4k7 lin. preset  
 P3,P6 = 47 k lin.  
 P4,P5,P7,P8 = 100 k lin. preset

##### Capacitors:

C1,C2 = 4µ7, 10 V  
 C3 = 22 n  
 C4,C8,C11,C14,C17,C20,C23 = 100 n  
 C5,C6 = 15 n  
 C7 = 390 p  
 C9,C15,C21 = 1n5  
 C10,C16,C22 = 180 p  
 C12,C18,C24,C26,C27,C28,C29 = 470 n  
 C13 = 68 n  
 C19,C25,C30 = 220 n  
 C31,C32 = 47 µ, 10 V  
 C33 = 3n3  
 C34 = 150 n  
 C35 = 3p3  
 C36 = 4 ... 20 p trimmer  
 C37 = 47 p

##### Semiconductors:

T1,T2,T3,T4,T5,T6,T7,T8,T9,T10,T11,  
 T12 = BC547B  
 T13 = AF239  
 D1 ... D14 = 1N4148  
 IC1,IC2,IC3,IC4,IC5,IC6,IC7,IC8,IC9  
 = 74121  
 IC10,IC11 = 7400  
 IC12 = 7402  
 IC13 = 7474

##### Sundries:

L = 4 wdg, 1 mm φ Cu, φ 8 mm  
 HF Tr = 60 Ω → 240 Ω impedance con-  
 verter (see text)

to the junction of R58 and R59. This portion of the circuitry functions as the video mixer. Black level occurs when the  $\bar{Q}$  outputs of IC7 and IC8 are both high and the bat and ball inputs to D11, D12 and D13 are all low. The voltage at the junction of R58 and R59 is then solely determined by the value of these resistors and is about 1.35 V. When a sync pulse occurs then the junction of these two resistors is held down to about 1 V via D3 or D4. When bat or ball signals occur the inputs to D11, D12 or D13 go high, so the potential at the junction of R58 and R59 becomes about 4 V. If the unit is to be used for mains only operation the astable in box A can be dispensed with and field sync pulses may be derived from the 50 Hz mains by the modification shown in figure 3a. P1, R5, R6, C1 and C2 are omitted; the sync pulses are fed in at the original connection to the positive side of C1 on the board, and the track between this point and the output of N2 (pin 6 of IC10) must be broken.

The sync pulses are buffered by emitter followers T1 and T2 to avoid loading the monostables excessively. The buffered sync pulses are then fed via the trigger delays to the appropriate monostables which generate the horizontal and vertical components of the bat and ball waveforms. The trigger delay circuits are all identical in principle and merely vary in component values. The trigger delay for IC3 operates as follows: normally T5 is turned on by base current through R23. Its collector voltage (and hence the A inputs of IC3) is low. The cathode of D7 is held at a few volts positive by the voltage via R21 from P7 (max. 2.5 V), and since T2 is turned off the anode of D7 is at 0 V. C15 thus has a voltage across it equal to the voltage on the cathode of D7 minus the base-emitter voltage of T5. On the leading edge of the line sync pulse T2 turns on, forward biasing D7. C15 thus charges until the voltage across it is

$$5 \text{ V} - V_{beT2} - V_{D7} - V_{beT5} = 3 \text{ V}$$

approximately. On the trailing edge of the sync pulse T2 turns off. The voltage on the cathode of D7 therefore reverts to its initial value (the potential sup-

plied via R21 from P7). However, since the voltage across C15 is still 3 V then the base of T5 must be negative. T5 therefore turns off. C15 now charges via R22 until the voltage on the base of T5 reaches about 0.7 V when T5 turns on and the collector voltage goes low, triggering the monostable.

It is evident that the trigger delay is dependent on the time taken to charge C15 after T5 has been turned off, which is in turn dependent upon the voltage applied to the cathode of D7 from P7. The trigger delay may thus be varied by a d.c. voltage, in the case of the bats derived from the various potentiometers, and in the case of the ball from the emitters of T11 and T12.

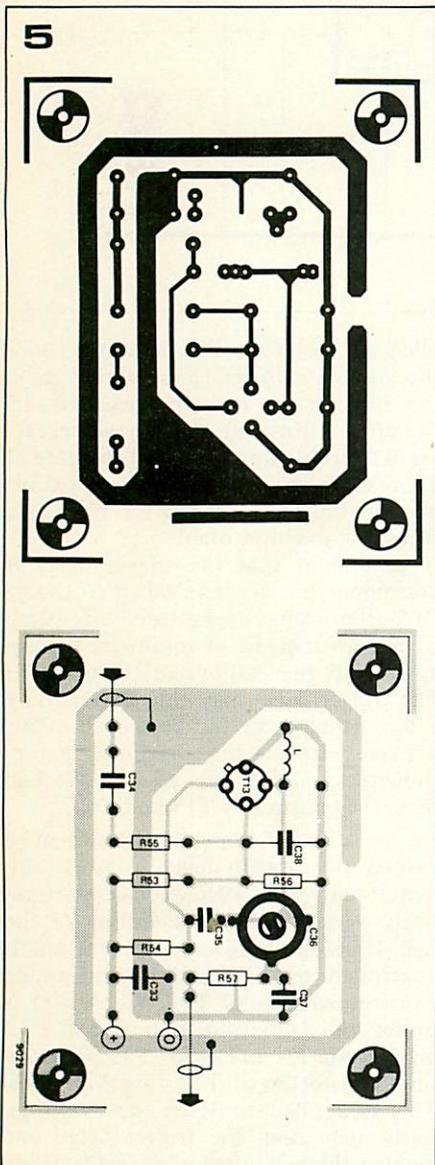
In the case of the ball, as explained earlier, the trigger delay in both horizontal and vertical directions is continuously varied to achieve motion of the ball. Horizontal movement of the ball is controlled by FF2 and the integrator constructed around T12. When FF2 is preset the Q output is high and C32 charges via P9 and R50. The potential on the emitter of T12 therefore rises. This is applied to R13, thus continuously increasing the trigger delay and making the ball move to the right. When FF2 is cleared (reset) then C32 discharges via P9 and R50. The voltage on the emitter of T12 falls, thus decreasing the trigger delay and making the ball move to the left. The rate of charge or discharge of C32, hence the speed of the ball, is determined by the setting of P9. Vertical ball movement is controlled in a similar manner by FF1 and T11. Note that in this circuit the AND-gates shown in the block diagram have been replaced by NOR-gates connected to the Q outputs of the monostables. This is of course exactly equivalent to AND-gates connected to the Q outputs (De Morgan's theorem).

The horizontal bat trigger delays are preset, by P7 for the right-hand player, and by P4 for the left-hand player. This allows the position of the bats to be adjusted to a few cm away from the sides of the screen. The vertical position of the bats is continuously adjustable, by P6 for the right-hand player and P3 for the left-hand player. P5 and P8 are presets used to adjust the bat position

Figure 5. Printed circuit board and component layout for the modulator/oscillator circuit.

Figure 6. Printed circuit for the TV Tennis game.

Figure 7. Component layout for the main board.

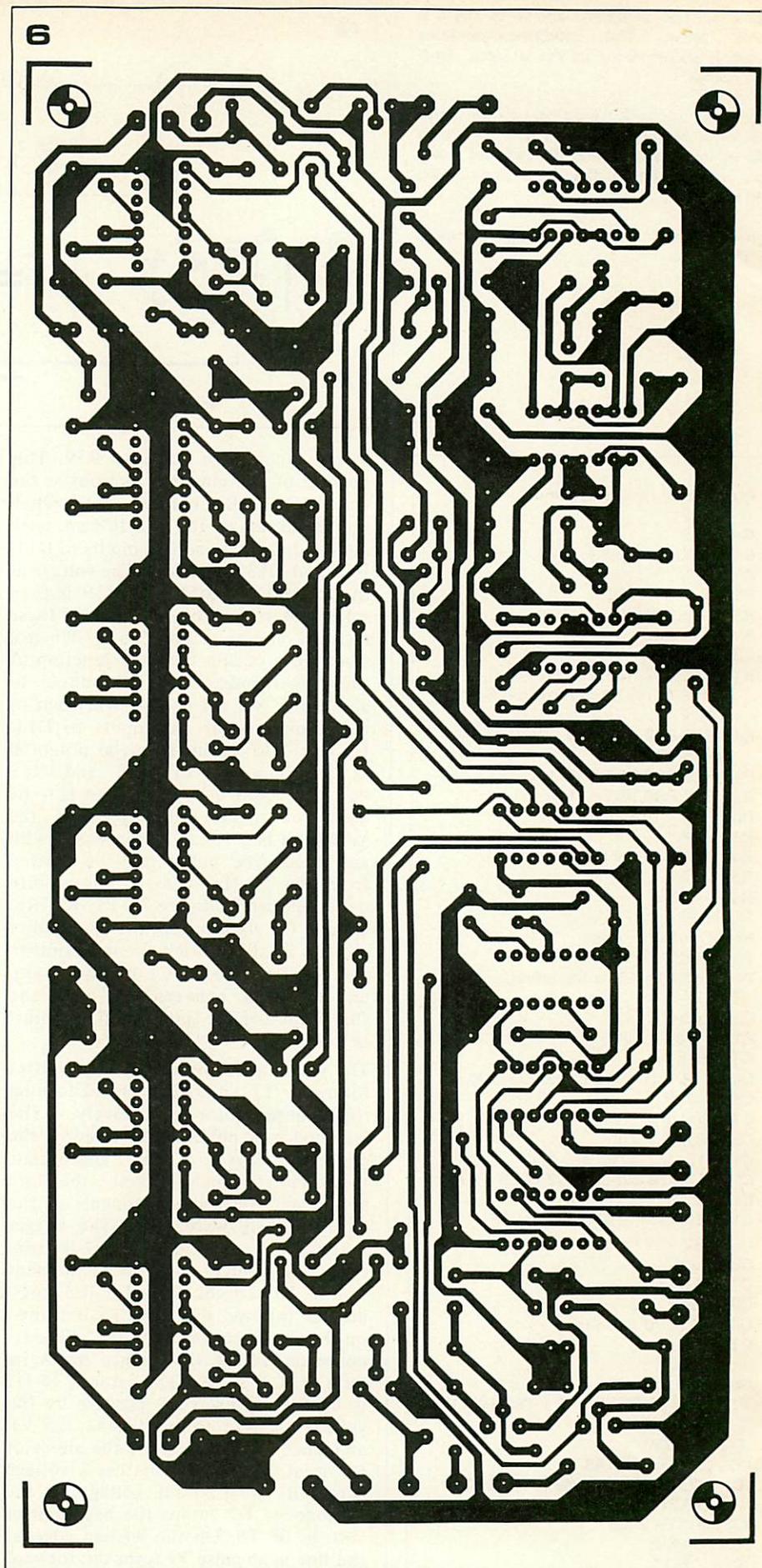


so that P6 and P3 are effective over the full height of the screen.

### Service of the ball

It is evident that if the state of FF2 is not reversed by a coincidence between the ball and one of the bat signals then the voltage at the emitter of T12 will continue to rise or fall as C32 either charges or discharges, until it reaches either zero volts or supply minus the base-emitter voltage of T12. The ball will then disappear off one side of the screen or the other and will not return. For this reason (as well as for the rules of the game) it is necessary to 'serve' the ball when this has occurred.

Ideally the ball should emanate from the bat of the player who is serving. However, in practice this is difficult to achieve as it means that at the instant of service the vertical ball trigger delay must be matched to the vertical bat trigger delay. Since the delay circuits are independent component tolerances will make this unlikely. It is, however,

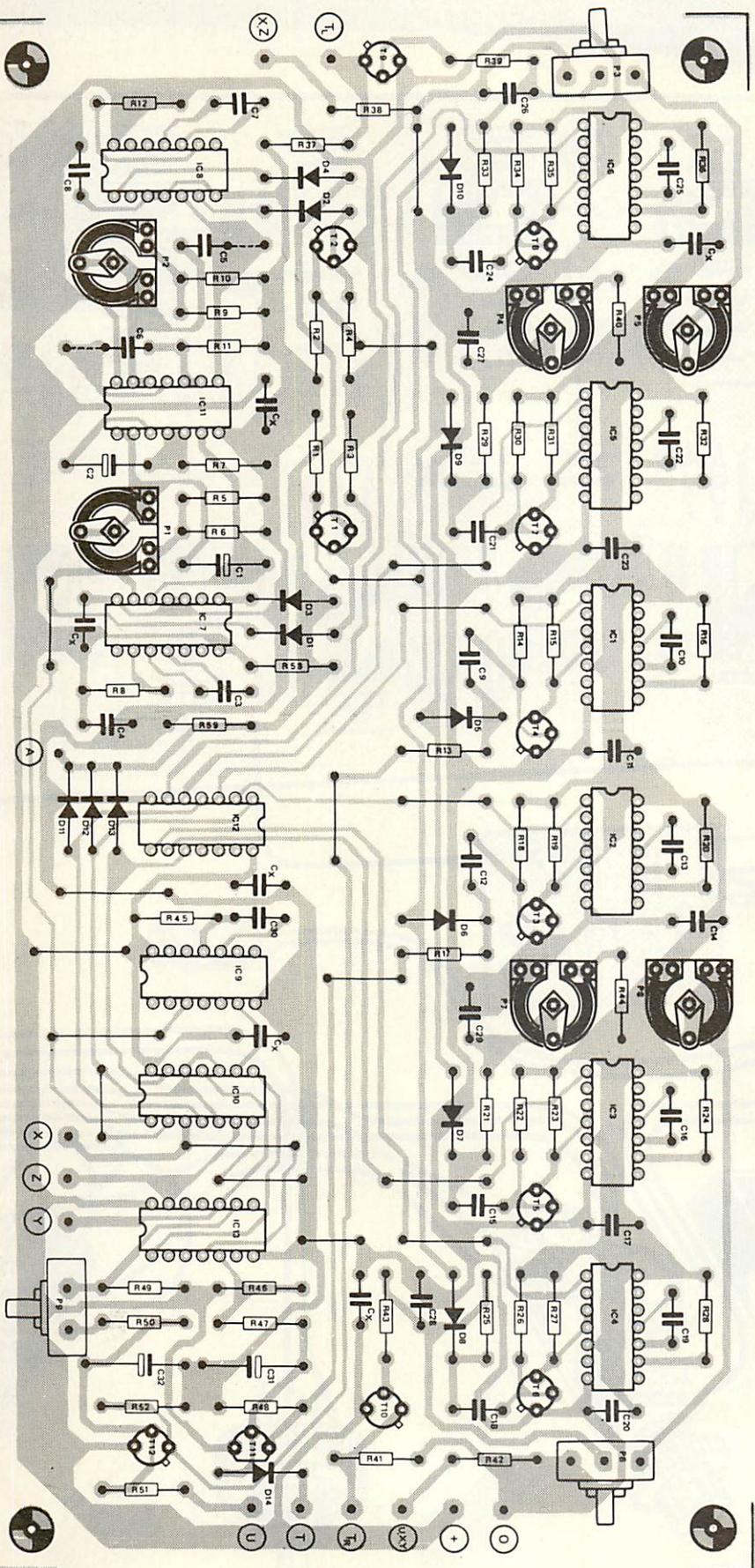


possible to make the ball service dependent upon the bat position at the time of service, though not coincident with it.

Service is accomplished as follows: for a service by the left-hand player the

4-pole switch S1 is closed. This produces several results. Firstly points X and Z are connected to ground via R38. This clears FF1 and presets FF2 so that when the ball is served it will travel upwards and to the right.

7



Point U (R51) is connected to positive supply, thus charging C32 rapidly and holding the ball off the left-hand side of the screen. Point T (cathode of D14) is connected to the emitter of T9, whose base is fed via R39 from P3 (left-hand

bat control). The voltage on C31 is thus constrained to slightly above the emitter voltage of T9, thus determining the vertical position from which the ball will start. When the switch is released the constraints on C31 and C32 are released

so the ball travels in a direction determined by the states of FF1 and FF2 (i.e. up and to the right). Service by the right-hand player operates, so to speak the same way but backwards, i.e. pushing S2 grounds point X so that the ball still travels upwards. However, point Y is grounded so that the ball travels to the left, and point U is grounded to discharge C32 so that it starts from the right. The vertical starting position is determined by the emitter potential of T10.

**Modulator and oscillator**

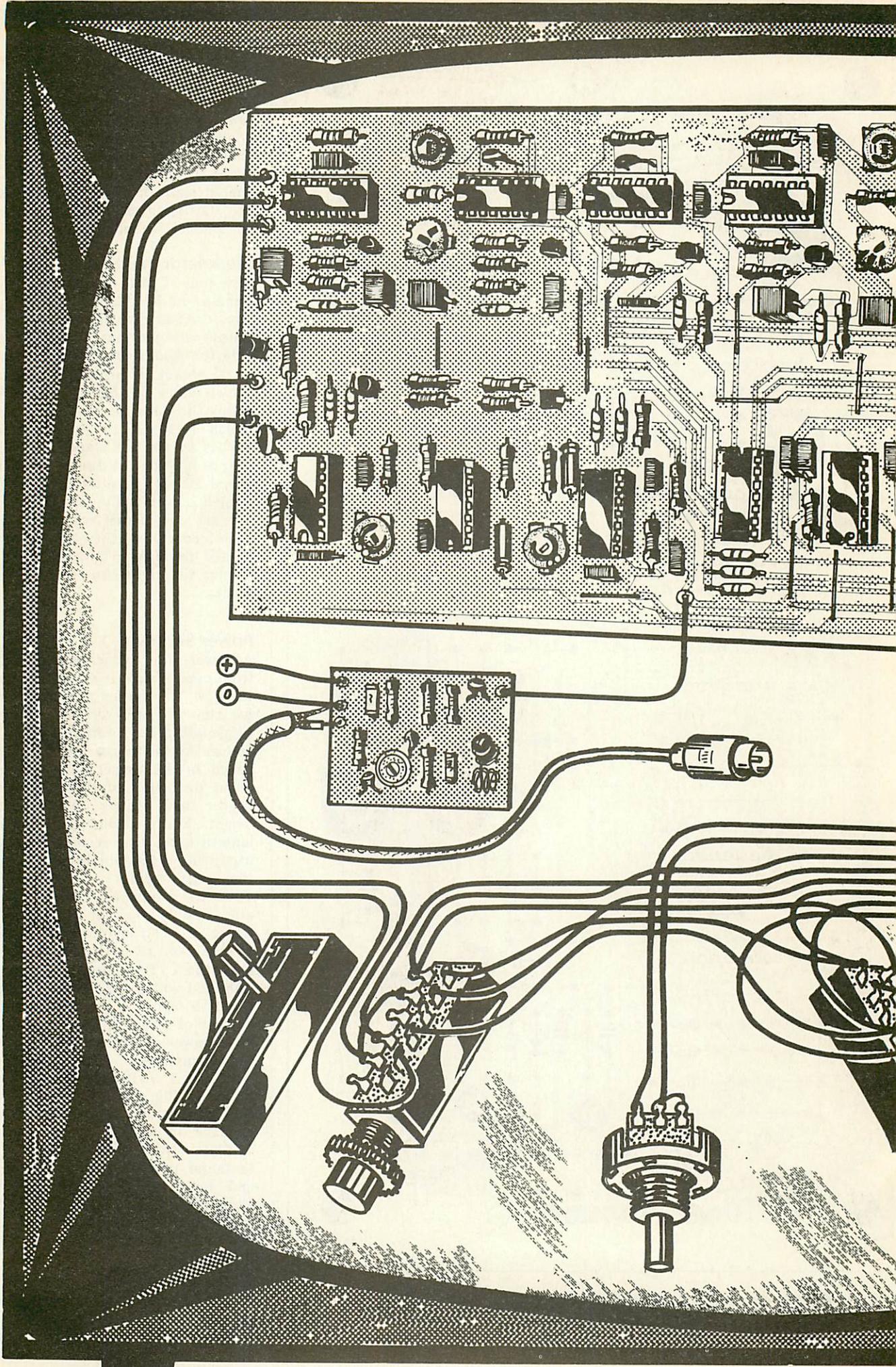
The only part of the circuit which remains to be described is the modulator/oscillator which converts the video output at point A into a VHF signal suitable for feeding direct into a television aerial socket. This part of the circuit is shown inset in figure 3. An AF239 forms the basis of the oscillator circuit which is tuned to the required frequency by the coil L and C36/C37. The output may be fed direct into an unbalanced 50 - 75 Ω coaxial cable terminating in a normal TV coax plug, or if the TV has continental type 240 - 300 Ω twin feeder input then the output must be fed through an inverse balun transformer before feeding into the 300 Ω feeder.

**Power Supply**

A power supply which is absolutely free from mains ripple is absolutely essential for the TV Tennis game. The reason for this is fairly obvious. Any mains ripple will cause a variation in the input voltages to the trigger delay circuits, and hence in the trigger delays. This produces distortion of the picture as the trigger delay varies down the screen height. For portable operation a 6 V lantern battery or accumulator may be used, with a decoupling capacitor across the supply pins on the board (say 1000 μ), whilst for mains only operation the 5 V power supply shown in figure 4 is strongly recommended. It is based on an integrated circuit regulator the L129. This IC will provide a stabilised voltage of 5 V from inputs up to 20 V and will supply a maximum current of 600 mA. However, to minimise power dissipation within the IC it is recommended that a transformer with a 6.3 V RMS secondary voltage be used. This will give a D.C. input to the IC of about 9 V. The bridge rectifier is made up of 4 1-amp diodes such as 1N4001. Note that C3 should be a tantalum type to reduce output noise and any tendency to R.F. instability. Components D1, D2, R1 and R2 correspond with figure 3a.

**Construction and adjustment**

The p.c. board and component layout for the VHF oscillator are given in figure 5, for the main board in figures 6 and 7, and for the power supply in figure 8. A point-to-point wiring diagram is given in figure 9. Slider poten-



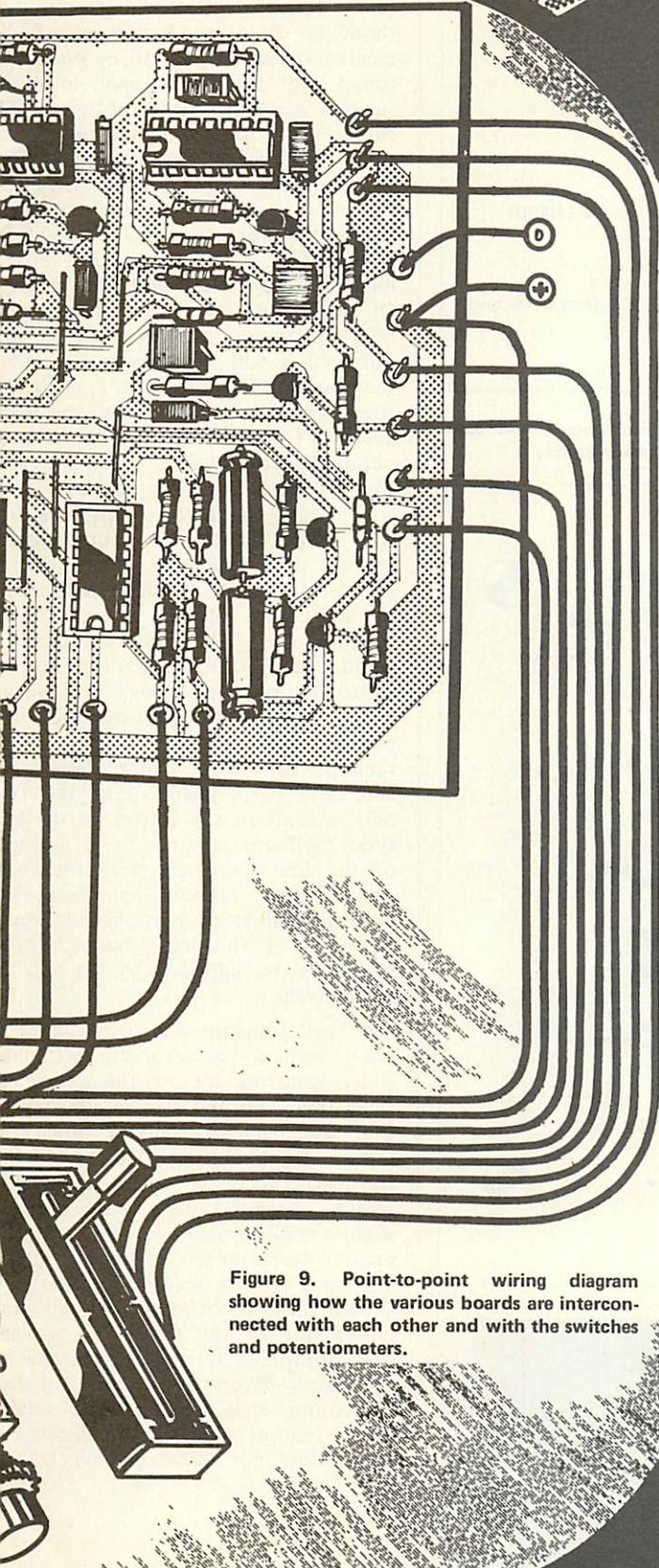
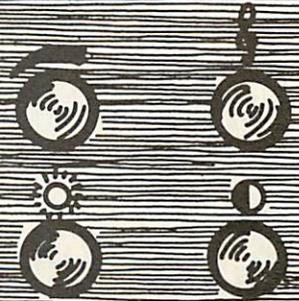
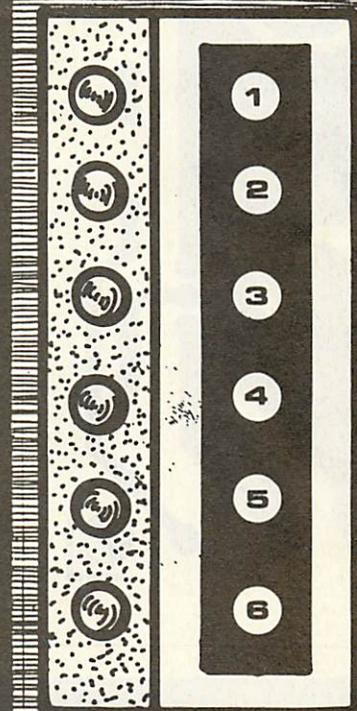


Figure 9. Point-to-point wiring diagram showing how the various boards are interconnected with each other and with the switches and potentiometers.



tiometers are used for the bat controls as these give easier control than rotary types and are sufficiently robust for domestic use. The oscillator is mounted on a separate board as it must be housed in a completely screened box to avoid radiated interference and to minimise pickup of other transmissions. A small diecast or pressed aluminium box with a lid is suitable. The main board housing should also be a metal box. Having checked that the circuit is correct and that the power supply is giving the correct voltage before connecting it to the unit, power can then be applied and the output of the VHF oscillator plugged into a TV set. Due to the harmonics generated extending into the hundreds of MHz the unit will function on both VHF and UHF although the line oscillator frequency is of course different for 405 and 625 line reception. Initially all the potentiometers should

#### Parts list for figures 4 and 8

##### Resistors:

R1, R2 = 470  $\Omega$

##### Capacitors:

C1 = 470  $\mu$ /16 V

C2, C4 = 100 n

C3 = 10  $\mu$ /6 V (tantalum)

##### Semiconductors:

D1 = DUS

D2 = 4.7 V zener

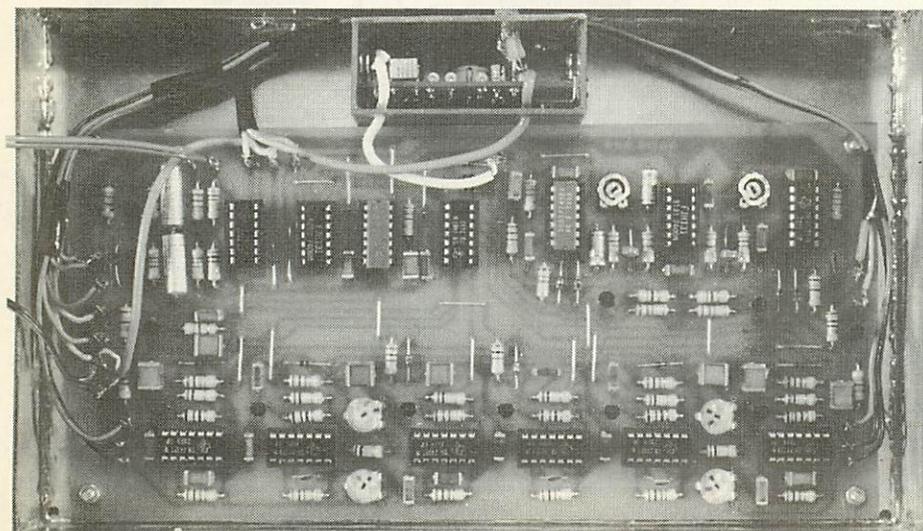
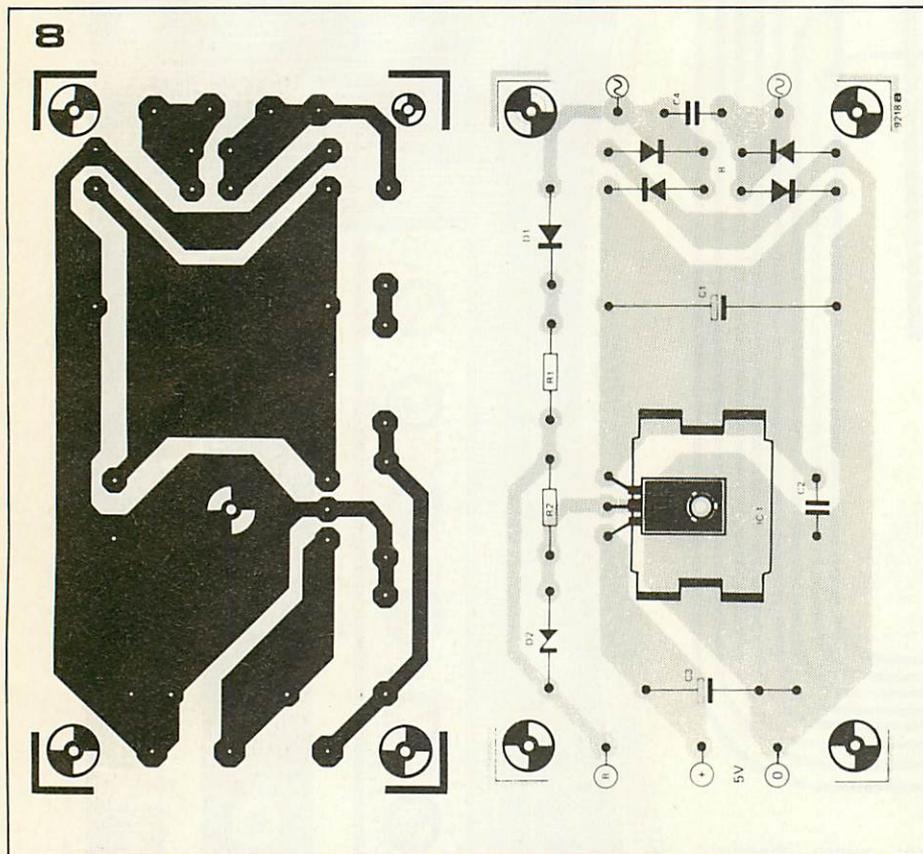
B = Bridge rectifier, or 4 x 1N4001

IC1 = L129

##### Sundries:

Transformer, 6.3 ... 8 V (r.m.s.) secondary

Figure 8. Printed circuit board and component layout for the power supply.



be set at the middle of their travel. If an oscilloscope is available the waveform at point A can be checked, if not, then proceed as follows. For VHF operation the TV set should be tuned to channel 5 or 9, though with pushbutton tuning there is often no indication of the channel the set is tuned to, so it must be tuned over the entire band until the signal is picked up. By adjusting the tuning and C36 it should be possible to tune in the signal. At first the picture will be rather chaotic as the field and line sync oscillators are not running at the correct frequency. By adjusting L1 it should be possible to obtain vertical lock, i.e. the picture will stop 'rolling'. Of course with mains field sync there is no adjustment and if lock is not obtained it will be necessary to adjust the frame hold control on the TV set. It may be found that, due to the tolerances of C1 and C2 it is not possible to obtain the correct field sync frequency. The oscillator may run at 25 Hz, in which case the picture will lock but will jitter considerably. In this case C1 and C2 should be reduced to 2  $\mu$  2. It may be found that a black bar appears in the centre of the screen. This is because the field sync oscillator is running at 100 Hz, and P1 should be adjusted until normal lock is obtained. Having obtained vertical lock the picture will probably consist of a random pattern of white dashes. L1 can now be adjusted until the two bats appear on the screen. If the line sync oscillator is tuned to a multiple of the line frequency then four bats may appear. Having obtained the correct number of bats the horizontal positions of the left- and right-hand bats may be adjusted by P4 and P5 respectively.

The final adjustment is to the range of the vertical bat controls. With the slider controls set to the centre of their travel P5 and P8 are adjusted so that the bats are halfway down the screen. It should now be possible to traverse the bats over the entire screen height, and some further slight readjustment of P5 and P8 may be necessary to achieve this.

The unit is now ready for use and it should be possible to serve a ball from either side of the screen by pressing the appropriate service button. Due to the simple nature of the circuit it may be found that pressing the service button causes slight picture jitter, but this should not prove inconvenient in practice.

# frequency counter

Logic IC's are nowadays so cheap that it is possible to build a digital frequency counter for a very small outlay. The circuit described here is based on the popular 74 TTL logic family. The first part deals with the basic counter, and in a subsequent article additions to the instrument will be described.

**Specification**

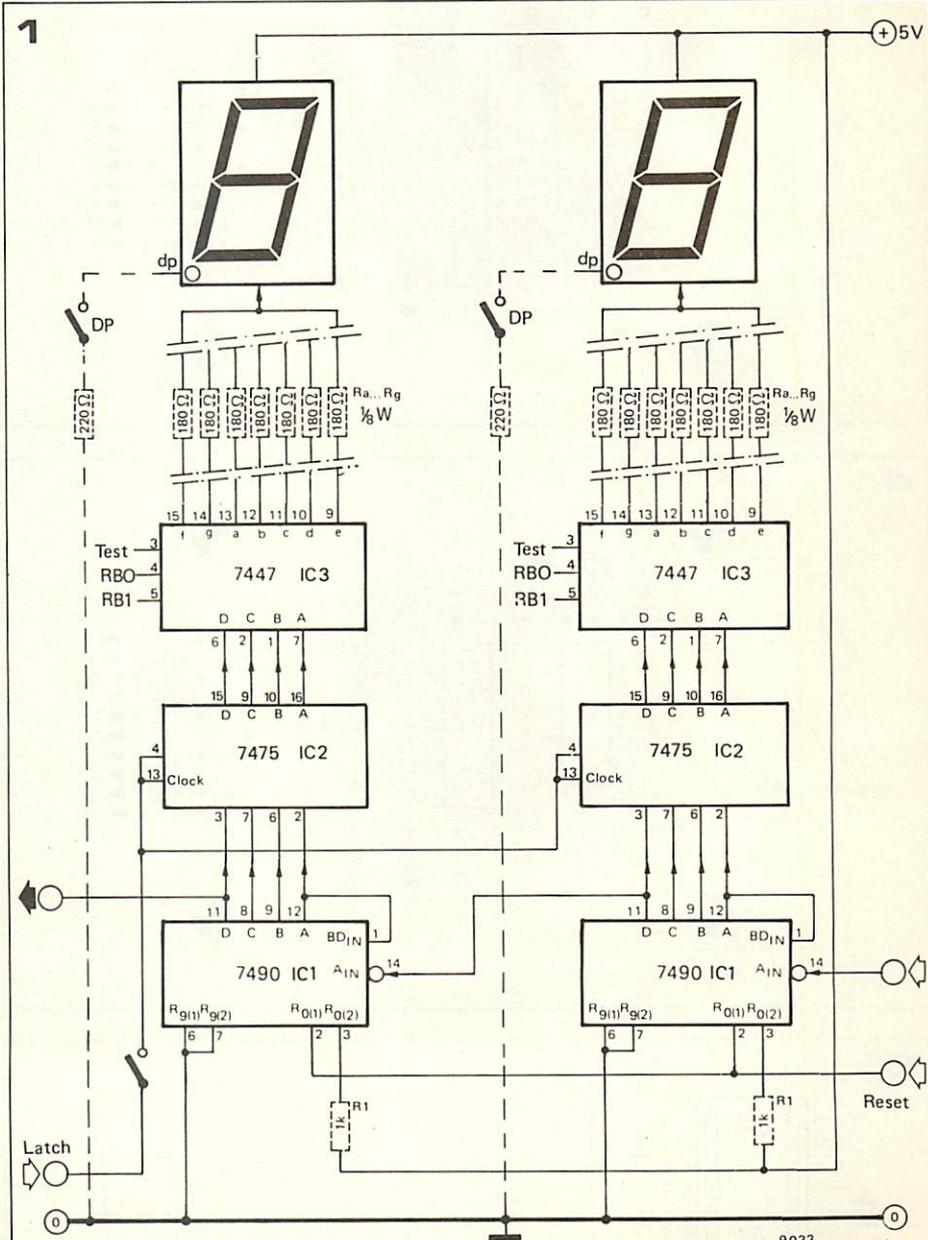
Input sensitivity (frequency measurement)	1.7 V p-p.
Input sensitivity (period measurement)	2.6 V p-p.
with an input risetime of 0.5 $\mu$ s/V.	
Maximum input frequency	18 MHz.

In its basic form the instrument is a six-digit frequency/period meter. The basic counter/latch/display is shown in figure 1, which is the circuit of two stages of the counter, showing how the 7490's are cascaded, and how the interconnections between the latch and reset inputs are made. The segment series resistors are shown dotted, as the circuit may be used with either Minitron or LED displays, and series resistors are not required with Minitrons.

A p.c. board for one stage of the counter/latch/display decoding is given in figure 2. Six of these boards are required for the six-digit counter. The displays are all mounted on a single board to which the counter boards are wired, either with wire links, as in figure 3, or if LED displays are used, via segment resistors, as in figure 4.

Figure 5 shows the pinout and voltage/current curve for a Minitron display type 3015F. Note that for use with a 7447 decoder the points shown as around are in fact commoned to +5 V.

A p.c. board for use with Minitron displays is shown in figure 6, and the component layout in figure 7, showing the connections to a counter board.



Parts list for figure 1

- IC's:  
 IC1 = 7490  
 IC2 = 7475  
 IC3 = 7447

- Resistors:  
 R1 = 1 k  
 Ra ... Rg = 180  $\Omega$  (LED display only)

Figure 1. Two stages of the counter/latch/display circuit, showing how the counters are cascaded.

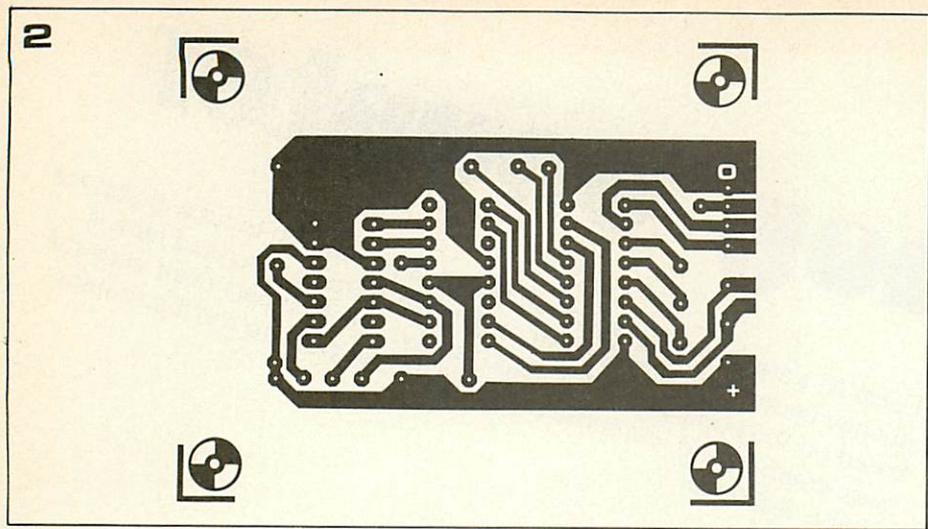


Figure 2. P.c. board for one decade of counter, latch and display driver.

Figure 3. Component layout for figure 2 using Minitron displays.

Figure 4. Component layout for figure 2 showing segment resistors for LED displays.

Figure 5. Pinout and characteristics of Minitron.

Figure 6. P.c. board for Minitron display.

Figure 7. Component layout for Minitron display.

Figure 8. Pinouts of three popular LED displays.

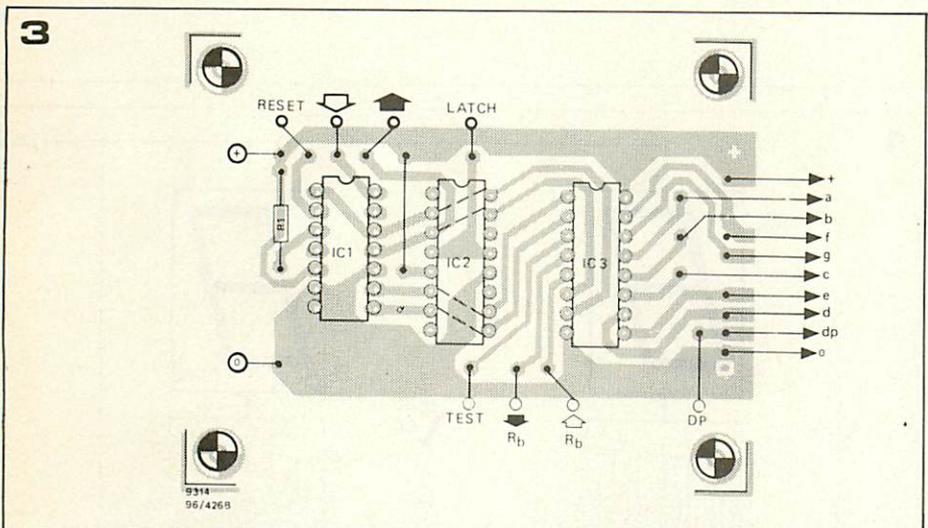
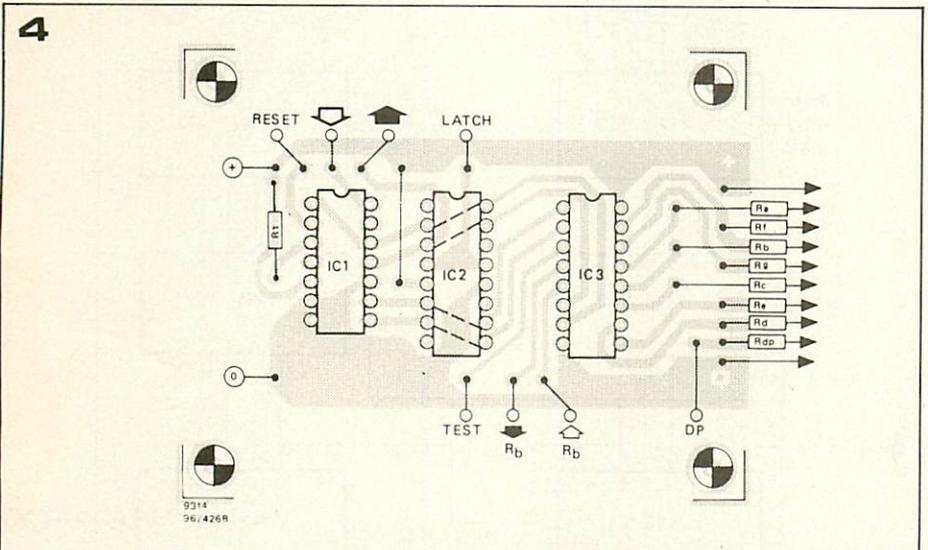


Figure 9 shows the corresponding board for use with LED displays. Most common anode LED displays are pin compatible with respect to the cathode (segment) connections, but some types have multiple anode connections (usually pins 3 and 9). These are catered for on the board, but if a display is used that does not have anode connections to these pins it may or may not be necessary to cut them off, depending on whether or not they are N.C. (no connection).

The pin connections of three popular LED displays are given in figure 8. For further data on common-anode LED displays see Elektor No. 3 page 451.

Photographs 1 and 2 show the general appearance of the display/counter board assembly, and also how the segment resistors are soldered to the back of the display board when using LED displays.



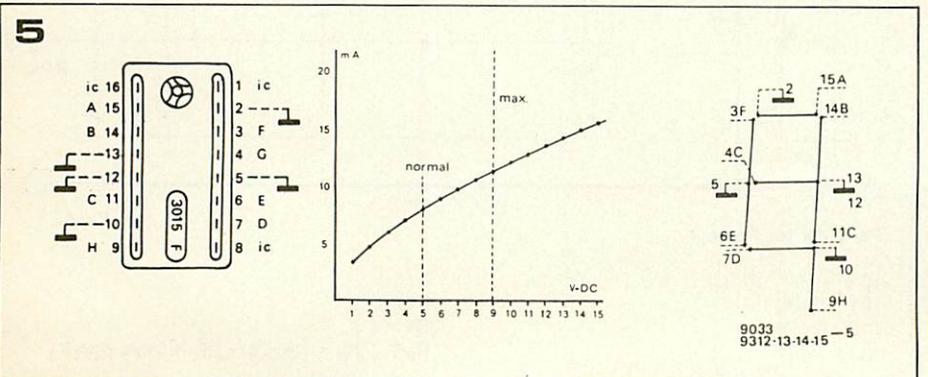
**Control logic**

To make the decade counter just described function as a frequency counter various control signals must be applied to it. Firstly, the pulses to be counted must be gated into the first stage of the counter. Secondly, after the counting period has ended the count must be stored in the latch. The counter must then be reset ready for the next count. All these functions are performed by the control logic, the circuit of which is given in figure 10.

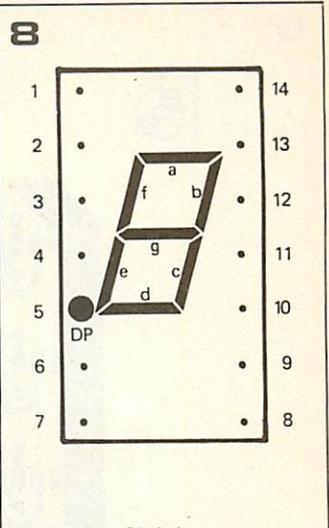
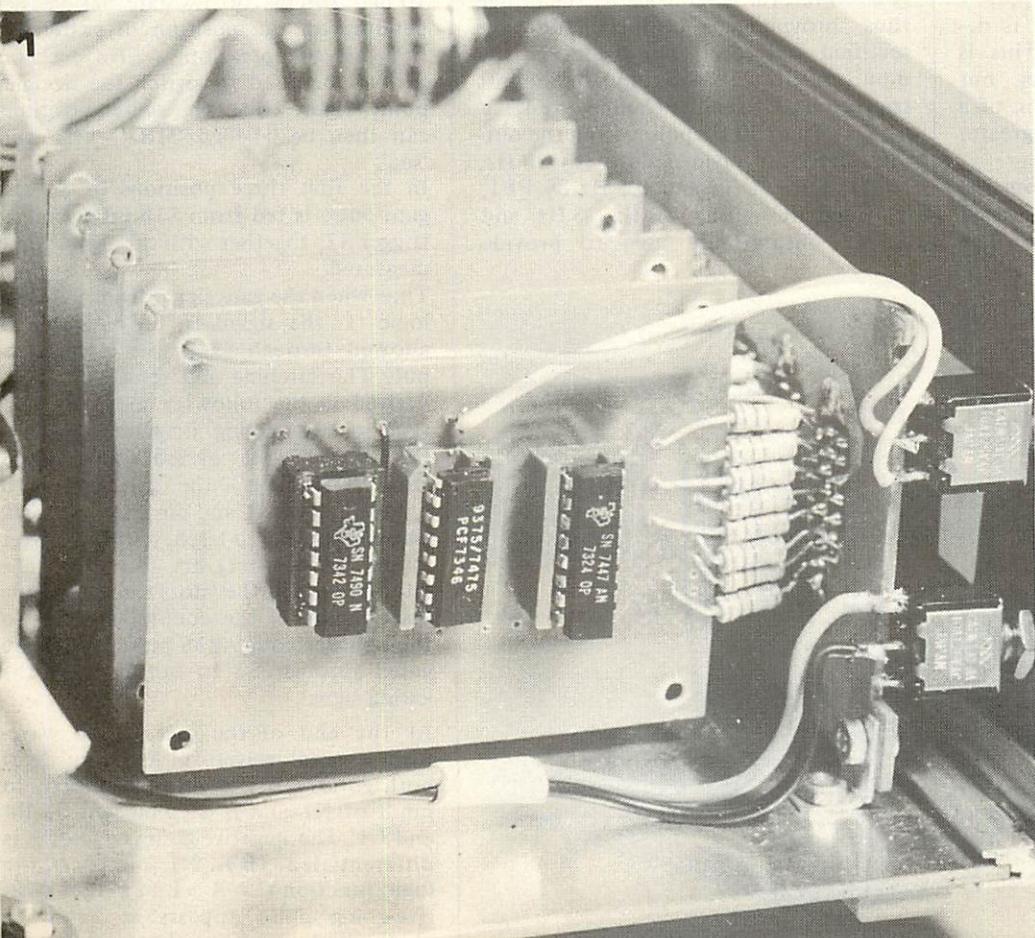
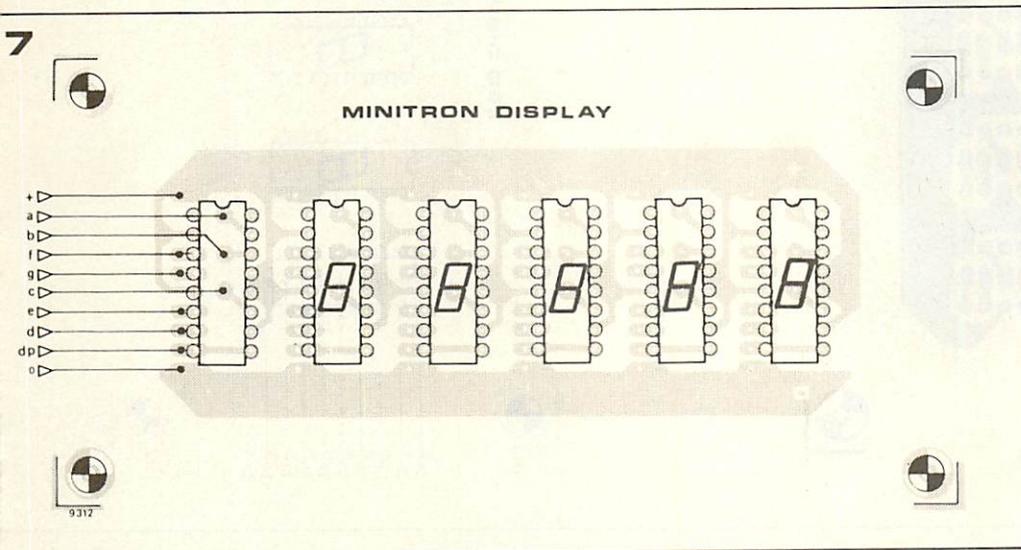
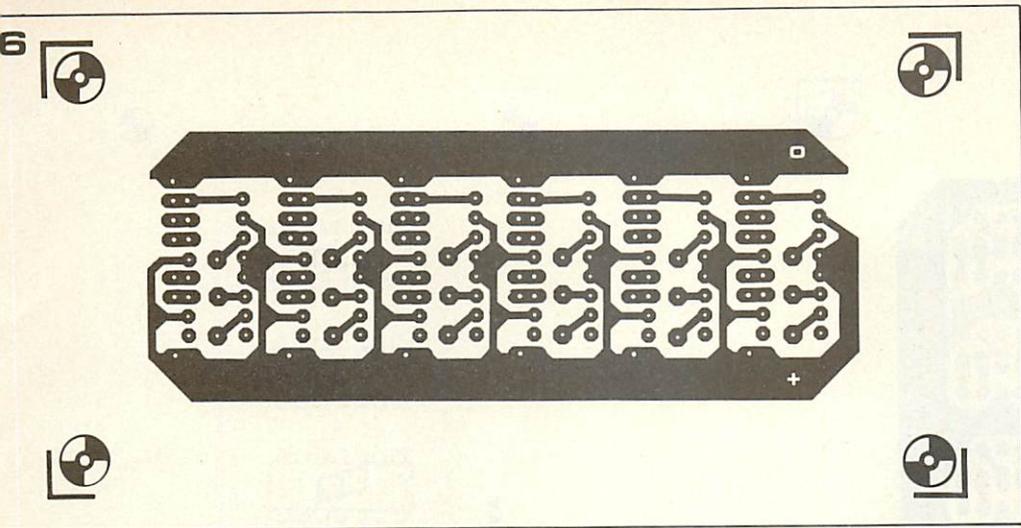
The counter will operate in two basic modes, frequency and period. In the frequency mode incoming pulses are counted for a period of time dependent upon the counter gate period. Thus if the incoming frequency was 100 kHz and the gate period 1 s then the count displayed would be 100000.

In the period mode the internal frequency reference of the counter is itself counted and is gated by one cycle of the incoming signal. Thus, if the internal reference frequency was 100 Hz, and the signal to be measured had a period of 1 s, then the count displayed would be 000100. Of course the decimal point on the display board can be shifted so that this could be displayed as 1.00 (see below).

The control logic operates as follows. I



9033 9312-13-14-15-5



Opcoa SLA 1

Pin

- 1 Cathode a
- 2 Cathode f
- 3 NC
- 4 NC
- 5 NC
- 6 Cathode DP
- 7 Cathode e
- 8 Cathode d
- 9 NC
- 10 Cathode c
- 11 Cathode g
- 12 NC
- 13 Cathode b
- 14 Common Anode

Hewlett-Packard

Pin 5082-7730

- 1 Cathode a
- 2 Cathode f
- 3 Common Anode
- 4 No pin
- 5 No pin
- 6 Cathode DP
- 7 Cathode e
- 8 Cathode d
- 9 NC
- 10 Cathode c
- 11 Cathode g
- 12 No pin
- 13 Cathode b
- 14 Common Anode

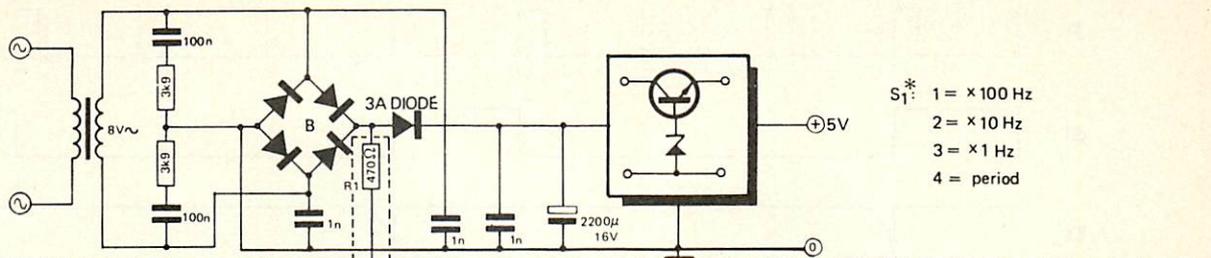
Data Lit 707

Pin

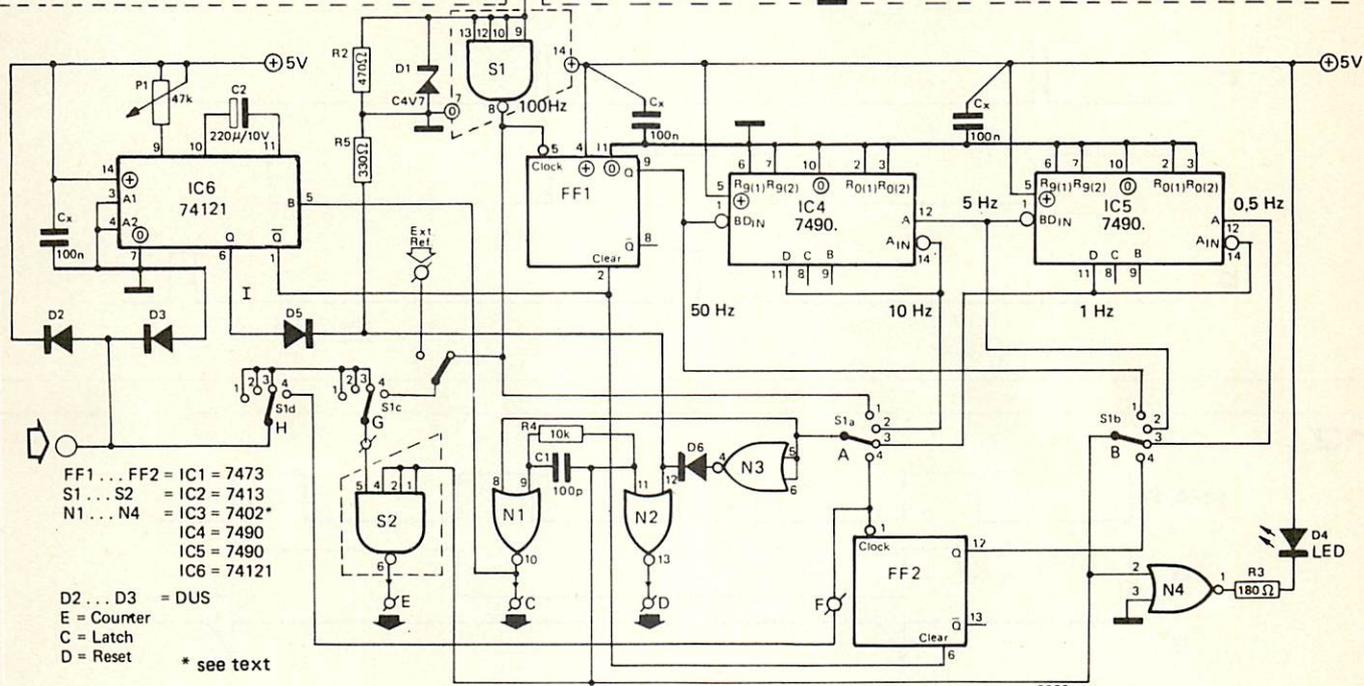
- 1 Cathode a
- 2 Cathode f
- 3 Common Anode
- 4 NC
- 5 NC
- 6 Cathode DP
- 7 Cathode e
- 8 Cathode d
- 9 Common Anode
- 10 Cathode c
- 11 Cathode g
- 12 NC
- 13 Cathode b
- 14 Common Anode



10a



S<sub>1</sub>\*: 1 = × 100 Hz  
 2 = × 10 Hz  
 3 = × 1 Hz  
 4 = period



FF1...FF2 = IC1 = 7473  
 S1...S2 = IC2 = 7413  
 N1...N4 = IC3 = 7402\*  
 IC4 = 7490  
 IC5 = 7490  
 IC6 = 74121  
 D2...D3 = DUS  
 E = Counter  
 C = Latch  
 D = Reset  
 \* see text

Figure 9. P.c. board and component layout for LED display.

Figure 10. Circuit diagram of control logic.

the 'enable data entry' mode and thus storing the count. This pulse also triggers the monostable IC6, which performs several functions. Firstly, its Q output holds the input to S1 high, thus blocking the 100 Hz pulses to FF1. It also holds pin 12 of N2 high, so the output remains low. The  $\bar{Q}$  output clears FF1. When the monostable resets the timebase will restart. The next positive transition of the A signal will be inverted by N3, and the input (pin 12) of N2 will be pulled low by R5. Since the other input is connected to the B signal, which is already low, the output of N2 goes high for the duration of the positive A pulse, thus resetting the counter. When the B signal goes high again the counter commences another count and the sequence repeats. D4 lights when the gate is open. The pulse length of the monostable IC6 can be varied by P1. It is apparent that this pulse length determines the time for which the timebase is disabled, and hence the interval between counts. This facility is useful, as with a short count interval the continual variation in the last digit can be annoying. A longer count interval will alleviate this. On the other hand, when a rapid succession of measurements is to be taken then a short count interval is useful.

**Period Measurement**

To measure the period of the incoming

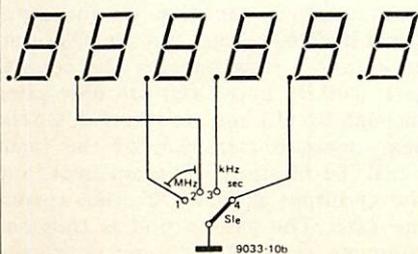
**Parts list for figure 10**

- Resistors:**  
 R1, R2 = 470 Ω  
 R3 = 180 Ω  
 R4 = 10 k  
 R5 = 330 Ω  
 P1 = 47 k, lin.
- Capacitors:**  
 C1 = 100 p  
 C2 = 220 µ, 10 V  
 C<sub>x</sub> = 100 n
- Semiconductors:**  
 D1 = zener 4.7 V, 250 mW  
 D2, D3, D5, D6 = DUS  
 D4 = LED

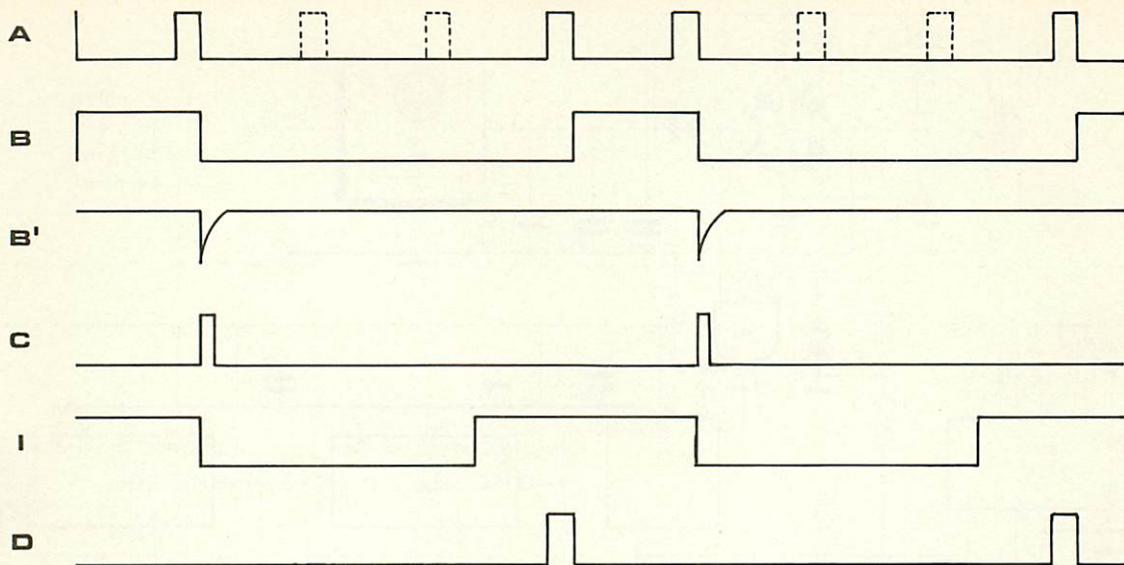
- IC's:**  
 IC1 = 7473  
 IC2 = 7413  
 IC3 = 7428 (7402)  
 IC4, IC5 = 7490  
 IC6 = 74121

- Sundries:**  
 S1 = 4-pole 4-way switch (or 5-pole 4-way, see text)

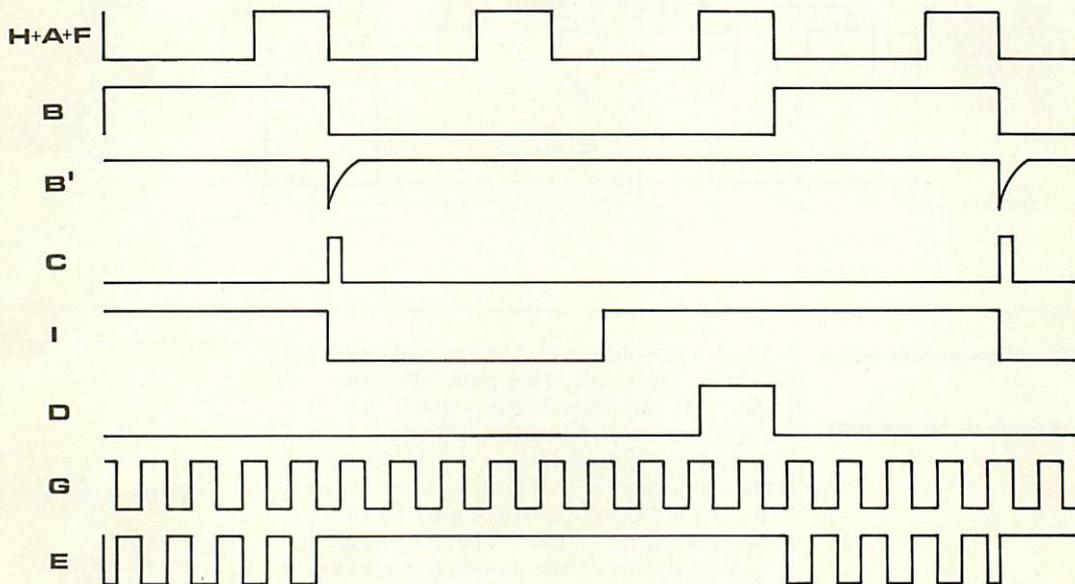
10b



11

9312-13-14-15 — 11  
9033

12

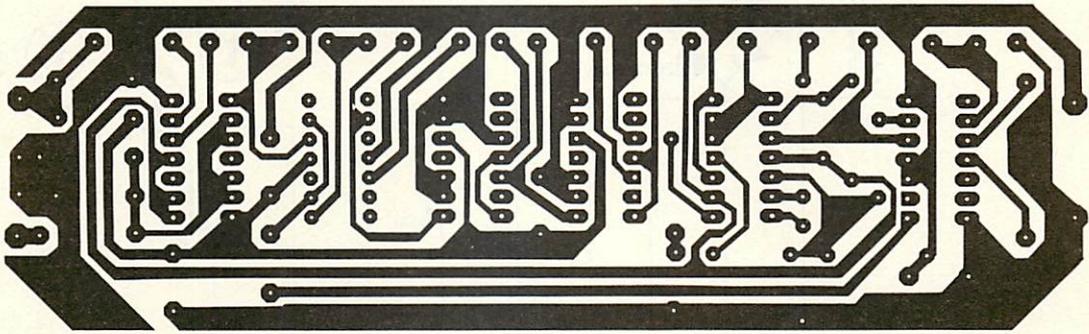
9312-13-14-15 — 12  
9033

3



waveform the 100 Hz reference is counted whilst the gate, latch and reset functions are derived from the signal to be measured. To do this the switch S1 is set in position 4. This disables the time base, connects the gate input of S2 to the Q output of FF2 and connects the 100 Hz signal to the other input. It also connects the latch circuitry input A to the incoming signal. The sequence of operations is thus as follows: on the first negative transition of the input signal H FF2 clocks and its Q output goes to '1' thus opening the counter gate. 100 Hz pulses (G) are now gated through S1 (E) and are counted. On the next negative transition of the input signal the flip-flop FF2 again clocks and the Q output goes to '0', thus closing the gate. The gate period is thus one complete cycle of the input waveform. The input waveform drives the latch and reset circuitry in a similar manner to

13



14

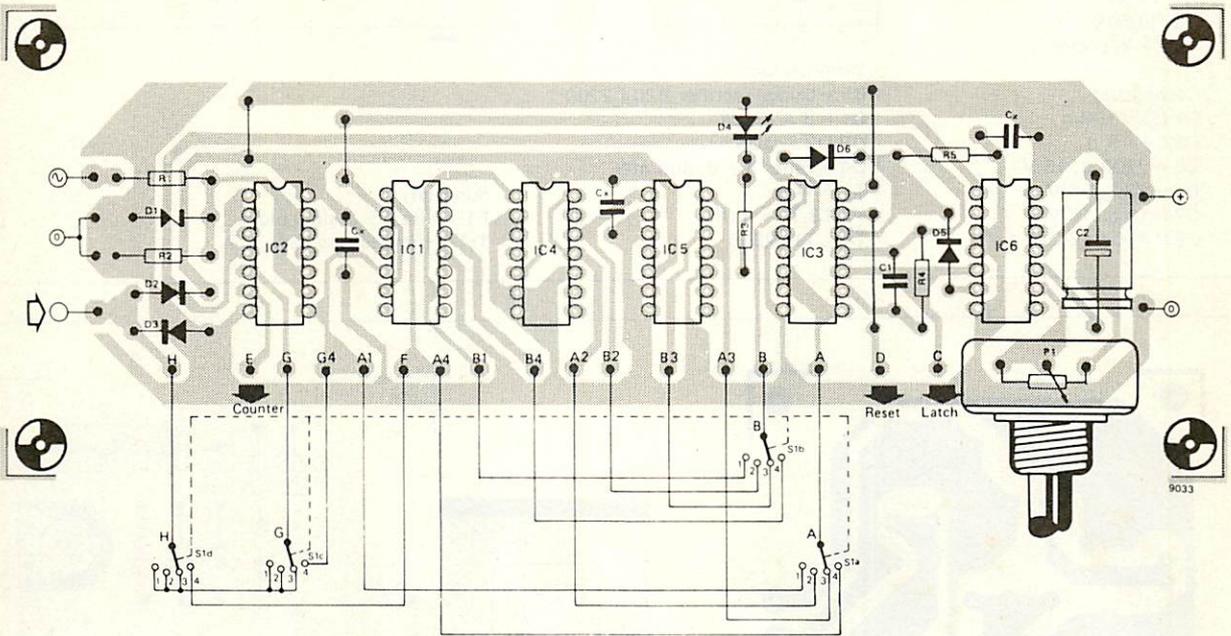


Figure 11. Timing diagram of counter in frequency measuring mode.

Figure 12. Timing diagram of counter in period measuring mode.

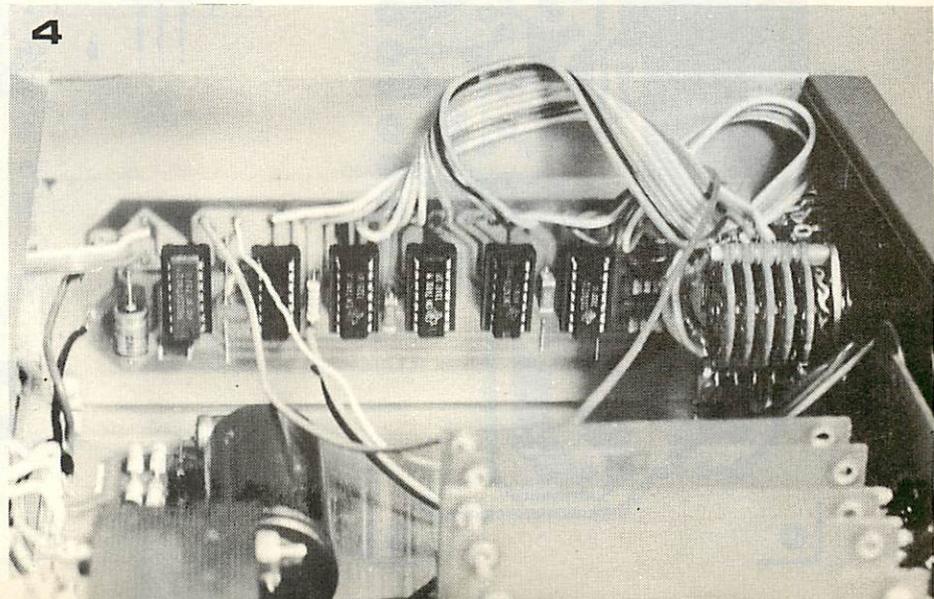
Figure 13. P.c. board for control logic.

Figure 14. Component layout for control logic.

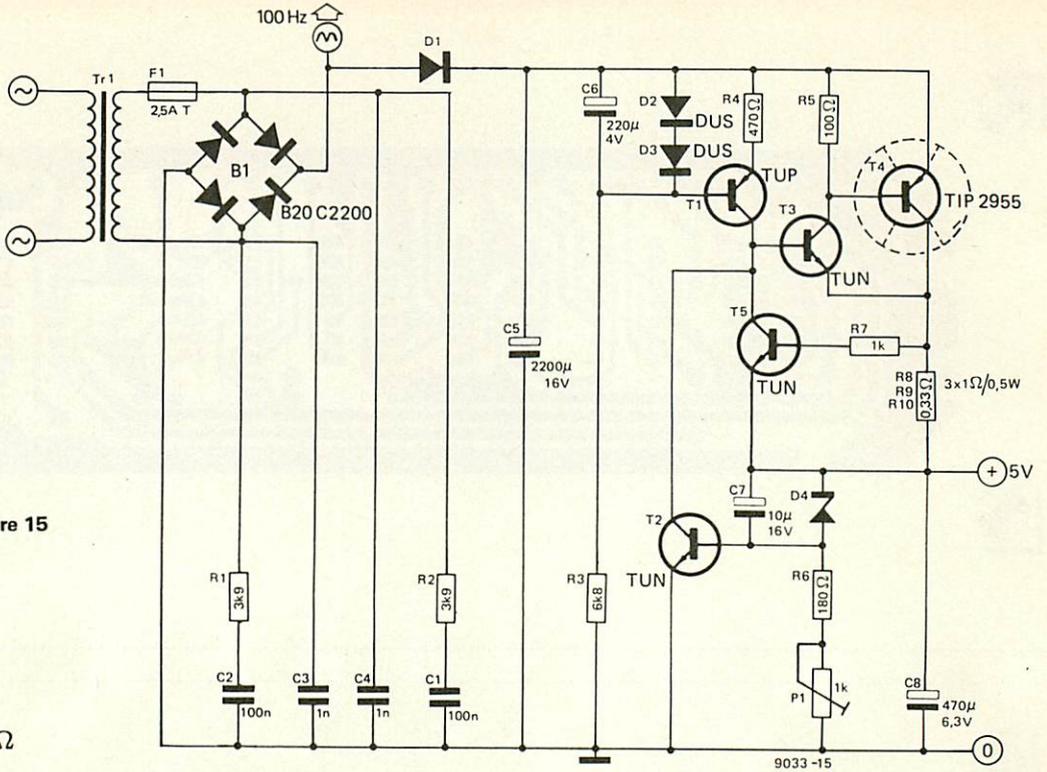
that for a frequency measurement, and the timing diagram is shown in figure 12. Of course, the A signal is now the input signal, and the B signal is the Q output of FF2.

With a 100 Hz reference frequency and

4



15



Parts list for figure 15

Resistors:

- R1, R2 = 3k9
- R3 = 6k8
- R4 = 470 Ω
- R5 = 100 Ω
- R6 = 180 Ω
- R7 = 1 k
- R8, R9, R10 = 1 Ω
- P1 = 1 k, preset

Capacitors:

- C1, C2 = 100 n
- C3, C4 = 1 n
- C5 = 2200 μ, 16 V
- C6 = 220 μ, 4 V
- C7 = 10 μ, 16 V
- C8 = 470 μ, 6.3 V

Semiconductors:

- B1 = bridge rectifier B20 C2200
- D1 = 3 A diode
- D2, D3 = DUS
- D4 = zener 4.7 V, 400 mW
- T1 = TUP
- T2, T3, T5 = TUN
- T4 = TIP 2955

Sundries:

- F1 = fuse 2.5 A slow blow
- Tr1 = transformer 12 V, 2 A

16

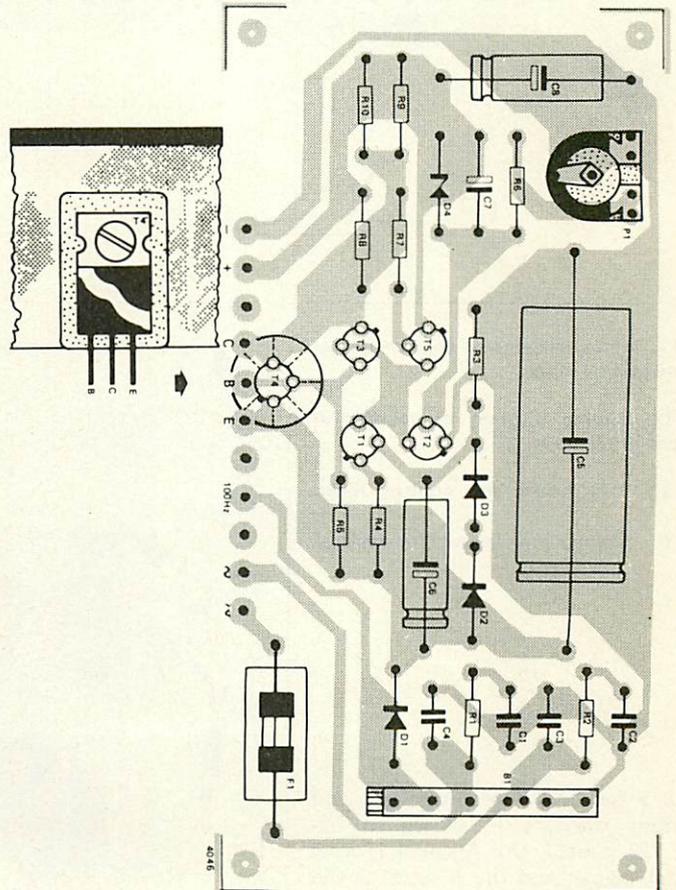
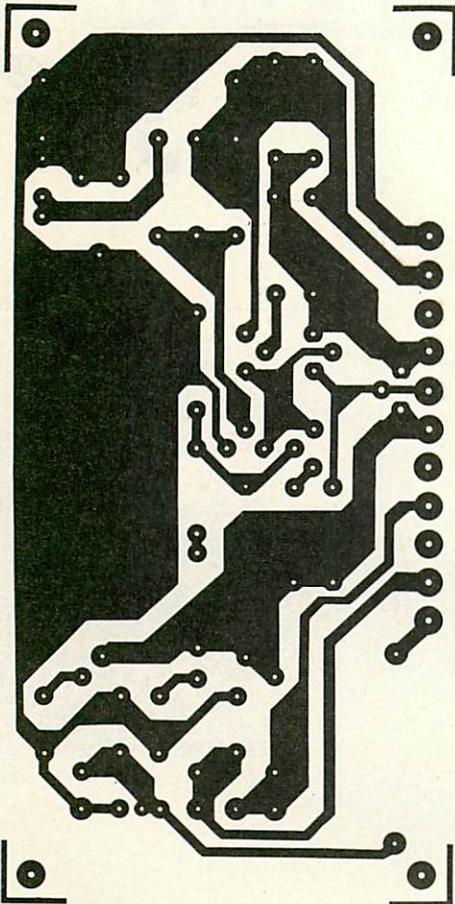


Figure 15. Power supply for frequency counter.

Figure 16. P.c. board and component layout of power supply.

the gate periods of 10 ms, 100 ms and 1 s the range of the instrument is limited. It is only possible to obtain a full-scale reading in the period mode when the period is 9,999.99 seconds. For a period of 1 s the display will be only 000100, a resolution of one part in a hundred. Clearly, for short period measurements a higher reference frequency is necessary to obtain a larger count and hence a better resolution. Provision is made for feeding in an external reference frequency by breaking the circuit at the point marked 'EXT REF'. In the frequency mode the maximum and minimum frequencies which can be measured are limited by the gate periods. For instance with a 1 s gate period a frequency of 100 Hz will only be measured with a resolution of one part in a hundred, whilst with a 10 ms gate period an input frequency of greater than 99.9999 MHz would cause the counter to overrange. However, since the upper frequency limit of the TTL counters used in the circuit is only 8 MHz anyway, this problem does not arise.

A printed circuit board and component layout for the control logic board are given in figures 13 and 14, showing the connections to the switch.

### Power supply

A suitable power supply for the frequency counter is shown in figure 15. This is well decoupled against mains-borne interference and has a 100 Hz output for the reference frequency. A board and component layout for the power supply are given in figure 16. As the complete frequency counter draws about 2 amps, the series regulator transistor T4 should be mounted on an adequate heatsink. If the unit is housed in an aluminium case then the back of the case should prove suitable.

In a future issue we shall be describing additions to the frequency counter, notably an input preamplifier to increase the input sensitivity.

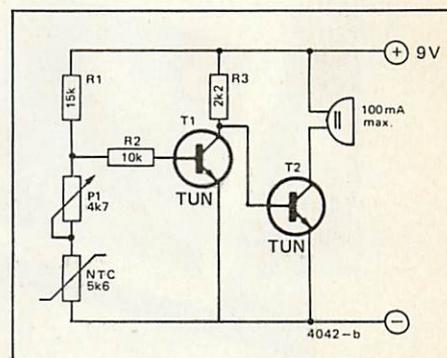
J.P. Kuhler jr.

## humming kettle

Those who have in the course of time lost the whistle of their domestic kettle and the unfortunate ones who do not possess a whistling kettle at all, who must boil water without the aid of an acoustic signal, are encouraged by the author not to resign themselves to this unsatisfactory situation. A very modest amount spent on components together with a little work puts a 'humming kettle' within everyone's grasp!

The circuit is so simple that further explanation is hardly necessary. As the temperature increases, the resistance of the NTC drops until at a certain moment (adjustable with P<sub>1</sub>) transistor T<sub>1</sub> cuts off, so that T<sub>2</sub> conducts and the buzzer is activated.

Of course the circuit must be mounted in, on, or in the immediate vicinity of the kettle.



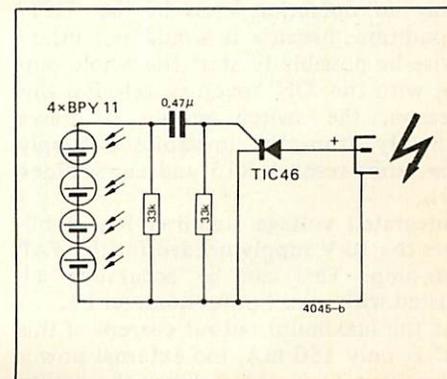
R. Bugge

## active flash slave

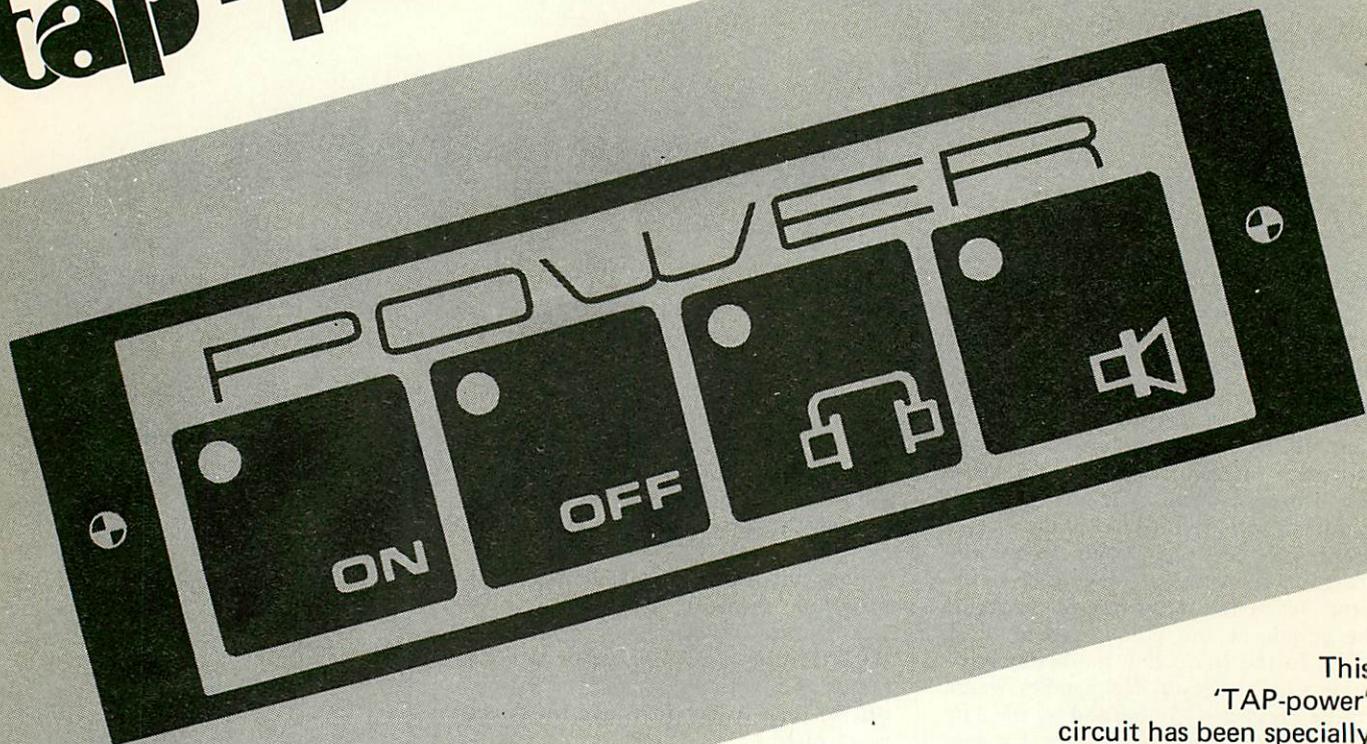
For those who have often been annoyed by badly illuminated flash photographs and also dislike the tangle of cables involved in using two flashguns, the flash slave is the only solution.

The author spent quite some time building several slave units before arriving at the design presented here, which has the advantages that it requires no separate supply voltage and that both electronic and ordinary flashguns can be operated. Four silicon photovoltaic cells (BPY 11) form a light sensor. Undoubtedly other types will do, too. The thyristor must be of a type with a very low firing voltage; the TIC 46 used here performs quite well. The circuit itself needs little comment: only that the polarity of the flash connection should be correct; the 'plus'

should be connected to the centre pin of the connecting cable. The circuit can best be housed in a small, transparent plastic box.



# tap - power



This 'TAP-power' circuit has been specially designed for the TAP preamp system.

It includes touch-controlled switches for turning the whole equipment on or off and for selecting the main power amplifiers or the headphone amplifiers, a power supply for the TAP pre-amp, simple headphone amplifiers and a disc preamplifier.

NAND gates N1, N2 and N3, N4 ( $IC_4 = CD4001$ ) make up two touch switches. Four LEDs are used to indicate the condition in which the system has been set; D2 = ON, D3 = OFF, D6 = headphones and D5 = power amplifier.

Because of the difference between this circuitry and the rest of the TAP system, construction is much simpler: instead of a diode matrix only two flip-flops are used here.

The power supply is split up into three sections: one for the touch switches, one for the rest of the TAP preamp and one for the disc preamplifier.

The supply for the touch switches must stay in operation even in the 'OFF' condition, because it would not otherwise be possible to start the whole outfit with the 'ON' touch switch. For this reason, the switch supply is drawn directly from the unregulated supply via series resistor R15 and zener diode D1.

Integrated voltage stabiliser  $IC_3$  stabilises the 10-V supply needed for the TAP pre-amp. This can be accurately adjusted with preset potentiometer P1.

As the maximum output current of this IC is only 150 mA, the external power transistor T1 is added. When the supply

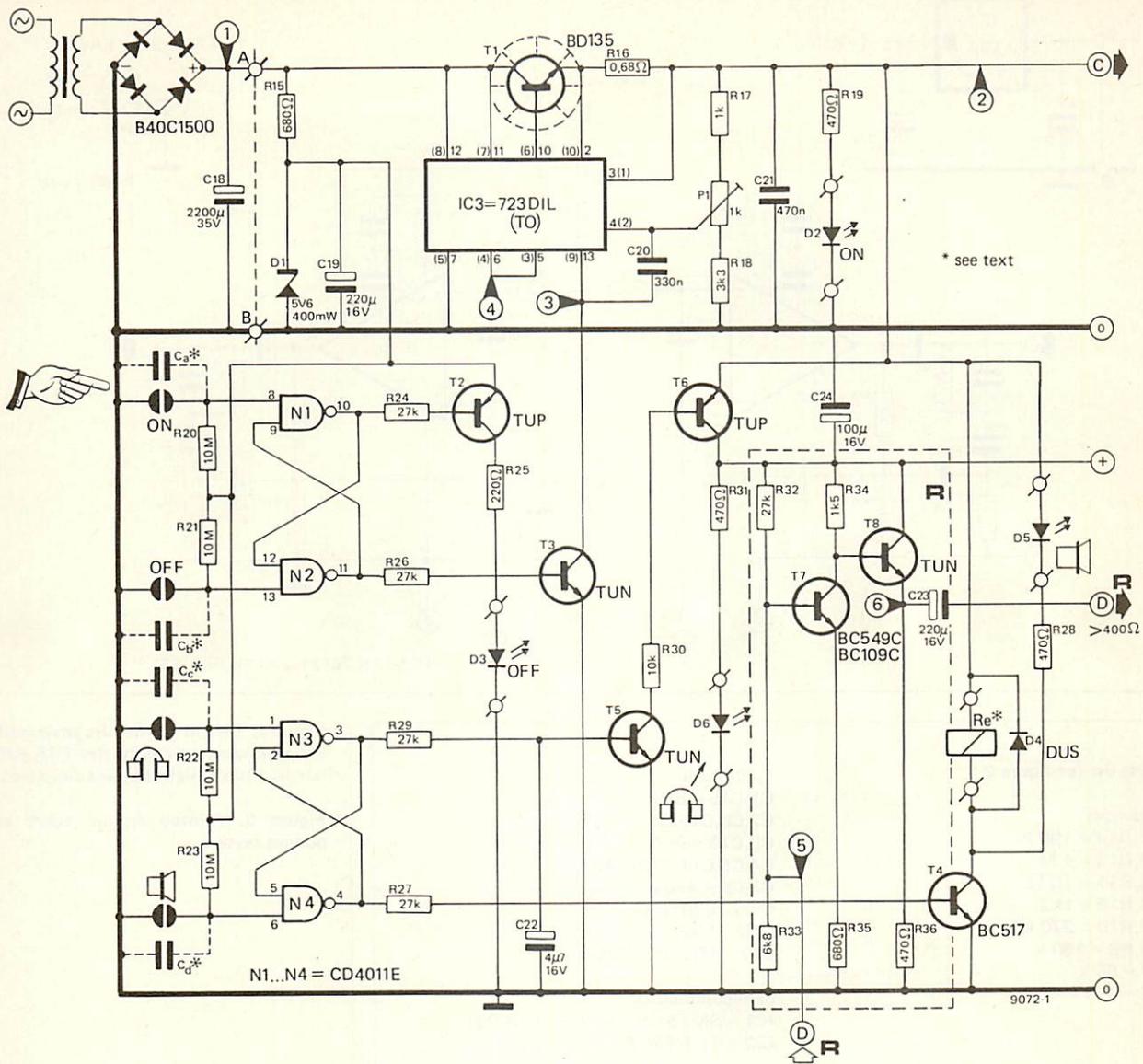
voltage is switched on with the 'ON' touch switch, the logic state prevailing at the output of gate N1 is '1', while it is '0' at the output of N2. Transistors T2 and T3 are therefore cut off, and the supply voltage becomes available at output C.

When the 'OFF' panel is touched, logic levels at the outputs of N1 and N2 are reversed, with the result that T2 and T3 turn on. The potential at pin 13 of  $IC_3$  is therefore pulled down almost to zero, so that the internal output transistors in the IC are cut off. The voltage at output C drops to 0 and the TAP preamp is turned off.

The flip-flop formed by N3 and N4 provides a changeover between headphones and the main power amplifier. When the output of N3 is at logic '1', transistors T5 and T6 turn on, switching on the headphone amplifier built around T7 and T8. This amplifier, including the associated components within the dashed rectangle in figure 1, is duplicated on the board for the left-hand headphone channel. Both amplifiers derive their supply from the collector of T6. The output of N4 is at logic '0'. Transistor T4 is cut off and relay Re is not energised. The relay contacts,

Figure 1. Circuit of the main power supply, the TAP switches for on/off switching and loudspeaker/headphone selection, and one of the headphone amplifiers.

1



**Parts list for figure 1**

- Resistors:**  
 R15, R35 = 680 Ω  
 R16 = 0.68 Ω  
 R17 = 1 k  
 R18 = 3k3  
 R19, R28, R31, R36 = 470 Ω  
 R20, R21, R22, R23 = 10 M  
 R24, R26, R27, R29, R32 = 27 k  
 R25 = 220 Ω  
 R30 = 10 k  
 R33 = 6k8  
 R34 = 1k5  
 P1 = 1 k

- Capacitors:**  
 C18 = 2200 µ/35 V  
 C19, C23 = 220 µ/16 V  
 C20 = 330 n  
 C21 = 470 n  
 C22 = 4µ7/16 V  
 C24 = 100 µ/26 V

- Sundries:**  
 Transformer = 240 V/16 V, 1 A (see text)  
 Bridge rectifier = B40C 1500  
 Relay Re = 10 V, 300 Ω (see text)

- Semiconductors:**  
 D1 = 5V6/400 mW  
 D2, D3, D5, D6 = LED  
 D4 = DUS  
 T1 = BD 135 (cooled)  
 T2, T6 = BC 177 (possib. TUP)  
 T3, T5, T8 = BC 107 (possib. TUN)  
 T4 = BC 517  
 T7 = BC 549 C, BC 109 C  
 IC3 = µA 723  
 IC4 = CD 4011

which switch the supply for the main power amplifiers on and off at the primary of the mains transformer for these amplifiers, stay open.

When the loudspeaker touch panel is touched the relay contacts close and the power amplifier is turned on: the headphone amplifier no longer gets a power supply because the logic '0' at the output of gate N3 cuts off transistors T5 and T6.

The disc preamplifier (figure 2) is the same as was described in the April 1975 issue of Elektor. Power supply for the

preamplifier is provided by the integrated stabiliser IC<sub>2</sub>. Points A and B are connected to the corresponding points in figure 1.

**Construction**

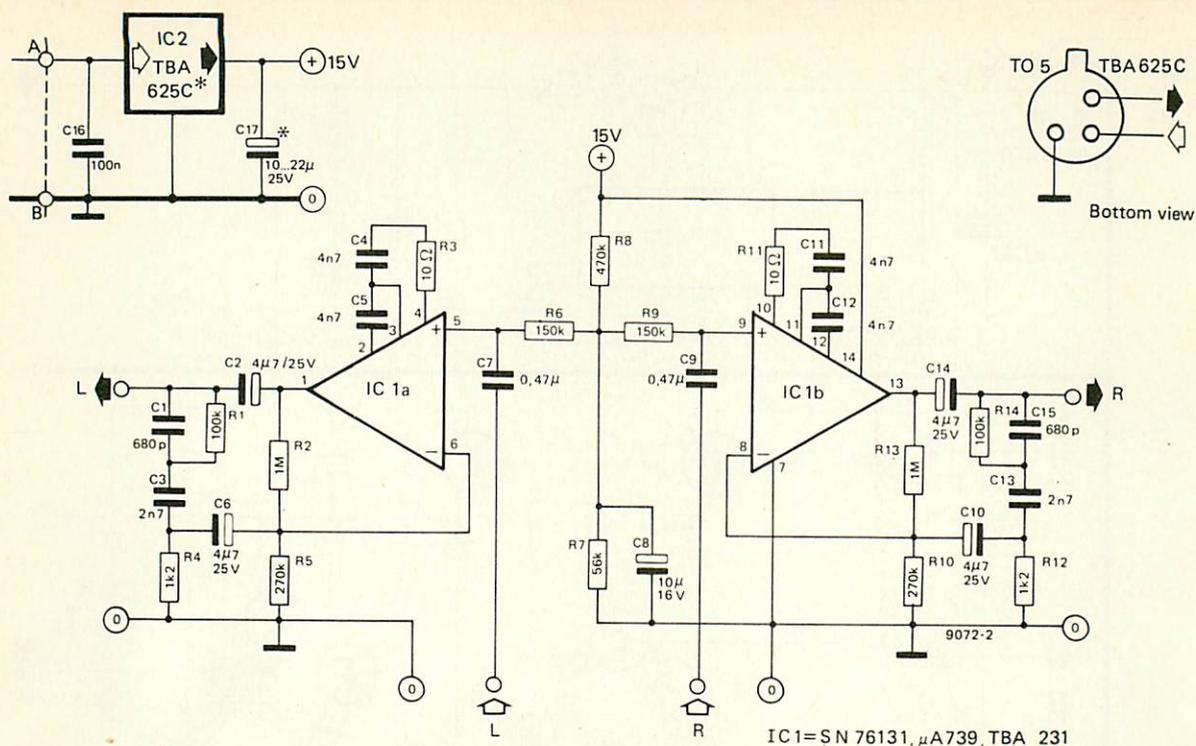
Current consumption of the touch-switching circuit is about 30 mA in the 'OFF' position. In the switched-on state, the maximum consumption with headphone listening is about 100 mA (not counting the TAP preamplifier, of course!). Including the TAP preamplifier, the maximum current consumption

is 320 mA when the headphone amplifiers are on and the volume control is at maximum.

Figure 1 shows six points at which the D.C. voltage can be checked. With the transformer secondary delivering 16 volts RMS and the TAP preamp not connected, the voltages at these points should be 20 V, 10 V, 12 V, 6.8 V, 1.8 V and 6 V respectively.

The headphone amplifier delivers 2 V R.M.S. with the maximum input signal of 850 mV. Headphones with an impedance of 400 ohms or higher can be

2



**Parts list for figure 2**

**Resistors:**

- R1, R14 = 100 k
- R2, R13 = 1 M
- R3, R11 = 10  $\Omega$
- R4, R12 = 1k2
- R5, R10 = 270 k
- R6, R9 = 150 k
- R7 = 56 k
- R8 = 470 k

**Capacitors:**

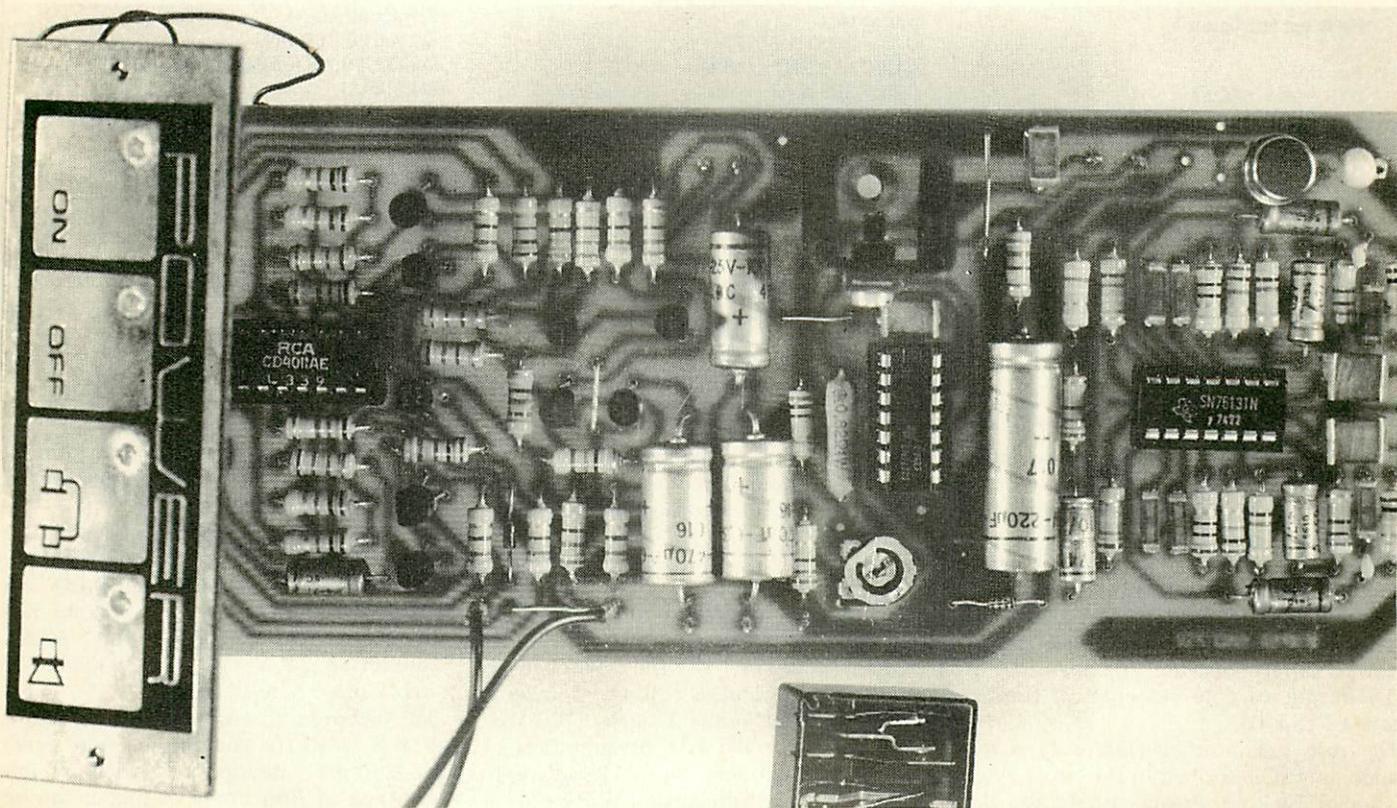
- C1, C15 = 680 p
- C2, C6, C10, C14 = 4 $\mu$ 7/25 V
- C3, C13 = 2n7
- C4, C5, C11, C12 = 4n7
- C7, C9 = 470 n
- C8 = 10  $\mu$ /16 V
- C16 = 100 n
- C17 = 10 ... 22  $\mu$ /25 V

**Semiconductors:**

- IC1 = SN 76131,  $\mu$ A 739, TBA 231
- IC2 = TBA 625 C

**Figure 2. Circuit of the disc preamplifiers, and external connections to the TBA 625C stabiliser IC from which they are supplied.**

**Figure 3. Printed circuit board and component layout.**



connected to the output D. The value of capacitor C23 is calculated for headphones with an impedance of 2 k. Transistor T1 must be adequately cooled; the power dissipation - and hence the dimensions of the heatsink needed - depends on the transformer secondary voltage:

Transformer secondary voltage (V RMS)	Heatsink area (cm <sup>2</sup> )
16	50
18	80

It is often a good solution to use the case as a heat sink, with the transistor mounted on the outside. The pull-in voltage for relay Re is about 10 V. The contacts must be rated to make and break at least 250 V, and a current depending on the maximum drawn by the power amplifiers. For two 100 W amplifiers driving 4-ohm loads a relay with 8 A contacts is suitable.

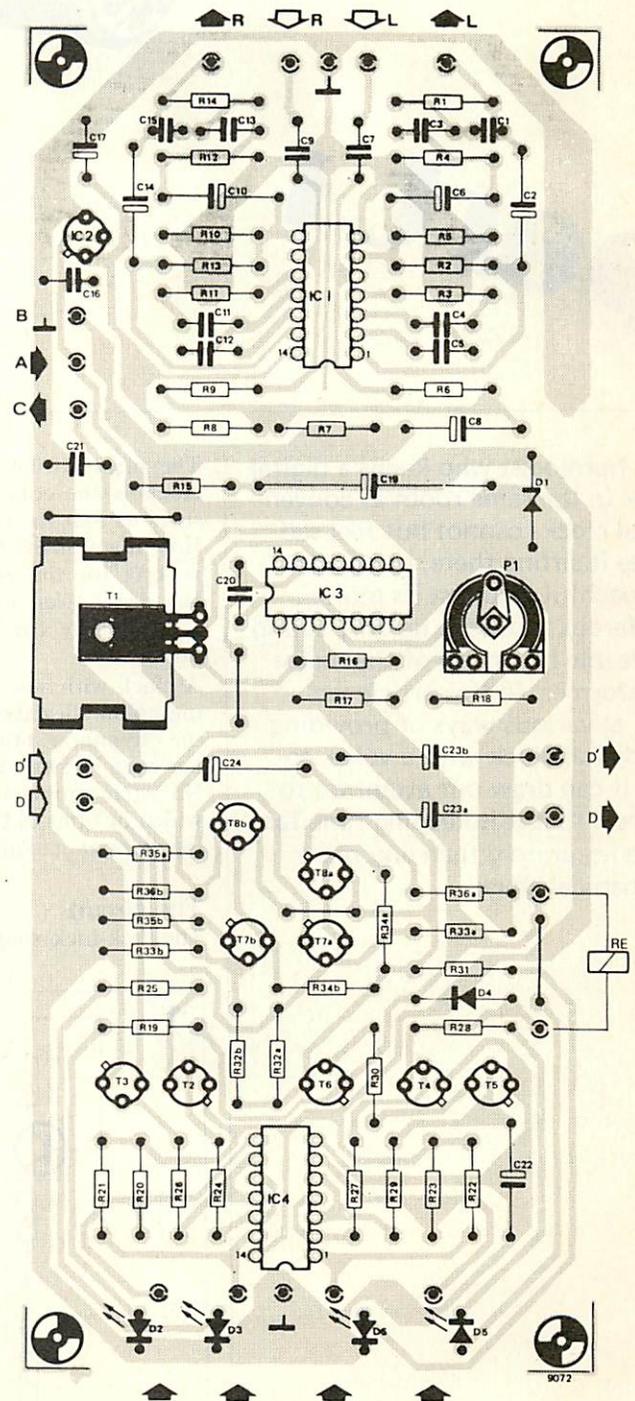
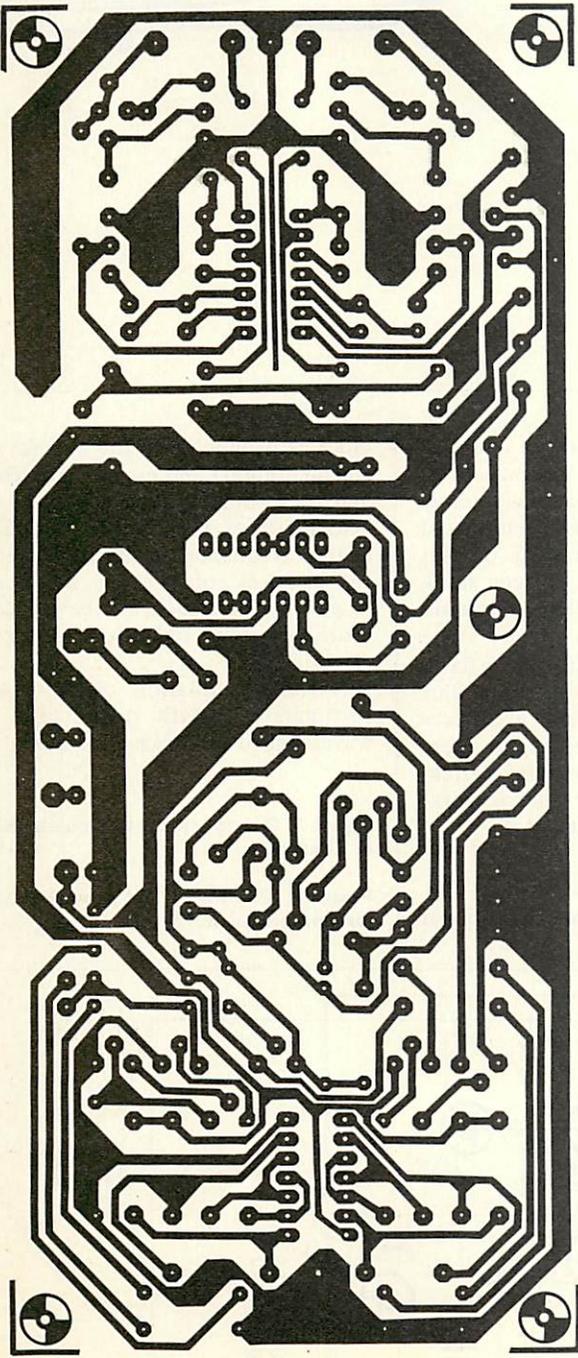
To avoid relay chatter when a number of touch panels are operated at the same time, it is advisable to connect 1 n capacitors C<sub>a</sub> to C<sub>d</sub> across each pair of touch contacts. A 100 n/400 V capacitor can be con-

nected across the relay to prevent contact burning.

The TBA 625C stabiliser IC delivers an output of 15 V. As this is the minimum acceptable voltage for the disc preamplifier, it is essential that a Type C stabiliser be used. A heat sink is not absolutely necessary. A tantalum electrolytic capacitor should be used for C17 to forestall any possible tendency to oscillation.

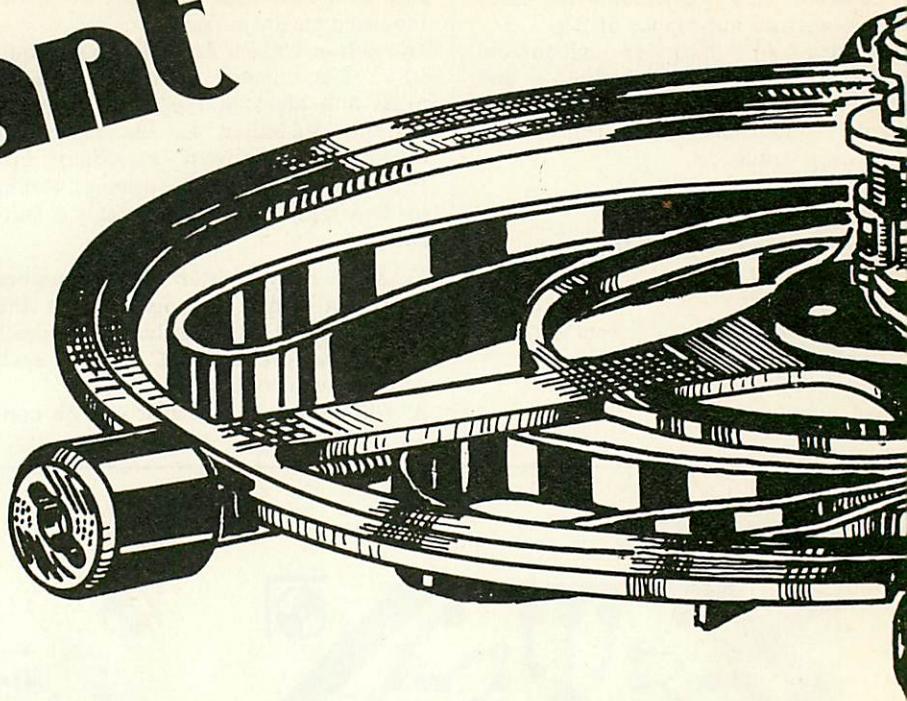
Figure 3 shows the printed circuit board and the component layout for the TAP-power circuit. Except for the mains transformer, bridge rectifier, smoothing capacitor C18 and relay, all the components are accommodated on one board.

3



# clamant clock

## part 1



Any horologist who keeps a digital clock in the same room as conventional clocks cannot but feel sad to see it sitting there, mute and reproachful amongst its more vociferous brothers, its only sound the feeble humming of the mains transformer. In this article we look at various ways of providing the digital clock with a voice, so that it can draw our attention to the fact that it is keeping time far more accurately than any mere mechanical clock.

The main attribute lacking in a digital clock is the comforting tick which assures us that the thing is actually going. How many man-hours have been wasted waiting for the elusive change of that last digit? 'Well I'm sure its been stuck at that time for more than a minute now.'

A clock with a seconds display or flashing colon alleviates these problems, but the hypnotic effect of such devices has been known to send people to sleep. No such problem exists with a tick, which informs us that the clock is working without actually looking at it.

clock is produced by the balance wheel (or pendulum) and escapement, the tick and tock sounds having different pitch. The pitch of the sounds and the repetition frequency obviously depend on the physical construction of the clock. A grandfather clock will have a deeper, more leisurely tick than a travelling alarm.

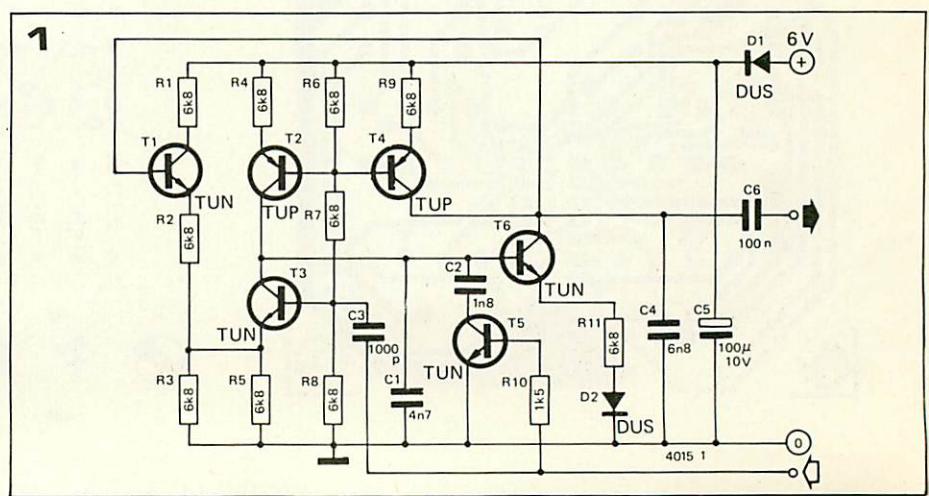
Electronic simulation of the sound is fortunately relatively simple. The waveform of the ticking is a damped res-

### The circuit

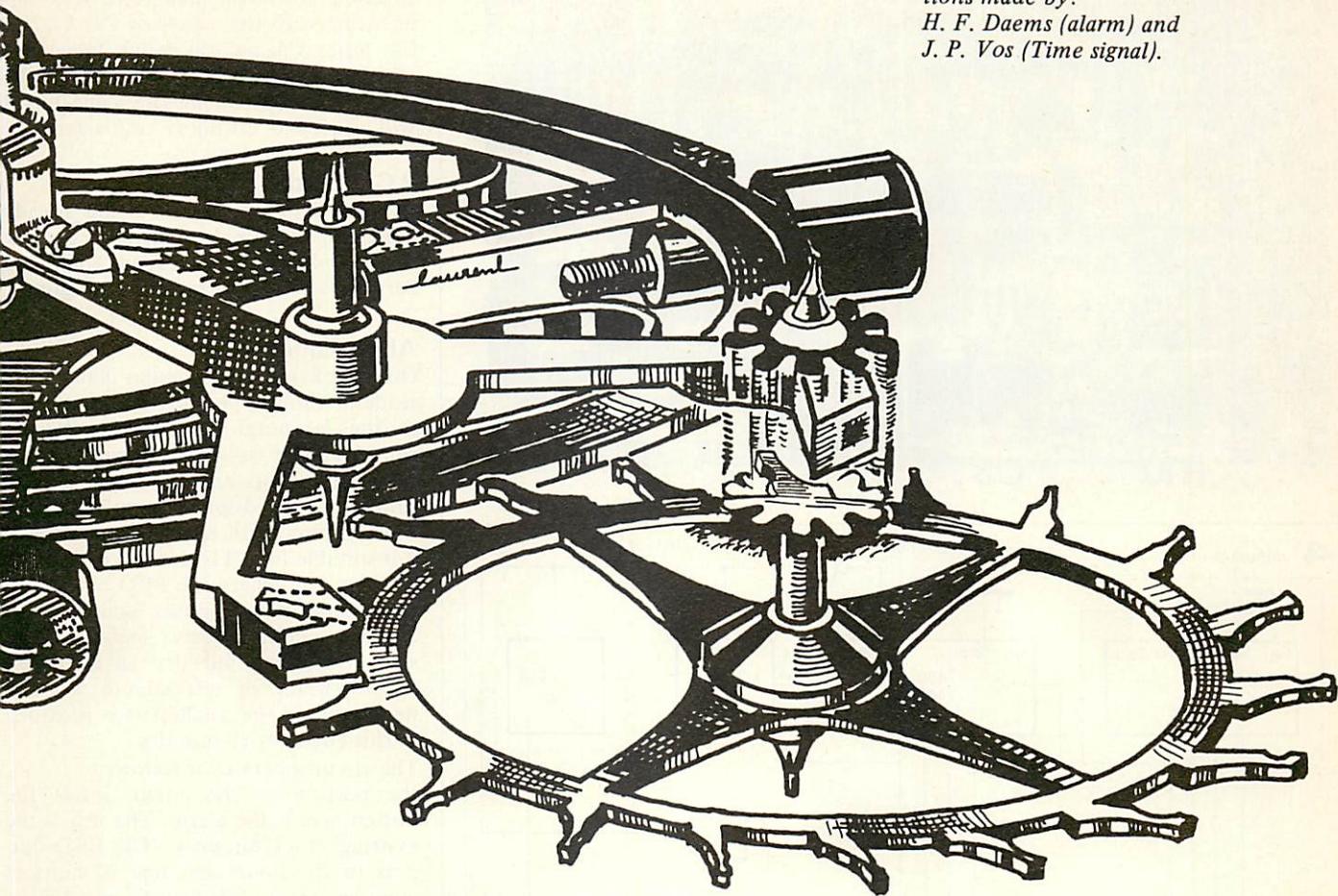
The tick-tock sound of a conventional

Figure 1. Gyator circuit to simulate tick-tock of a clock.

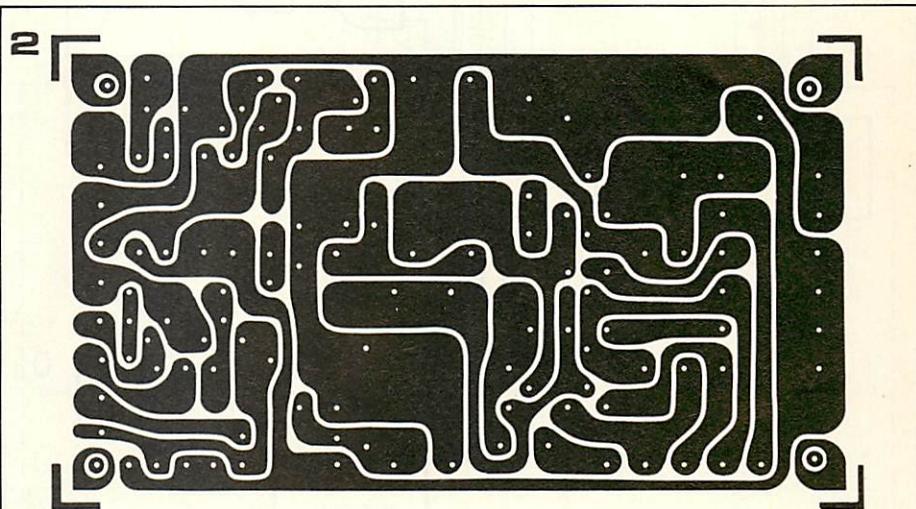
Figure 2. P.C. board and component layout for gyator circuit.



This article is based in part on suggestions made by:  
 H. F. Daems (alarm) and  
 J. P. Vos (Time signal).



onance similar to a percussion instrument. A suitable circuit is therefore the gyrator used in the Elektor Minidrum (february 1975). This circuit (with the component values modified for this application) is given in figure 1. Suitable 1 Hz trigger pulses may be obtained from the clock circuit by taking an output from the counter preceding the seconds counter. The pulses must be TTL compatible (5 V amplitude) and have a 1 : 1 mark-space ratio, otherwise the ticking will sound unbalanced. The pulses are fed into the base of T3 through C3 to trigger the gyrator, whilst T5 switches C2 in and out of circuit to alter the relative frequency of the tick and tock.

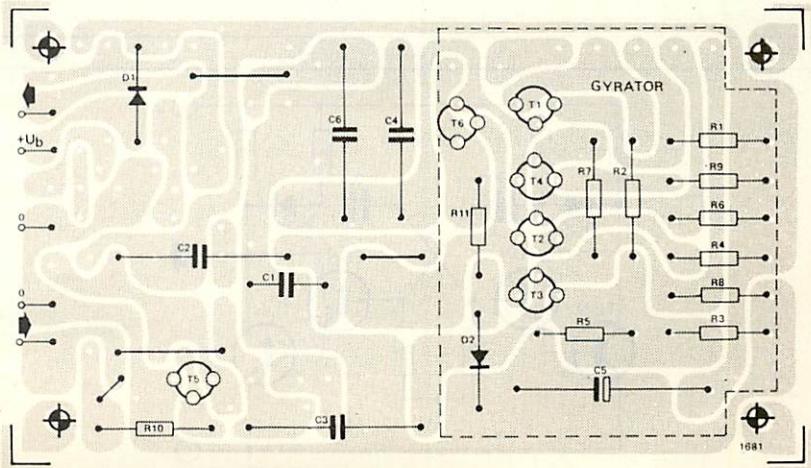


**Components list for figure 1**

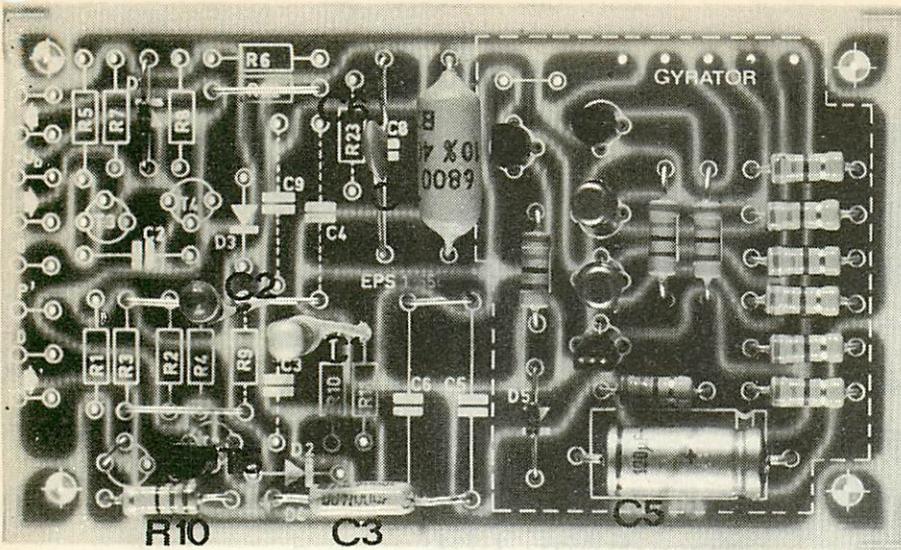
**Resistors:**  
 R1 ... R9, R11 = 6k8  
 R10 = 1k5

**Capacitors:**  
 C1 = 4n7  
 C2 = 1n8  
 C3 = 1 n  
 C4 = 6n8  
 C5 = 100 μ/10 V  
 C6 = 100 n

**Semiconductors:**  
 T1, T3, T5, T6 = TUN  
 T2, T4 = TUP  
 D1, D2 = DUS



3



The frequency of the sounds may be adjusted to suit personal taste by experimenting with the values of C1, C2 and C4. Since C3 and the input impedance of the trigger input differentiate the trigger pulse, changing the value of C3 will affect the 'crispness' of the sound.

**P.C. Board**

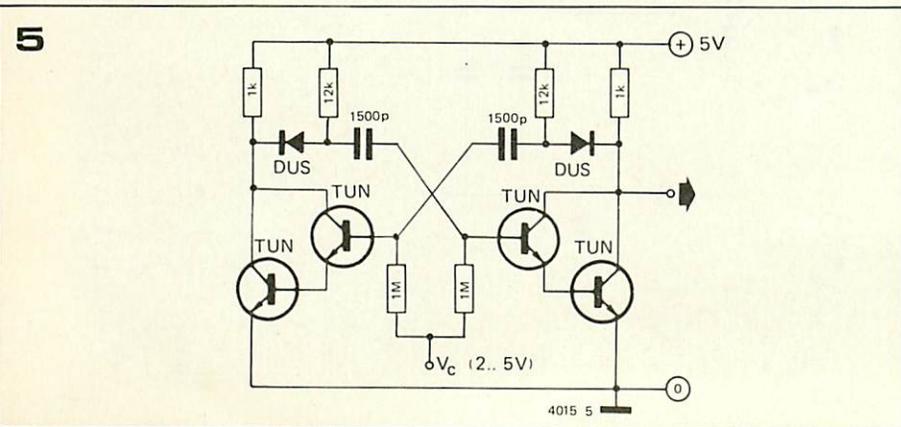
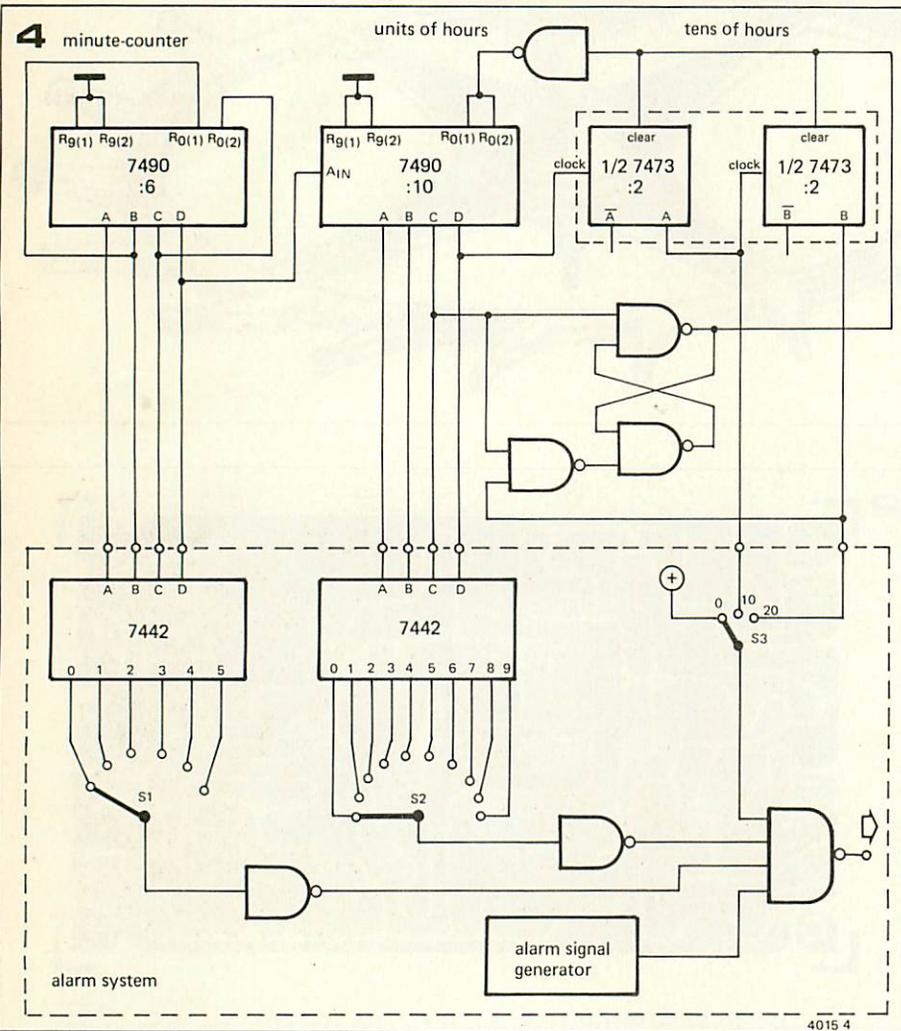
A suitable printed circuit board already exists for the Minidrum gyrator, and the board and component layout (modified for use with clock) are given in figure 2

**Alarm Clock**

One clock noise in popular demand by readers (though perhaps not first thing in the morning) is an alarm. It is a simple matter to add an alarm to a digital clock (but unfortunately not so simple if the display is multiplexed). The alarm control circuit given in figure 4 is suitable for TTL clocks with parallel outputs (i.e. where the BCD outputs of the hours and minutes counters are available continuously and are not strobed). It was felt that an alarm setting accuracy of one minute was not necessary, so the smallest step provided in this circuit is 10 minutes.

The circuit operates as follows: the portion of the circuit inside the dotted box is the alarm. The rest is the existing clock circuitry. The BCD outputs of the hours and tens of minutes counters are decoded to decimal by the 7442's. No decoding of the tens of hours is required as the truth table for this counter (table 1) shows. Outputs A and B are never both '1' at the same time. The desired alarm time is selected by single-pole switches S1 - S3. When the required time is reached three of the inputs of the four-input NAND gate go high. This allows the alarm signal connected to the fourth input to pass through the gate.

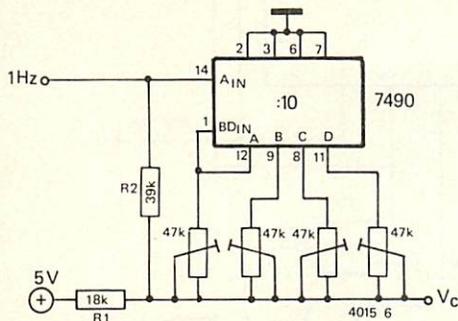
The possibilities for the actual alarm signal generator are endless. The simplest solution would be a fixed frequency oscillator such as an astable multivibrator. There are however more interesting possibilities. The voltage-controlled multivibrator of figure 5 can be made to play a tune by connecting differing voltages sequentially to the control input. For a control voltage range of 2-5 V the frequency range covered is about 3 octaves. There are various methods of driving the oscillator. A simple circuit is shown in figure 6. This consists of a 7490 connected as a BCD decade counter, with its outputs connected to the VCO via presets. As the



**Table 1**

HOURS	A	$\bar{A}$	B	$\bar{B}$
0	0	1	0	1
10	1	0	0	1
20	0	1	1	0

6



7

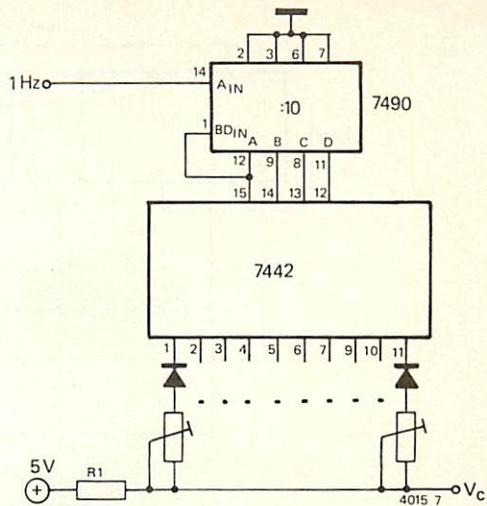


Figure 3. Photograph of the completed board.

Figure 4. Circuit of an alarm control system.

Figure 5. A voltage-controlled oscillator VCO that may be used to generate a tuneful alarm signal.

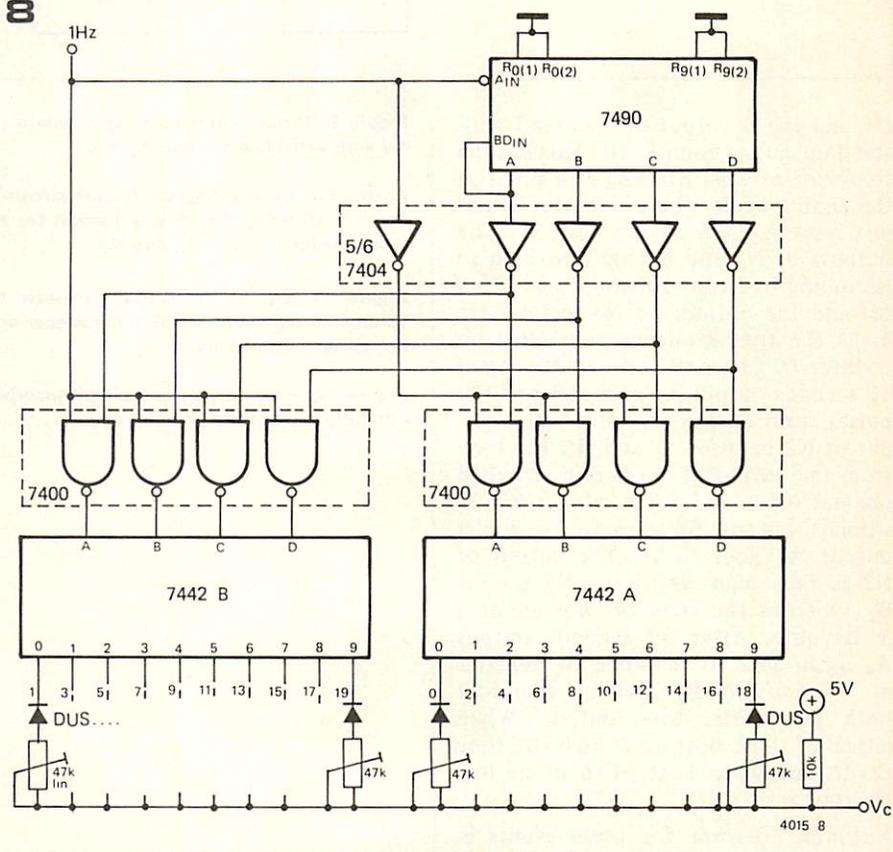
Figure 6. Using the existing seconds counter in the clock to produce a varying voltage for the VCO. Since the outputs interact it is difficult to tune this circuit to play a particular melody.

Figure 7. This circuit may be used to make the VCO play a tune. Ten independent sequential outputs are produced, so each preset can be used to tune one note in the sequence.

Figure 8. Extension of the circuit of figure 7 to a 20-note sequence.

Table 1. Output of an arbitrary tens of hours counter as in figure 4.

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output states of the counter change so will the output voltage to the VCO. Of course the outputs change in a binary sequence so more than one output can be high at one time.

Since the outputs interact it is difficult to set this circuit to play a particular tune. In addition the 1 Hz clock pulses are also fed in via R2 increasing the permutations still further.

If one requires a circuit which can be set to play a particular tune then figure 7 is more suitable. Here the outputs of the 7490 are decoded with a 7442 to give ten independent outputs. These outputs go low in sequence as the counter goes through its cycle. All other outputs are high, reverse-biasing their respective diodes, so no current flows through their respective presets. Only the preset connected to the output which is low forms a potential divider with R1. This

means that each note in the sequence can be tuned independently.

This ten-note sequence can easily be extended to twenty notes by the circuit of figure 8. In this circuit two decoders are driven by the 7490 and are switched in and out by the 1 Hz clock pulses to the counter. Thus, during the half-period when the clock pulse is '0' the outputs of the 7490 are switched through the transfer gates (7400) to decoder A. The other transfer gates are disabled by the '0' on their commoned inputs, so their outputs are all '1'. This is an invalid input code for the 7442 so all its outputs are high. During the '1' half period of the clock pulse the reverse situation occurs. Decoder B is enabled, whilst A is disabled. Decoder A thus controls the even notes 0, 2, 4, . . . in the sequence, whilst decoder B controls the odd notes 1, 3, 5, . . . . Of course in this case, if an

equal time span is required for each note then the clock pulse waveform must have a 1 : 1 mark-space ratio. The 7490 in all these cases can be the existing seconds counter in the clock.

Another variation on the alarm theme can be obtained by a circuit which changes the rhythm of the tone sequence, making it less monotonous. Such a circuit is given in figure 9. The dividers I to III are again part of the existing clock circuit. The operation of the circuit is as follows:

counter II controls the pitch of the voltage controlled multivibrator as in the circuit of figure 6, except that no adjustment is provided for. The time at which the alarm sounds is again determined by the alarm control circuit, as in figure 4. The rhythm variation is provided by gating the C output of counter I with the A output of counter

9

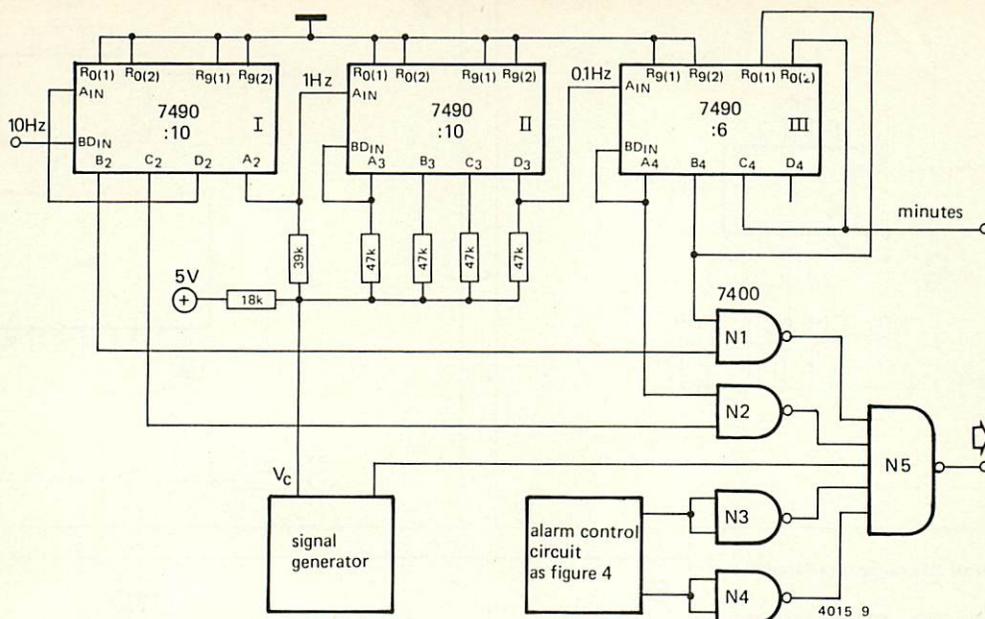


Figure 9. Circuit for generating an alarm signal with variable pitch and rhythm.

Figure 10. Timing diagram for the circuit of figure 9, showing the tone sequences for the four possible states of  $A_4$  and  $B_4$ .

Figure 11. Circuit to gradually increase the volume of the alarm signal if the sleeper does not awaken immediately.

Figure 12. A complete alarm circuit incorporating the ideas of the previous circuits.

III, and the B output of counter I with the B output of counter III. This has the following effects. Starting at a point in the timing cycle where counter III has just reset  $A_4$  and  $B_4$  are both '0'. The outputs of N1 and N2 are thus high so (assuming it is time for the alarm to go off and the outputs of N3 and N4 are high) the tone sequence controlled by counter III can pass through N5. After 10 seconds output  $A_4$  goes high and the pulses from output  $C_2$  switch the output of N2 between '0' and '1'. The tone from the output of N5 is thus switched on and off at a 2.5 Hz rate. After 20 seconds output  $B_4$  goes to '1' whilst output  $A_4$  goes to '0'. The output of N2 is thus high whilst via N1 output  $B_2$  switches the tone on and off at a 5 Hz rate. After 30 seconds output  $A_4$  again goes to '1' while  $B_4$  remains at '1'. Outputs  $B_2$  and  $C_2$  therefore both affect the tone output. When either of these outputs is high the tone is off, and when both of them are low the tone is on.

A timing diagram for these events is shown in figure 10. The top two waveforms are the outputs  $B_2$  and  $C_2$  during a 1 second interval of the sequence (this repeats every second). The other 4 waveforms are the tone outputs that occur for the four possible states of  $A_4$  and  $B_4$ .

The audible effect is thus as follows: an uninterrupted tone sequence for 10 seconds, then a further 10 second interval of tone bursts and silence as in figure 10d, then 10 seconds as in figure 10e and finally 10 seconds as in figure 10f, after which the sequence repeats. Of course, during each ten second period the frequency of the tone is being varied by the outputs of counter II.

It should be noted that for all these alarm circuits a symmetrical 1 Hz squarewave is required from the output of counter II. This means that the 7490 (which consists of a divide-by-2 and a

divide-by-five counter in the same package) must be connected with the divide-by-2 after the divide-by-5, as shown in figure 9. If an existing clock circuit is used this counter may be connected as a BCD decade counter (i.e. with the divide-by-5 after the divide-by-2). Some slight modification may therefore be necessary.

### Volume Control

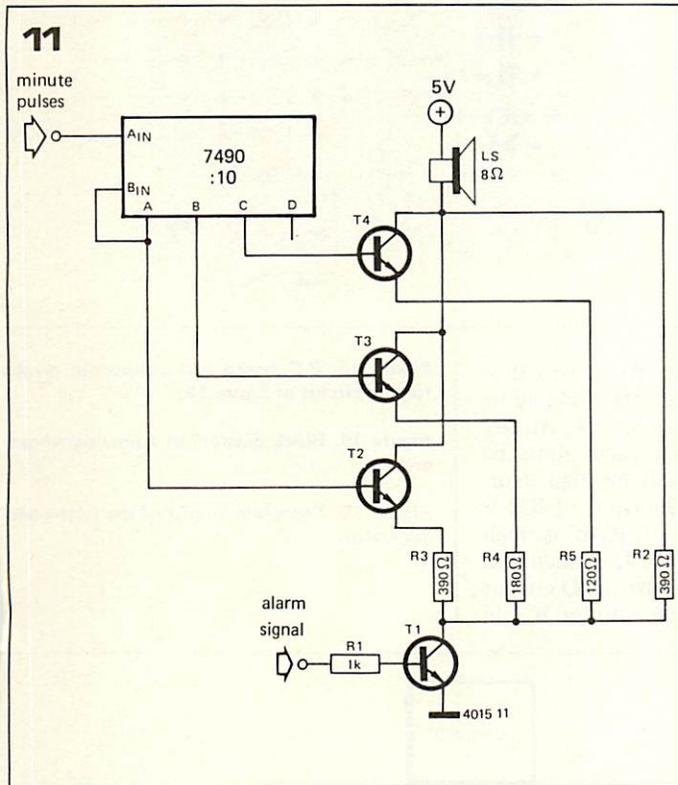
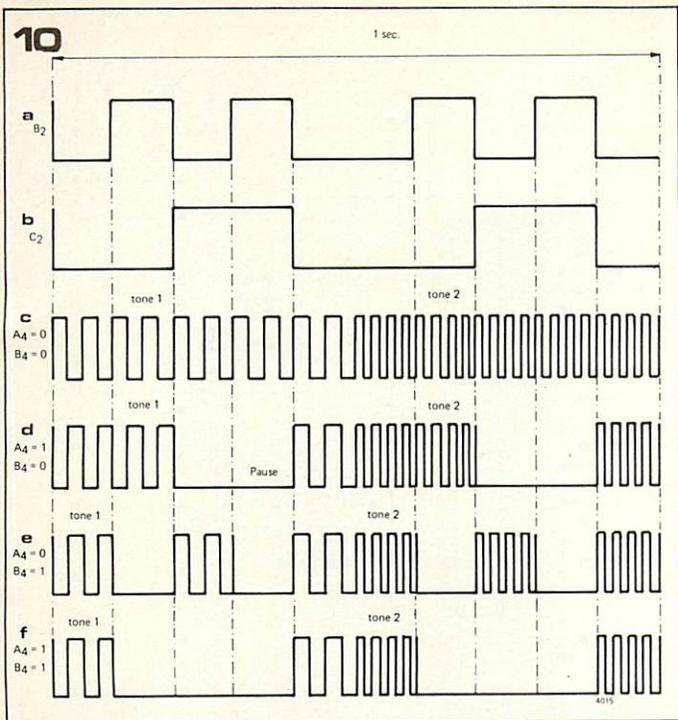
In order not to awaken the sleeper too harshly it is a simple matter to arrange a volume control so that the alarm tone starts at a low level and gradually becomes louder and louder until it is switched off. This is achieved by the circuit of figure 11. The counter shown is the minutes counter (i.e. the one that drives the minutes display). Since the alarm can only be set in units of ten minutes, the alarm will sound when the

tens of minutes have just changed to the required number and the minutes counter is reset. Outputs A to C of the minutes counter are thus at '0', so T2 to T4 are turned off. The alarm tone is applied to the base of T1 via R1 and switches this transistor on and off causing a signal from the loudspeaker. Since there is a 390  $\Omega$  resistor (R2) in series with it the tone is not very loud. After 1 minute the A output of the counter goes to '1', switching on T2 and thus connecting R3 in parallel with R2. The tone thus becomes louder. After 2 minutes output B becomes '1' while A becomes '0'. R4, which is smaller than R3, is paralleled with R2, so the tone becomes louder still. After 3 minutes outputs A and B are '1', and after 4 minutes output C becomes '1', by which time the tone is quite loud. Output D is not connected to this system. If the sleeper has not awoken after 8 minutes output D will become '1' and can be connected to set off a small explosive charge underneath the bed. A less drastic cure for the deep sleeper is to connect an additional transistor to output D with a 56  $\Omega$  resistor in series with its emitter.

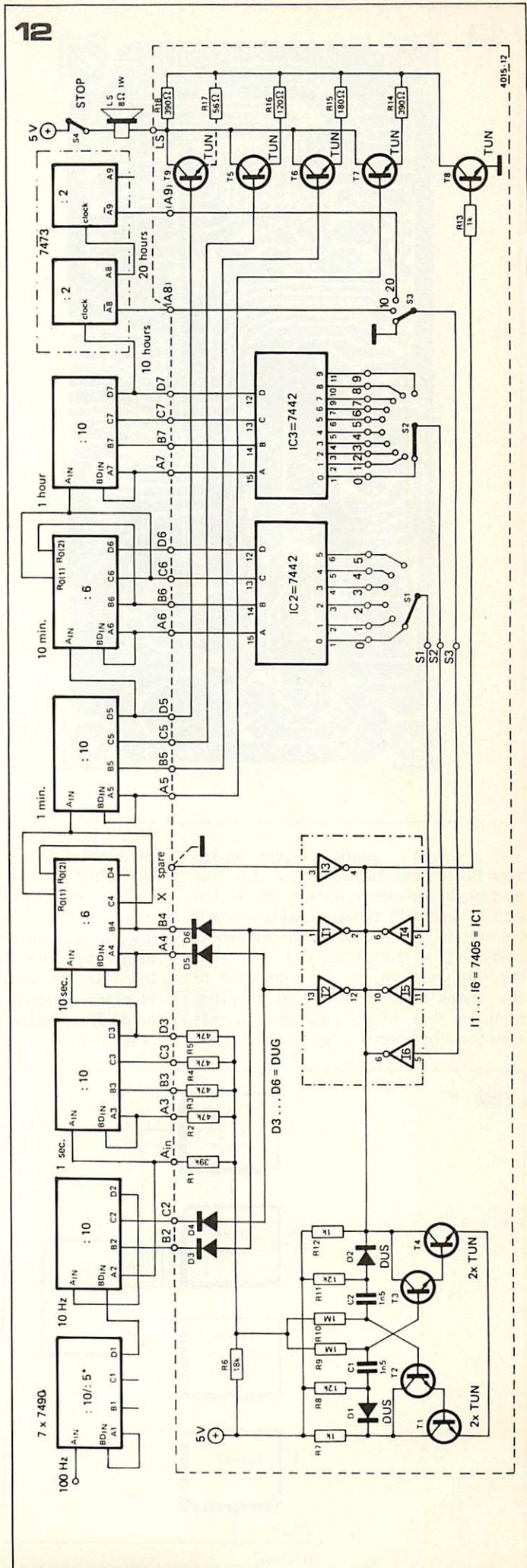
The complete circuit of an alarm system is given in figure 12. Everything within the dotted box is the alarm circuit, whilst everything outside is the existing clock circuitry. This differs slightly from the circuits discussed in that a HEX-inverter replaces the five-input NAND-gate in the alarm control circuit. This has open-collector outputs, so the outputs may be joined to perform a wired-OR function. In this circuit the additional transistor T9 is shown connected to output D5 for the extra loud alarm signal. A suitable printed circuit board and component layout for this alarm are given in figure 13.

### Time Signal Generator

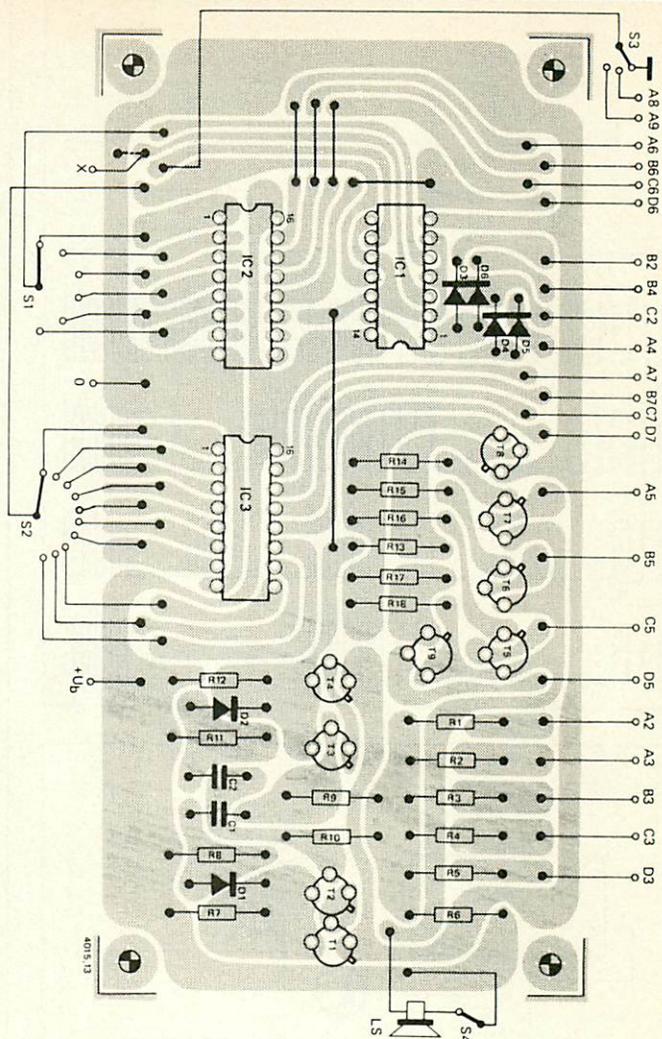
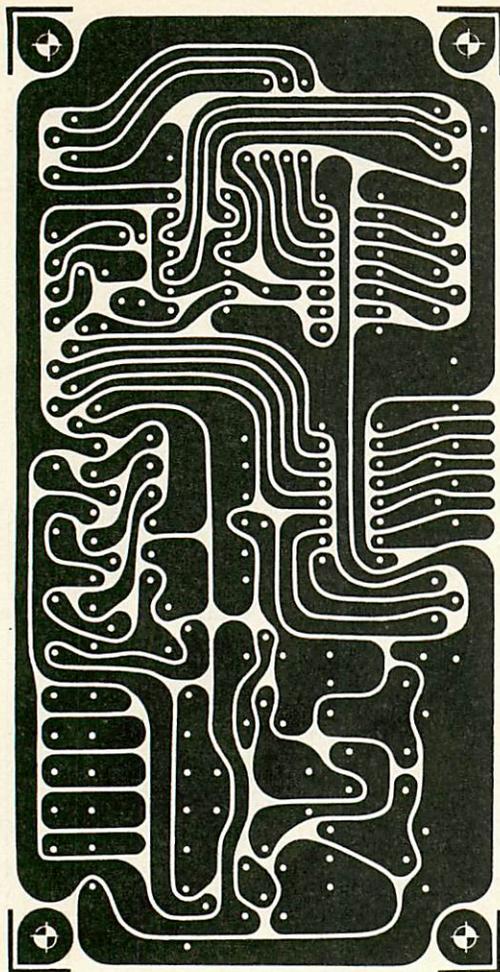
Provision of a 'six pips' time signal every hour is a relatively simple matter



- Components list for figure 12**
- Resistors:**  
 R1 = 39 k  
 R2 ... R5 = 47 k  
 R6 = 18 k  
 R7, R12, R13 = 1 k  
 R8, R11 = 12 k  
 R9, R10 = 1 M  
 R14, R18 = 390 Ω  
 R15 = 180 Ω  
 R16 = 120 Ω  
 R17 = 56 Ω
- Capacitors:**  
 C1, C2 = 1n5
- Semiconductors:**  
 T1 ... T9 = TUN  
 D1, D2 = DUS
- IC's:**  
 IC1 = 7401  
 IC2, IC3 = 7442
- Switches:**  
 S1 = single pole 6-way  
 S2 = single pole 10-way  
 S3 = single pole 3-way (decimal coded thumbwheel switches suggested)



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and a suitable circuit is given in figures 14 (block diagram) and 15. The portion of the circuit outside the dotted box in figure 15 is the existing seconds counter in the clock. The circuit works in the following manner: the inputs of gate 1 are connected to the outputs of the tens of minutes, minutes, tens of seconds and seconds counters corresponding to the time

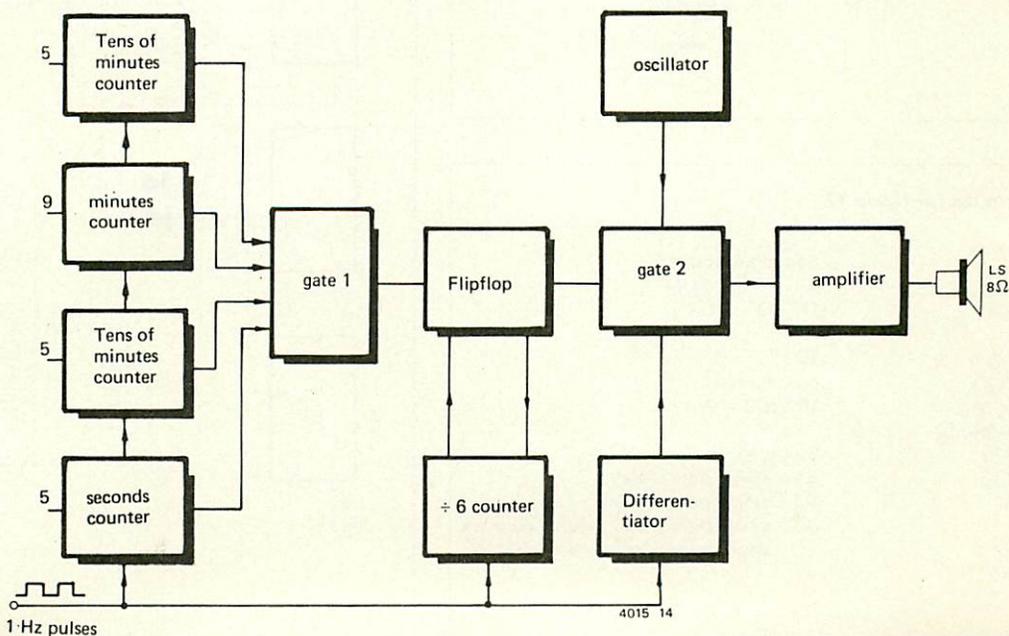
59 minutes 55 seconds. When this time is reached the inputs of gate 1 will all be high, so the output will be low. At any other time at least one input must be low, so the output will be high. Normally therefore, the  $\bar{Q}$  output of IC2 is low, so the output of IC4a (which will be dealt with later), whilst the Q output of IC3 is high, holding the  $\div 6$  counter in

Figure 13. P.C. board and component layout for the circuit of figure 12.

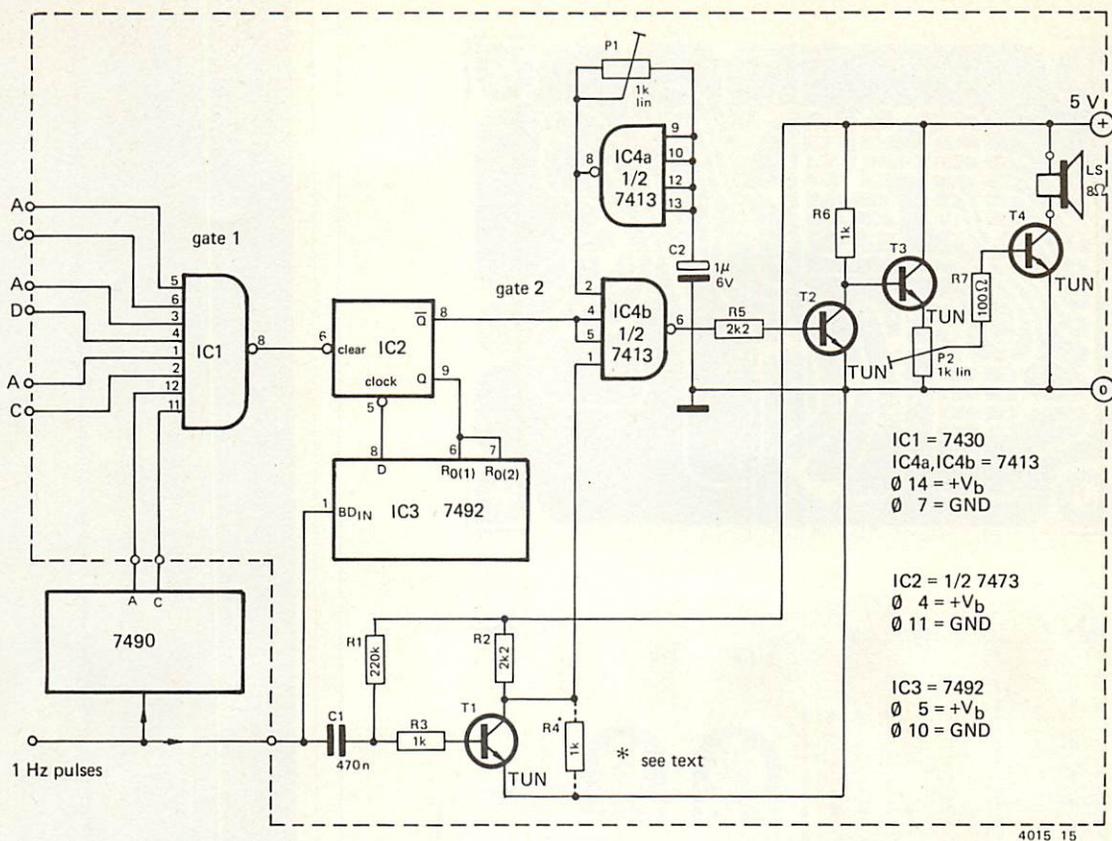
Figure 14. Block diagram of a time-signal generator.

Figure 15. Complete circuit of the time-signal generator.

14



15



- IC1 = 7430
- IC4a, IC4b = 7413
- Ø 14 = +V<sub>b</sub>
- Ø 7 = GND
  
- IC2 = 1/2 7413
- Ø 4 = +V<sub>b</sub>
- Ø 11 = GND
  
- IC3 = 7492
- Ø 5 = +V<sub>b</sub>
- Ø 10 = GND

Components list for figure 15

- Resistors:
- R1 = 220 k
- R2, R5 = 2k2
- R3, R4, R6 = 1 k
- R7 = 100 Ω
- P1, P2 = 1 k
  
- Capacitors:
- C1 = 470 n
- C2 = 1 μ, 6 V
  
- Transistors:
- T1 ... T4 = TUN
  
- IC's:
- IC1 = 7430
- IC2 = 7413
- IC3 = 7492
- IC4 = 7413

the reset condition. On the negative-going edge of the incoming seconds pulse at 59 minutes 55 seconds the output of the seconds counter will assume the condition '5', i.e. outputs A and C high. The output of gate 1 will go low, clearing IC2 so that the Q output goes low and the  $\bar{Q}$  output goes high.

IC3 may now count the incoming seconds pulses. However, due to the propagation delays through the seconds counter, IC1 and IC2, it will not count on the above-mentioned negative-going edge, as this has already disappeared before the counter is enabled. However, the negative-going pulse is differentiated by C1 and R3 (neglecting R1 and the base resistance of T1), and turns off T1 for about 100 ms. This takes pin 1 of IC4 high, and since pins 4 and 5 are already held high by the  $\bar{Q}$  output of IC2 the oscillator will be gated through it providing a 1 kHz tone burst of 100 ms duration.

On each negative-going edge of the five subsequent second pulses IC3 will count and the oscillator will provide a 100 ms tone burst. On the fifth pulse the D output of IC3 will go high, and on the sixth pulse the D output goes low, clocking IC2, so that its Q output goes high and its  $\bar{Q}$  output goes low. This disables the oscillator and holds the counter (IC3) in a reset condition so that it can count no further seconds pulses. This condition obtains for a further 59 minutes 55 sec-

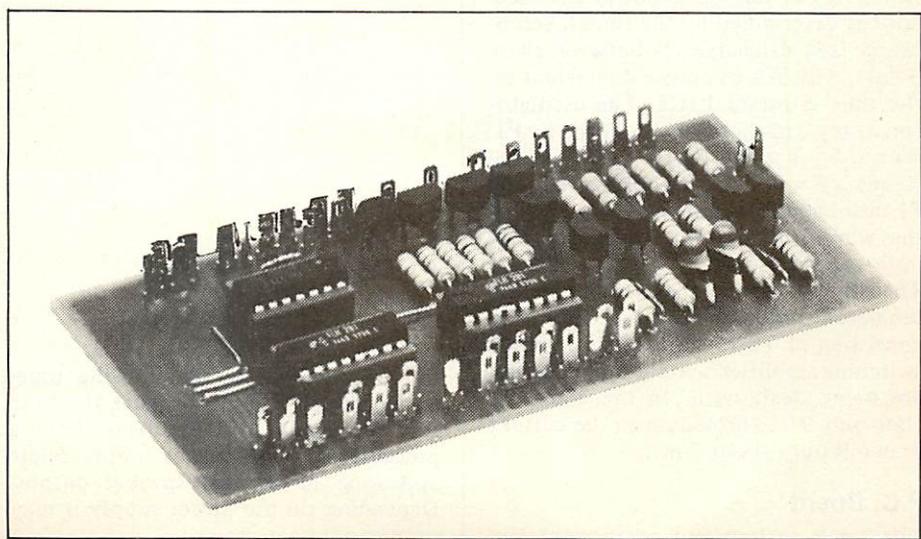
onds until it is time for the next signal. The circuit thus produces six pips every hour, starting with the first pip at 59 minutes 55 seconds and terminating with a pip exactly on the hour. Of course, this circuit produces pips of equal length, whereas the last pip of a radio time signal is longer than the preceding five. An alternative circuit, which produces this type of signal, was described in Elektor July/August 1975.

Oscillator and Amplifier

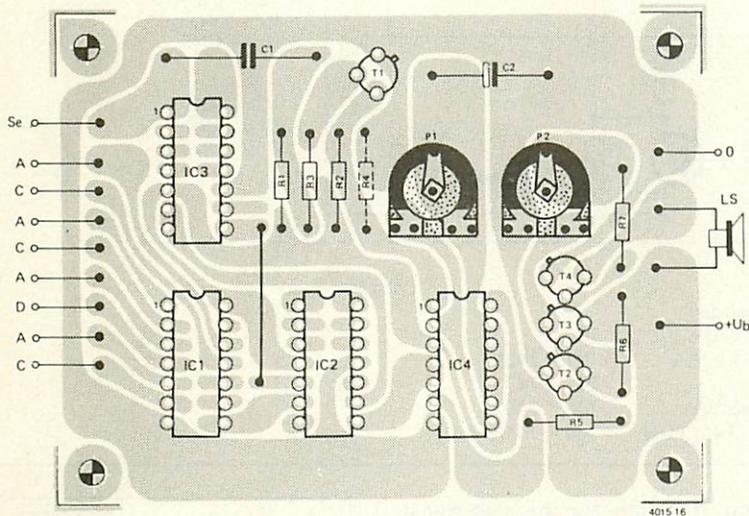
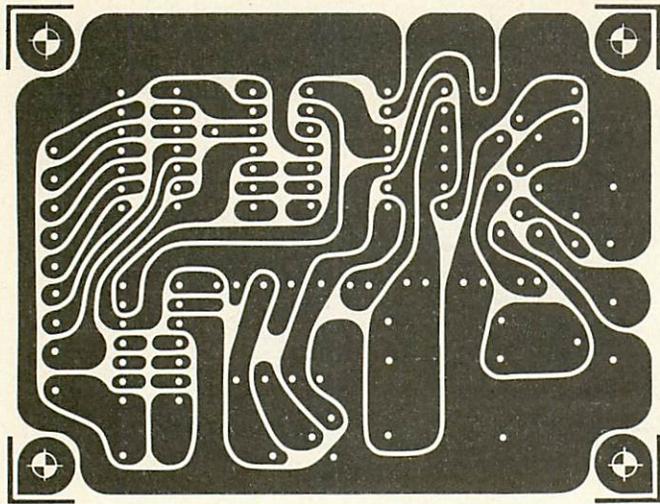
The oscillator is a simple single time

COUNT	OUTPUTS		
	D	C	B
0	0	0	0
1	0	0	1
2	0	1	0
3	1	0	0
4	1	0	1
5	1	1	0
0	0	0	0

Table II. Truth table for the 7492 connected as a divide-by-6 counter.



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constant multivibrator based on the 7413 which is a dual 4-input NAND Schmitt Trigger. Assuming the output of IC4a is initially high then C2 will charge through P1 until the voltage across it reaches the threshold of the Schmitt trigger. The output will then go low and C2 will discharge through P1 until it falls below the threshold, when the output will go high again. Because of hysteresis the negative-going threshold is below the positive-going threshold, so the frequency of the oscillator is determined by the time taken to charge and discharge C2 between these points, which is of course dependent on the time constant P1C2. The oscillator frequency can therefore be varied by P1. With  $C2 = 1 \mu$  and P1 set to  $330 \Omega$  the frequency will be about 1 kHz. Altering P1 also changes the mark-space ratio of the waveform, but this is unimportant in this application.

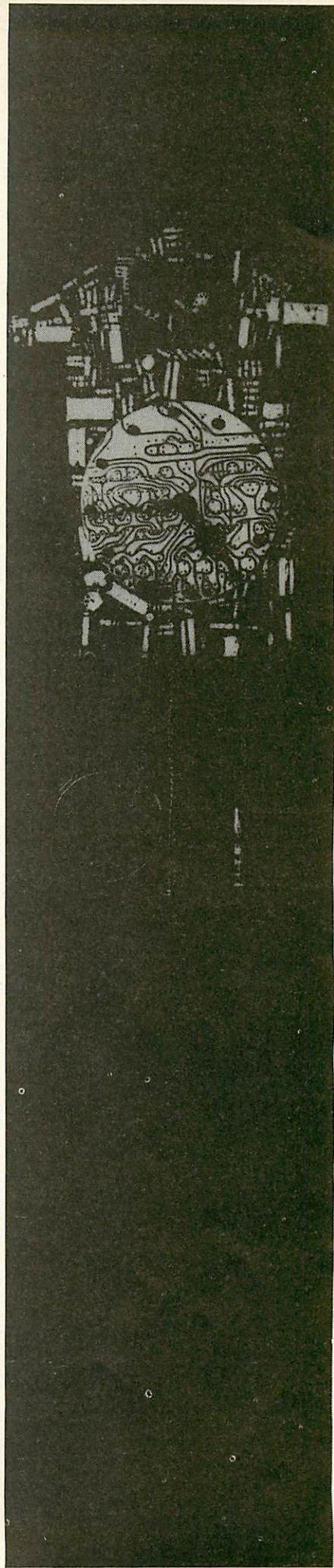
The other gate in IC4 is used to gate the oscillator output into the amplifier, consisting of T2 to T3. This is a simple switching amplifier, as only square waves are being dealt with. In the quiescent state only T2 is turned on so the current drawn is only about 7 mA.

### P.C. Board

The track pattern and component lay-

Figure 16. Board and component layout for the time-signal generator.

out of a board suitable for the time-signal circuit is given in figure 16. Note that R4 (shown dotted in figure 15) is a precaution against power supply ripple appearing at the loudspeaker output. Depending on the power supply it may or may not be necessary.



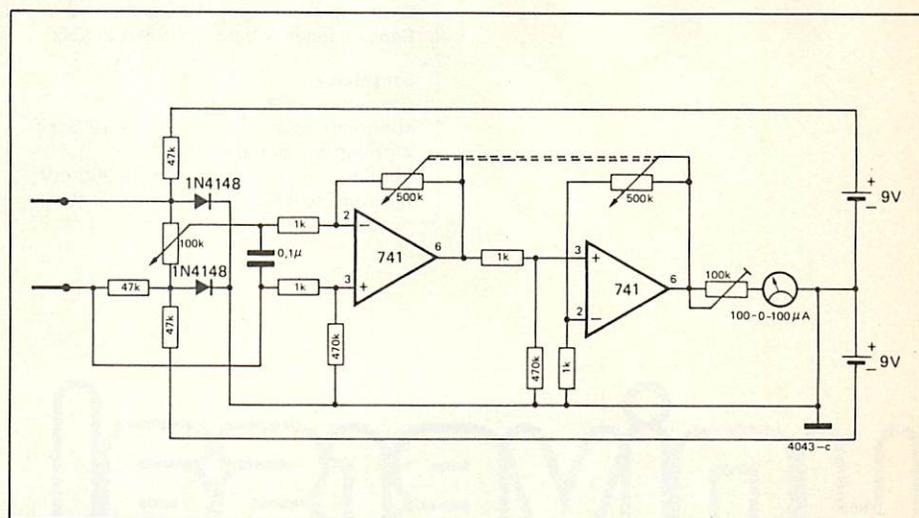
J. Jacobs

# lie detector

This lie detector works in the usual manner by measuring skin resistance and therefore is no innovation, but in comparison with the designs popular some years ago it offers a number of useful improvements. In the circuit the advantages of opamps have been turned to full use. The detector operates fully symmetrically, and therefore two batteries are required. The voltage across the electrodes according to local regulations in some countries, may not be higher than 2 V so a reference voltage of no more than 1.2 V is applied to the input of the measuring bridge. Since the resistance of the human skin is generally 50 k or less, the voltage across the electrodes will be at maximum 0.6 V. The set-up of the measuring bridge has the additional advantage that the reference voltage is independent of the battery voltage. To obtain a sufficiently high sensitivity the total amplification in the detector should preferably be greater than 100,000 times. Therefore a second opamp was added, which brings the overall amplification to about 250,000 times. With the double potentiometer of 500 k the amplification

can be adjusted from 0 to the above-mentioned maximum. The 100 k potentiometer serves to adjust the sensitivity of the moving coil meter; therefore the input bridge is first brought completely out of balance to the one side and then to the other by means of

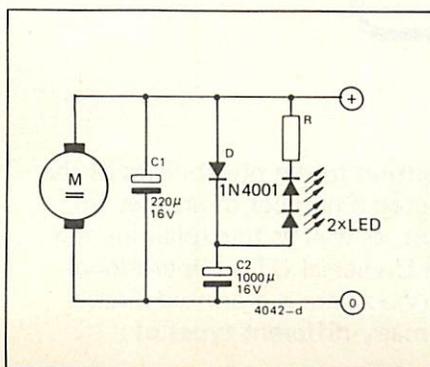
the 100 k potentiometer, whilst the positive and negative deflection of the meter is adjusted to maximum. Afterwards the adjustment potentiometer can, if required, be replaced by a fixed resistor.



R. Zimmer

# brake lights for model cars

This circuit performs two functions: when the supply voltage to the motor of the model car cuts out, the car will not stop abruptly but will continue over some distance and during that time two LED's will light up and function as brake lights. Thus a very realistic effect is obtained. The circuit is extremely simple. As long as the car is under power, there is a voltage across the motor (M), the polarity of which is indicated in the diagram. Capacitor C<sub>1</sub> and (via diode D) also C<sub>2</sub> are now charged. When the voltage cuts out, C<sub>1</sub> discharges



across M and C<sub>2</sub> discharges via the two LED's, resistor R, and motor M. If braking is the result of a short-circuit of the supply voltage, both capacitors discharge via the short-circuit connection; in that case the LED's burn somewhat brighter. The value of resistor R can be calculated with the following simple formula:

$$R = \frac{12 - 2 \cdot V_{LED}}{I_{LED}}$$

Usually a value of about 560 Ω will be suitable.

Performance Data		
<b>Narrow-band FM reception</b> (VCO free-running frequency approximately 10.7 MHz)		
<b>Capture and hold ranges</b>		
	<b>Capture</b>	<b>Hold</b>
Input 160 $\mu$ V	190 kHz	540 kHz
Input 1.6 mV	250 kHz	4 MHz
Input 10 mV	400 kHz	10 MHz
<b>AM Suppression</b>		
Input 160 $\mu$ V		$\geq 60$ dB
Input 100 $\mu$ V		$> 40$ dB
<b>Sensitivity</b>		
Deviation = $\pm 3$ kHz		
Minimum input		= 3.2 $\mu$ V
With input = 4 $\mu$ V:		
output		= 700 mV,
signal/noise ratio		= 40 dB
<b>Wide-band Stereo FM reception</b> (VCO free-running frequency approximately 455 kHz)		
<b>Capture and hold ranges</b>		
With minimum input (12.6 $\mu$ V):		
Capture range $\approx$ hold range $\approx$ 400 kHz		
<b>Sensitivity</b>		
(Deviation = $\pm 30$ kHz)		
Minimum input		= 12.6 $\mu$ V
With input = 500 $\mu$ V:		
output		= 360 mV,
signal/noise ratio		$\geq 40$ dB

Most of the integrated PLLs now available for FM receivers are expensive and require a 24-volt power supply, which makes them inconvenient for either portable or car-borne use. This universal PLL works quite happily on a 5-volt supply, but the working voltage may be determined in practice by the needs of a MOSFET RF amplifier, which can require 9 volts. This, however, is easy to provide in battery-powered portable equipment, and it also leaves a margin for stabilisation when running from a 12 V car supply.

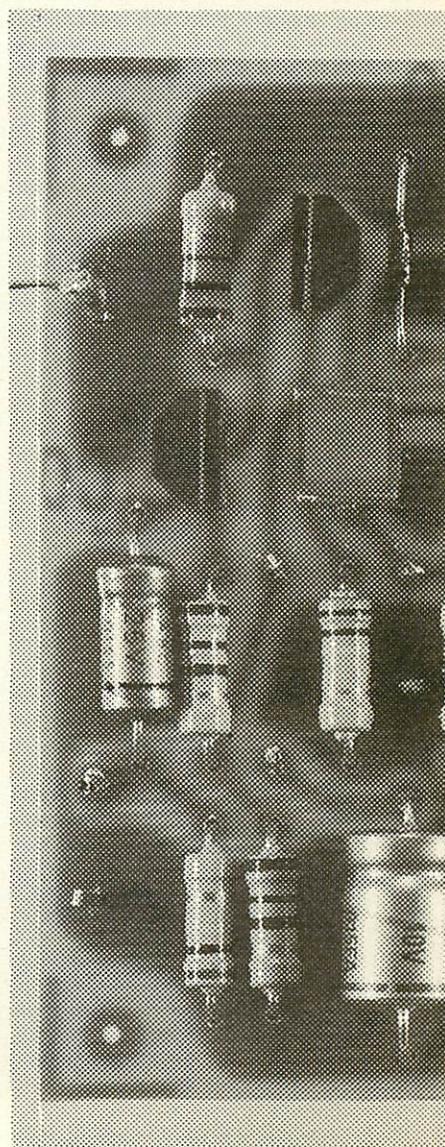
Sensitivity on a 10.7 MHz FM input with 3 kHz deviation is 3.2  $\mu$ V for a 700 mV audio output.

For a receiver for the 144 to 146 MHz band, the aerial signal is pre-amplified and converted to a band from 10 MHz to 12 MHz by a stable 134 MHz mixer-oscillator. Any signal in the 2 MHz-wide band can then be tuned in by adjusting (with a potmeter) the frequency of the voltage-controlled oscillator incorporated in the PLL.

Figure 1 shows a block diagram of the arrangement. The 134 MHz local oscillator will normally be a crystal oscillator of lower frequency in conjunction with a multiplier. Assuming the combined gain of the pre-amplifier and the mixing stage to have the easily-achievable value

# universal OTA PLL

Elektor has taken a lead in drawing attention to the possibilities of the PLL (Phase Locked Loop), and has devoted a number of articles to designs incorporating this versatile circuit, as well as to explaining the principles of different applications. The Universal OTA (Operational Transconductance Amplifier) PLL described here is a printed-circuit module which can form the nucleus of many different types of receiver.



of 20 dB, the overall receiver sensitivity for the quoted audio output of 700 mV will be some  $0.3 \mu\text{V}$ , which is better than that of most commercial receivers for this band.

For reception of wide-band broadcast FM signals, the unusual arrangement of a double superheterodyne, with a second IF as low as 455 kHz, is used (see figure 2). The low modulation index of a stereo FM signal makes demodulation with a good signal-to-noise ratio difficult to achieve, and even in the best (and most expensive) receivers this is seldom above 50 dB on strong signals. With this very low second IF, 60 dB is achieved.

### Yet again; what is a PLL?

For those who have not yet had an opportunity to familiarise themselves with the basic concept of the phase-locked loop, the essential features of this circuit can be repeated. The key element is a voltage-controlled oscillator. When the loop is used in a receiver, this oscillator is automatically synchronised with the carrier of the incoming signal. The other elements in the loop are subservient to the main purpose of keeping the oscillator synchronised. In practice, this is done by maintaining a constant phase difference between the incoming

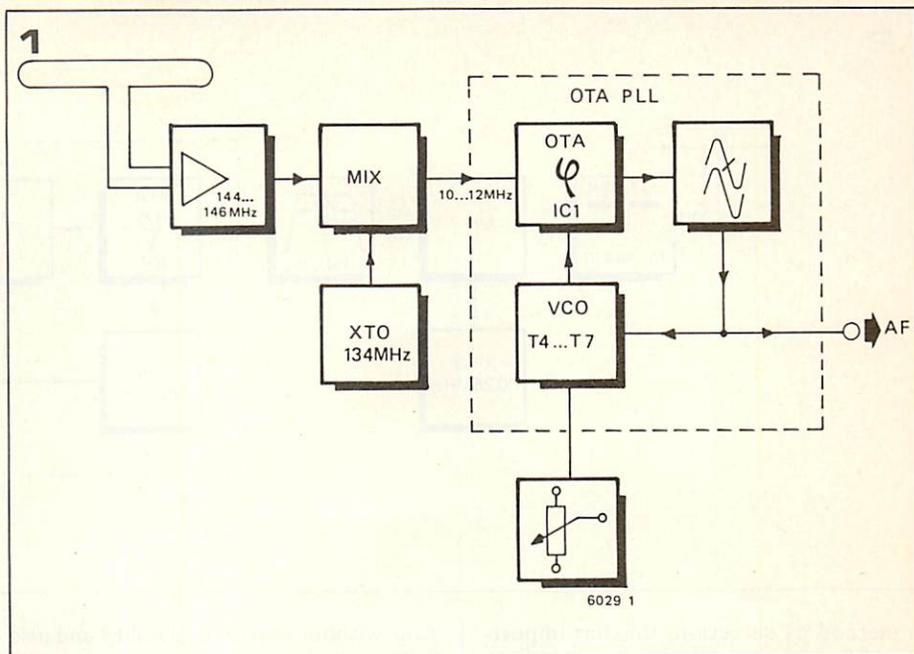
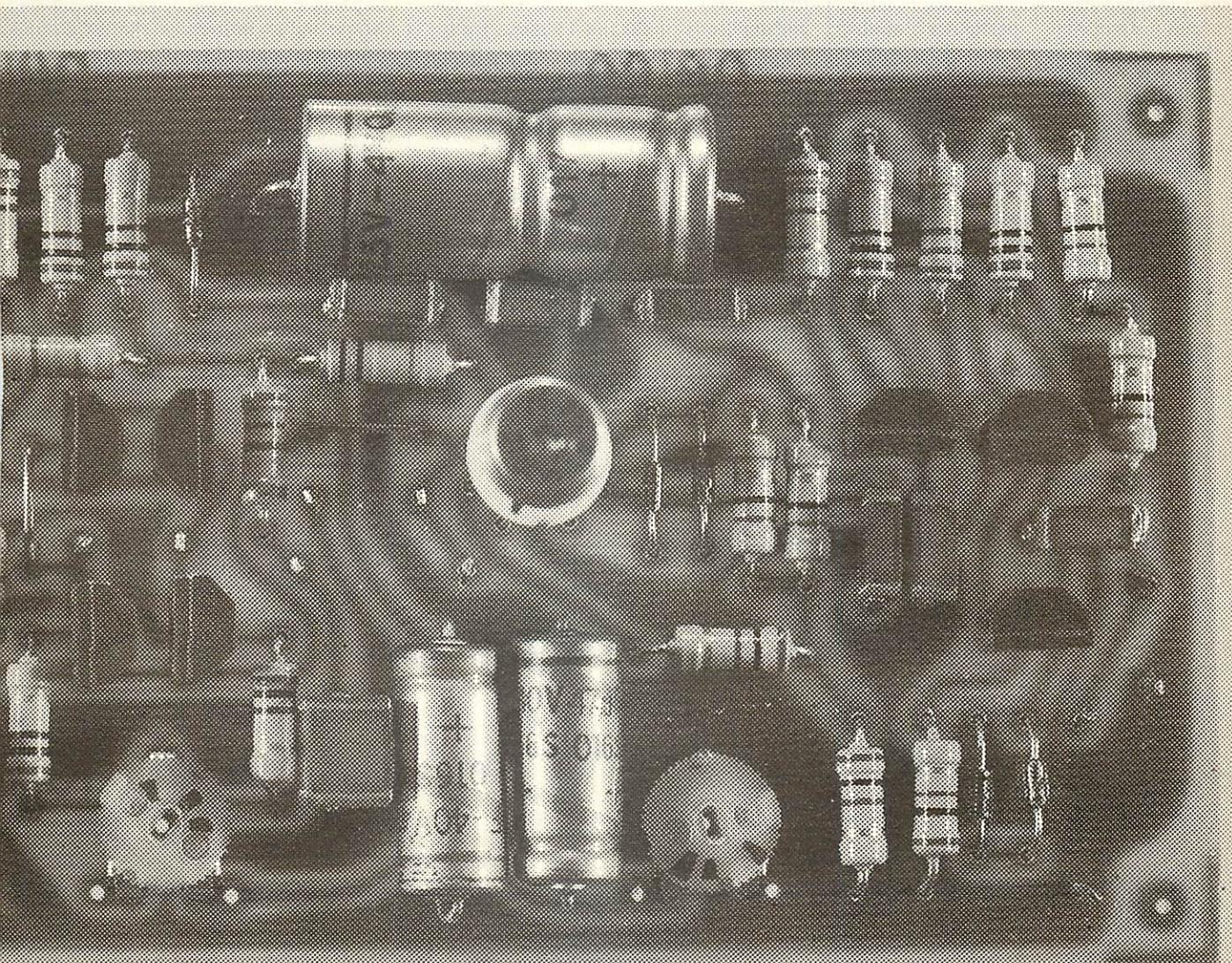


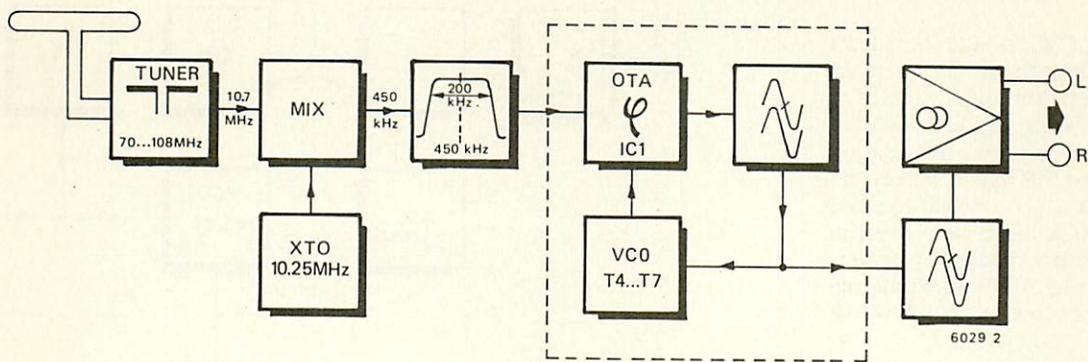
Figure 1. Block diagram of a receiver for narrow-band FM transmissions in the 144 MHz-146 MHz amateur band, with a fixed-frequency mixing oscillator and band-spread tuning by varying the intermediate frequency.

signal and the oscillator output: hence the term 'phase-locked loop'.

By definition, the oscillator is voltage-controlled. So if the incoming signal is frequency-modulated, the control voltage applied to the oscillator to keep it synchronised becomes, of itself, the demodulation of the incoming signal. As



2



a method of detection, this has important advantages over other methods in terms of better rejection of interfering signals, lower distortion, and better signal-to-noise ratio.

**Circuit description**

The input is fed in across resistor R1 (figure 3). The value of this resistor must be selected to give correct matching to the preceding mixer stage, and suitable values will be given in later articles describing particular applications. Transistors T1 and T2 form a differential amplifier with an asymmetrical input, while T3 and diodes D1 and D2 stabilise the current flowing through T1 and T2. The two collectors of the differential amplifier are connected through capacitors C4 and C5 to the two differential inputs (2 and 3) of the CA3080 operational transconductance amplifier IC1. The use of both inputs in this fashion gives an extra 6 dB

gain without impairing stability and also facilitates the operation of the limiting diodes D3 and D4.

In addition to receiving the RF (or IF) signal at the differential inputs (pins 2 and 3), IC1 is fed via pin 5 with the output of the voltage-controlled oscillator formed by T4 and T5. Although this oscillator is described as voltage-controlled, it should more properly be called current-controlled, the current being regulated by T6 and T7 in the emitter leads of T4 and T5 respectively. It can, however, be said without too much straining of the truth that the commoned bases of T6 and T7 are voltage-controlled from the output (pin 6) of IC1.

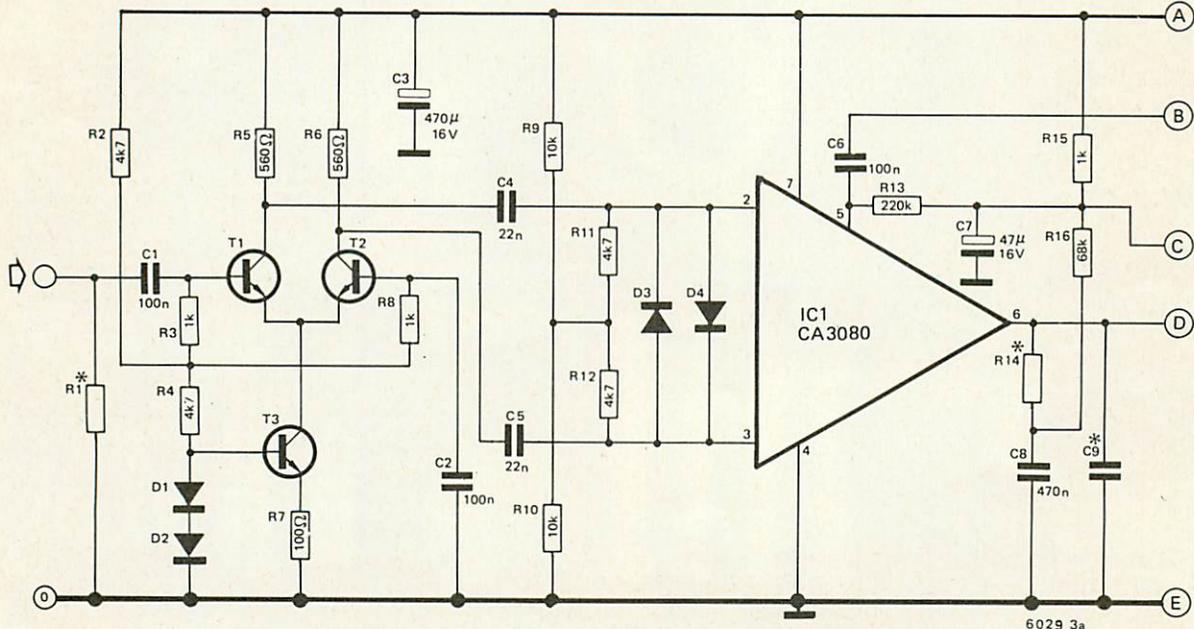
In the foregoing description the path of the loop has, in effect, been followed in the reverse direction. Recapping and going the correct way round: the DC component of the signal at pin 6 of the phase-comparator IC1 is amplified by

T6 and T7 and controls the frequency of oscillator T4 + T5.

As in all FM detectors, AM rejection is important. The CA 3080 has good AM rejection at low input-signal levels, but is less good at higher levels. These higher levels, however, are taken care of by the clipping diodes D3 and D4, which begin contributing to AM rejection when the peak-to-peak signal between pins 2 and 3 of IC1 exceeds 1 volt.

Capacitor C11 is one of the components whose value influences the VCO free-running frequency (455 kHz in the broadcast FM receiver, or about 10 MHz in the narrow-band FM receiver) so its value is quoted for particular applications (see Table). When the receiver is tuned by varying the VCO frequency, as in the narrow-band FM receiver, potentiometers P1 and P2 come into play. When the working IF frequency is fixed, these potentiometers can be used for preset adjustment.

3a



\* see text

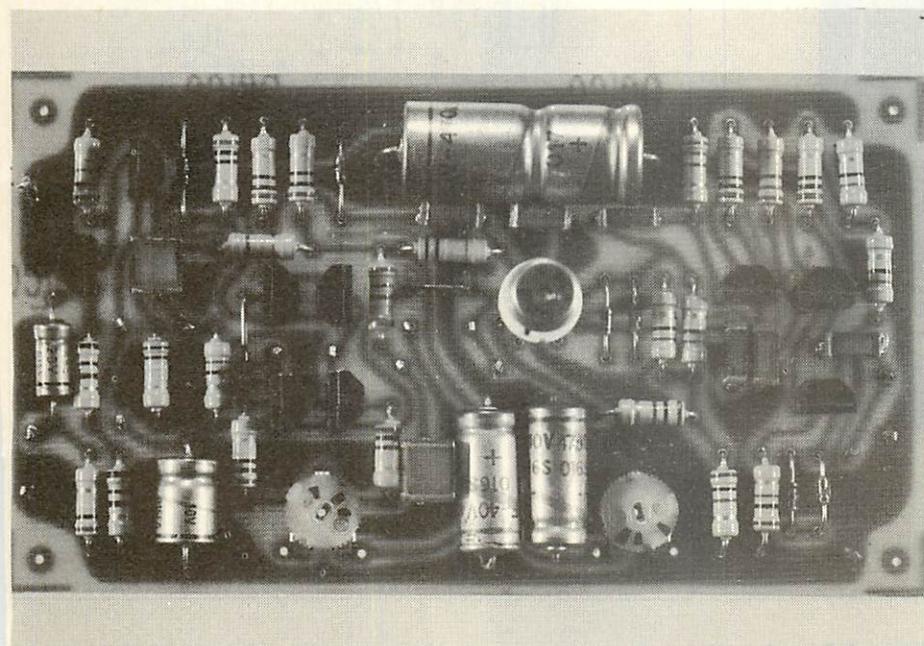
Figure 2. Block diagram of a double super-heterodyne for stereo FM reception, with intermediate frequencies of 10.7 MHz and 455 kHz.

Figure 3. Circuit of the Universal OTA PLL.

Table: Values of R1, R14, R24, C9, C11 and C14 for specific applications.

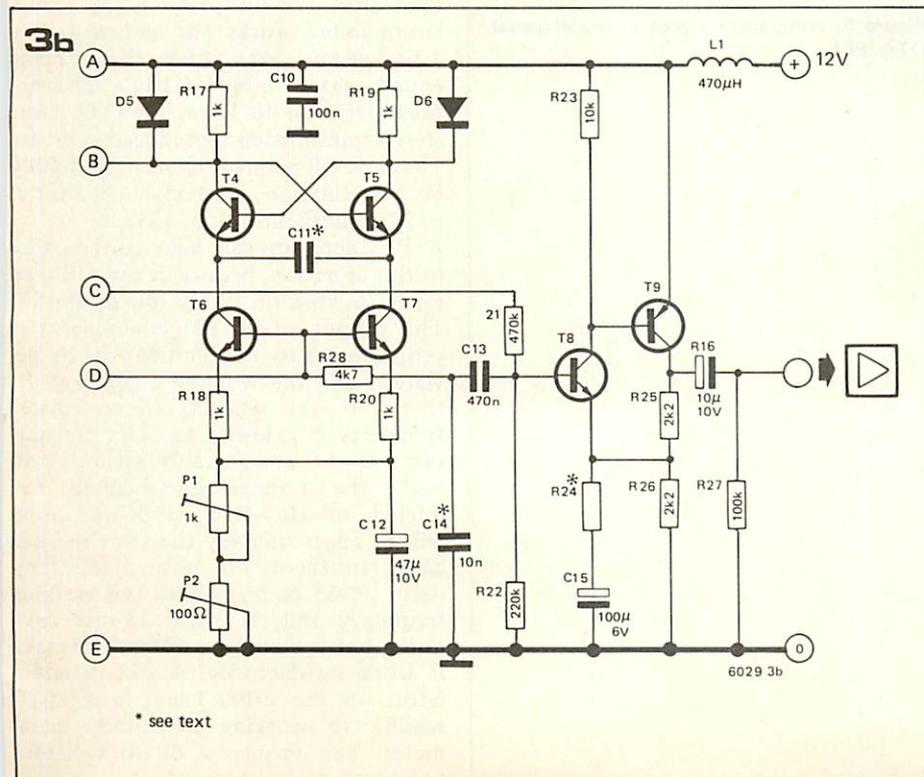
Mode of operation (all FM)			Supply voltage	R1	R14	R24	C9	C11	C14
Type of transmission	Intermediate frequency	Minimum input *							
Wide band mono	10.7 MHz	160 $\mu$ V	9	330 $\Omega$	1 k	150 $\Omega$	—	100 p	10 n
Narrow band	10.7 MHz	3.2 $\mu$ V	9	330 $\Omega$ -2k2	47 k	0 $\Omega$	—	220 p	10 n
Wide band mono	455 kHz	400 $\mu$ V	9	—	47 k	2k2	560 p	2n2	10 n
Narrow band	455 kHz	20 $\mu$ V	9	3k3	47 k	82 $\Omega$	560 p	2n2	10 n
Wide band stereo	455 kHz	500 $\mu$ V	9	—	47 k	2k2	220 p	2n2	—
Wide band stereo	455 kHz	200 $\mu$ V	12	—	47 k	2k2	220 p	2n2	—

\* At the PLL! (— = omitted)



The low-pass filter which removes the unwanted 'sum' frequency (oscillator plus input signal) is formed by C8, C9, R14 and R16. As the values of these resistors also effect the VCO free-running frequency, they have to be selected carefully for each application. In practice, R16 is given a fixed value of 68 k $\Omega$  while R14 is specified for each application. This also applies to the feedback resistor R24 which controls the gain of the output audio amplifier T8 and T9. Resistor R28 and capacitor C14 provide de-emphasis. It will be seen that the whole of the DC component at the output (pin 6) of the phase comparator is passed to the VCO: this helps to ensure a large 'hold range' for the loop.

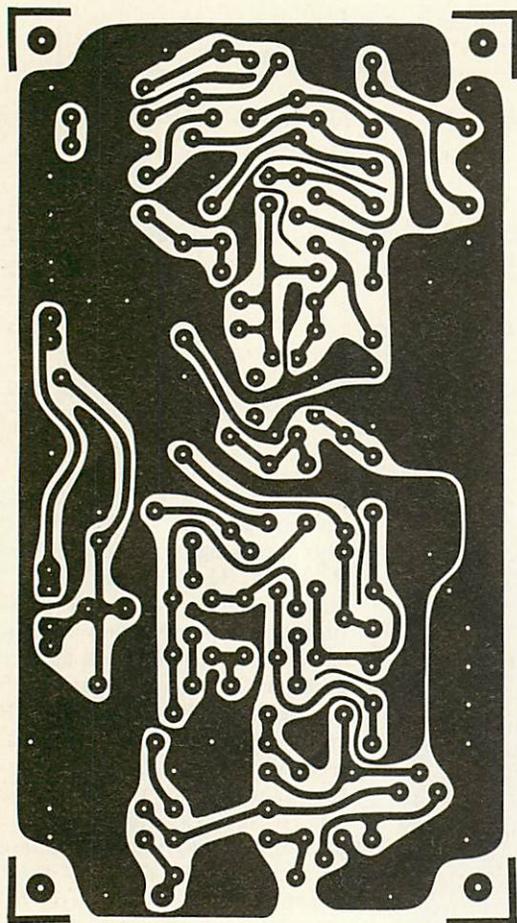
Detailed descriptions of applications of the Universal PLL will be given in later articles, but the two which have already been mentioned can be briefly discussed here.



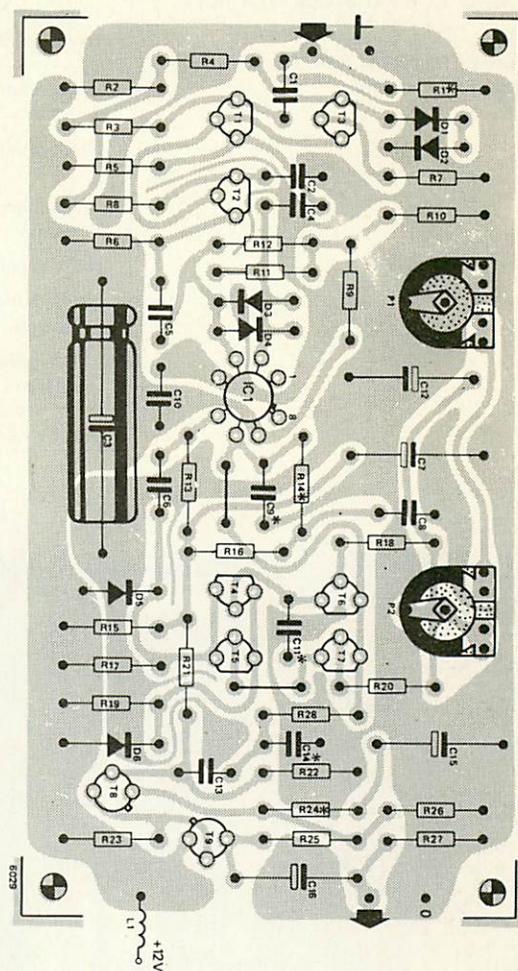
- Resistors:**  
 R1, R14, R24 = see table  
 R2, R4, R11, R12, R28 = 4k7  
 R3, R8, R15, R17, R18, R19, R20 = 1 k  
 R9, R10, R23 = 10 k  
 R5, R6 = 560  $\Omega$   
 R7 = 100  $\Omega$   
 R27 = 100 k  
 R13, R22 = 220 k  
 R16 = 68 k  
 R21 = 470 k  
 R25, R26 = 2k2  
 P1 = 1 k  
 P2 = 100  $\Omega$
- Capacitors:**  
 C1, C2, C6, C10 = 100 n  
 C3 = 470  $\mu$ /16 V  
 C4, C5 = 22 n  
 C7 = 47  $\mu$ /16 V  
 C8, C13 = 470 n  
 C9, C11, C14 = see table  
 C12 = 47  $\mu$ /10 V  
 C15 = 100  $\mu$ /6 V  
 C16 = 10  $\mu$ /10 V
- Semiconductors:**  
 T1 ... T7 = BF 494  
 T8 = BC 547  
 T9 = BC 557  
 IC1 = CA 3080  
 D1 ... D6 = 1 N 4148
- Inductor:**  
 L1 = 470  $\mu$ H

\* see text

4



5



### Narrow-band FM receiver

In narrow-band FM systems, noise always tends to be a problem because the modulation index (the ratio of the maximum deviation to the highest modulation frequency) is by definition low, but the good noise performance of a PLL demodulator goes a long way towards overcoming this handicap. The limiting sensitivity of the Universal PLL, when used in a narrow-band FM receiver, has already been stated to be  $3.2 \mu\text{V}$ , not counting the gain of the RF and mixer stages preceding it. With an input of  $4 \mu\text{V}$  — slightly above the limiting value — the signal-to-noise ratio is 40 dB.

The principle of using a crystal-controlled fixed-frequency local oscillator, and tuning the IF with the VCO, offers a very simple and effective form of band-spreading.

### Stereo FM receiver

FM sound broadcasting has a maximum deviation of 75 kHz, which gives a modulation index of 5 on mono transmissions having a 15-kHz audio bandwidth. With a stereo transmission, the maximum modulation frequency is 53 kHz, but the effective bandwidth of

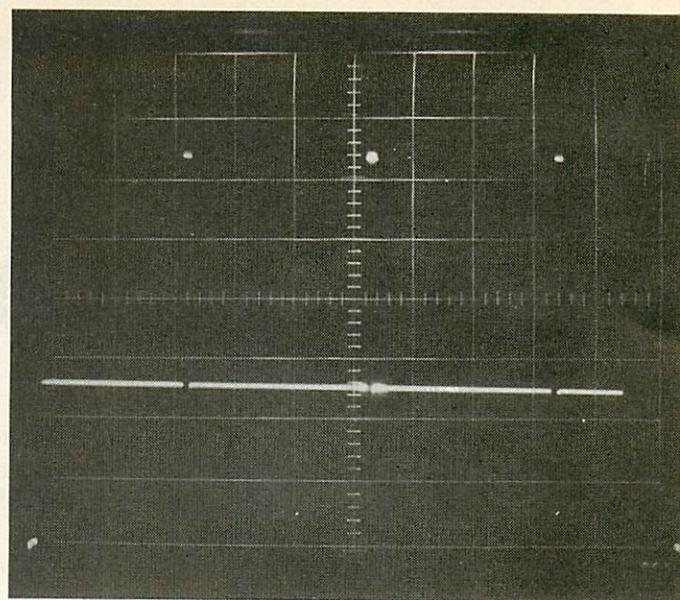
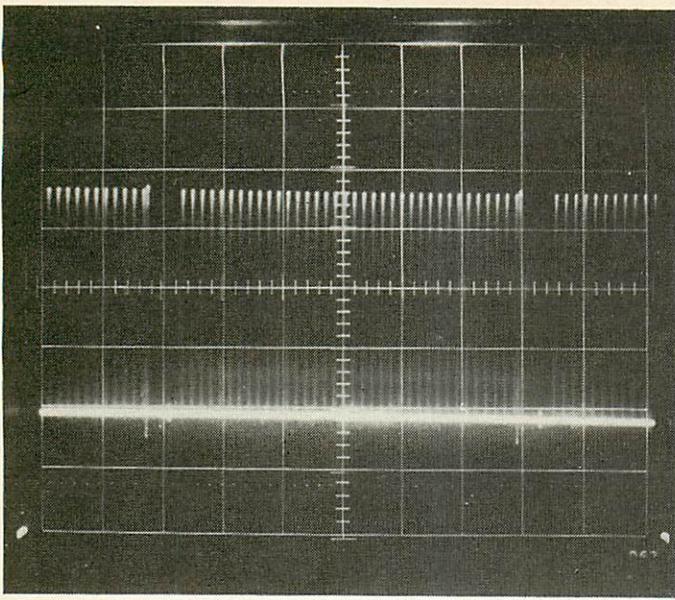
Figure 4. Printed circuit board.

Figure 5. Component layout of the universal OTA PLL.

the composite stereo signal is greater than this, and in practice the modulation index works out as low as 0.6. This means that, 'other things being equal', stereo reception has a signal-to-noise ratio 20 dB lower than the same stereo transmission reproduced in mono. These problems are discussed more fully in 'Modulation Systems' (Elektor 2, p. 246 and Elektor 3, p. 454).

A PLL detector can help considerably in this situation, because it can easily be made to work on a very low second IF. The output of an FM demodulator is proportional to the quotient of the deviation and the working frequency. If, therefore, the working (intermediate) frequency is as low as 455 kHz, the output will be considerably greater than with the normal intermediate frequency of 10.7 MHz, while the noise will be approximately the same in both cases. In theory, a 'normal' discriminator could be made with this working frequency and the usual 75-kHz deviation, but it would be difficult to make it work satisfactorily. A PLL demodulator, on the other hand, lends itself readily to working with these parameters and enables a 60-dB signal-to-noise ratio to be obtained.

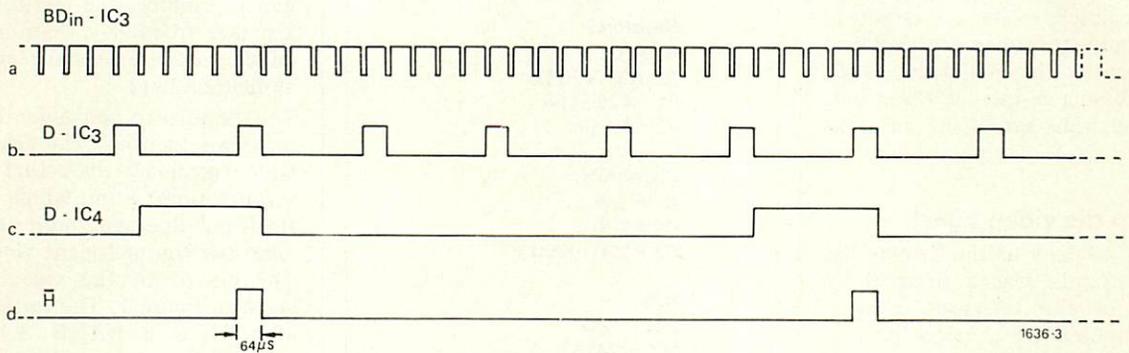




2

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5

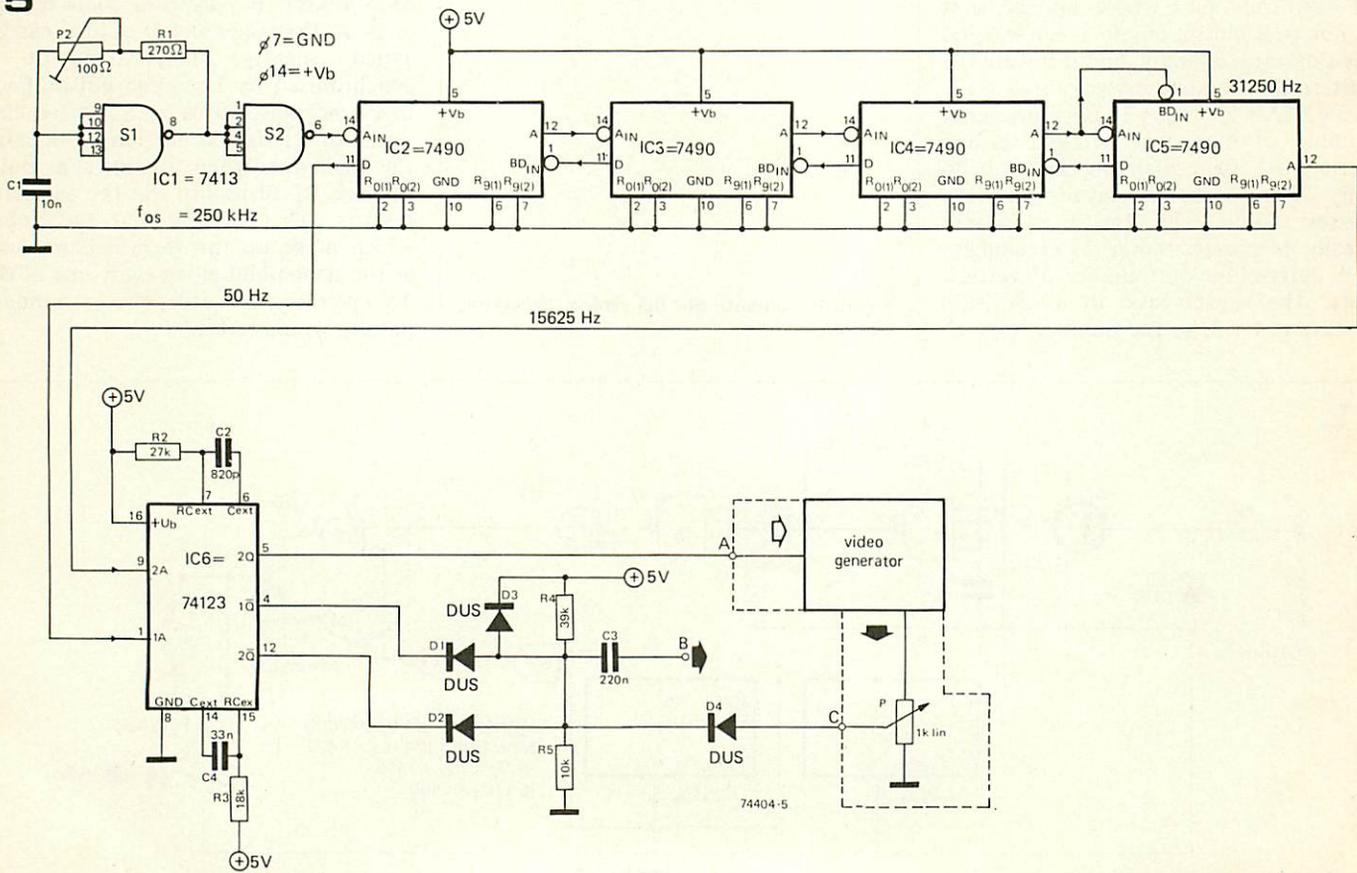


Figure 2. Oscillogram of the  $\bar{V}$  signal at the output of N1.

Figure 3. Timing diagram for the generation of the H signal.

Figure 4. Oscillogram of the  $\bar{H}$  signal.

Figure 5. Circuit of the sync generator, showing connections to the video generator.

Figure 6. P.c. board and component layout for the video generator.

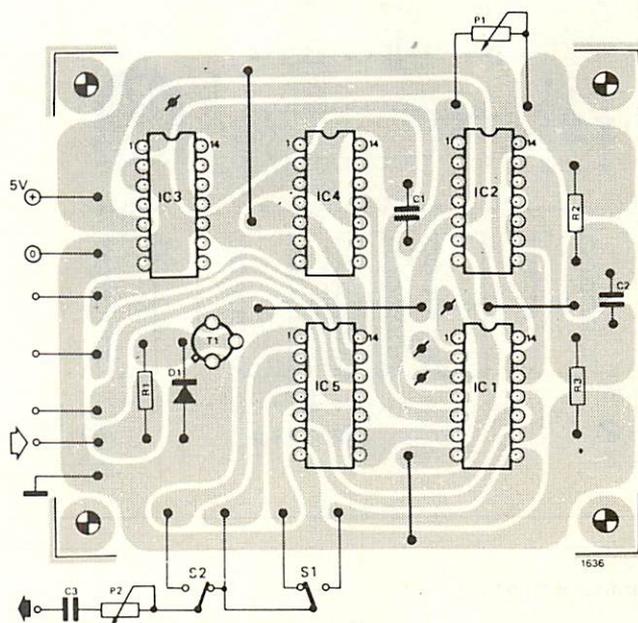
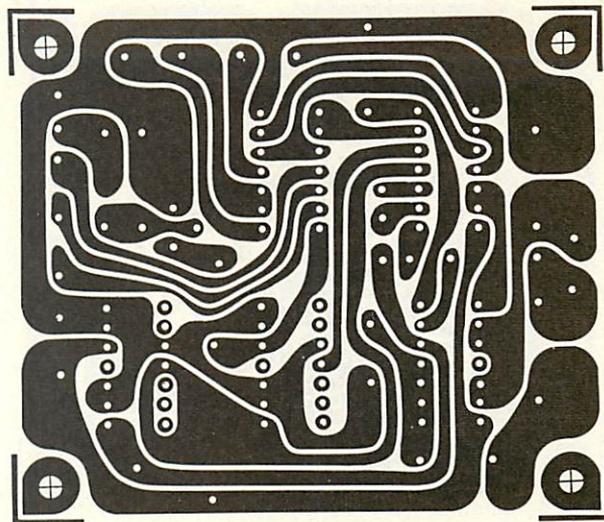
Figure 7. Photograph of the completed video generator.

The output of the astable has substantially a 1:1 mark space ratio. This would, if used as the video signal, produce black and white vertical bands of equal thickness. However, for the purposes of the pattern generator very narrow bands provide more information about the state of the video stages of the TV, since a narrow band requires a shorter pulse length and hence a greater bandwidth.

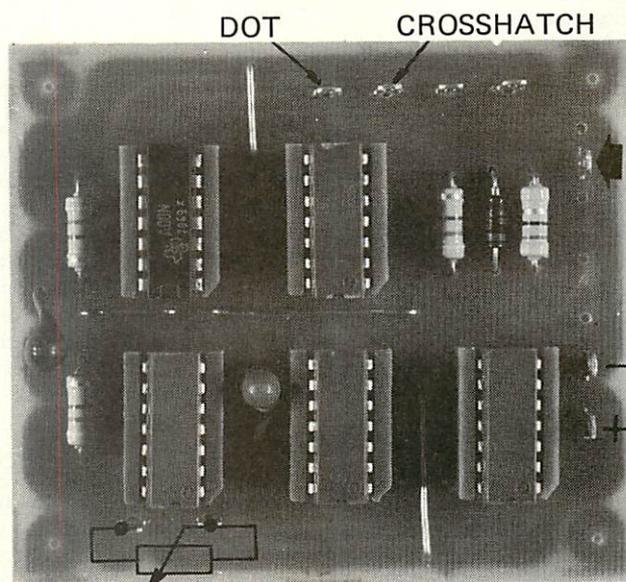
Accordingly the output of the astable is differentiated by C2 and R3, and the spiky pulses are fed into a second Schmitt trigger to square them up again. This also inverts the signal, so it is inverted a second time by N1 to appear in the correct sense. Figure 2 shows the vertical signal  $\bar{V}$  as it appears at the output of N1. The absence of pulses where the sync pulses occur can be clearly seen. The pulse length of the  $\bar{V}$  signal is about 200 ns.

Line sync pulses at the collector of T1 are also counted by IC3 and IC4, which are 7490's connected as divide-by-five counters. Output D of IC4 is therefore a pulse train at 1/25 of line frequency. The timing diagram for this division is shown in figure 3. Waveform 'a' is the line sync input. Waveform 'b' is the D output of IC3, and waveform 'c' is the D output of IC4. However, this waveform cannot be used directly as the horizontal video signal, as the pulse length is equal to 5 line periods, which would make the horizontal bars too thick. For this reason it is 'NANDed' with waveform 'b' in N2 and then inverted by N3 to produce waveform 'd' ( $\bar{H}$ ). This has a duration of 64  $\mu$ s or one line period. However, due to interlace each horizontal bar will actually have a thickness of two lines. Figure 4 shows an oscillogram of the  $\bar{H}$  signal. To produce the complete video signal the  $\bar{H}$  and  $\bar{V}$  signals must be summed. To produce the crosshatch pattern the horizontal and vertical signals must be 'OR-d' together, as there must be a bar when vertical or horizontal pulses are present. For the dot pattern, which corresponds to the crossing points of

6



7



8

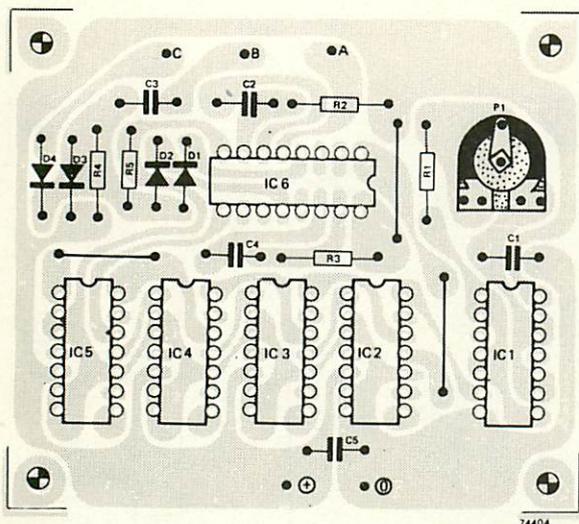
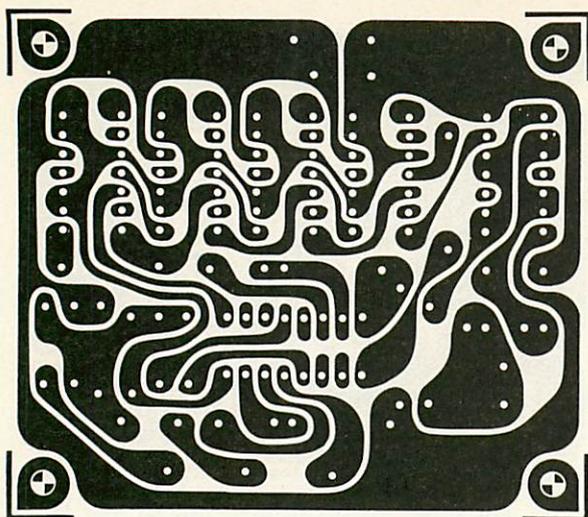


Figure 8. P.c. board and component layout for the sync generator.

Figure 9. Photograph of the completed sync generator.

critical, and several turns of insulated connecting wire a few cm diameter should prove suitable. The video signal is then taken from P1 via C3 and is injected into the video stages of the TV. P1 adjusts the video level so that the signal does not interfere with the synchronisation of the set.

A more elegant solution is to employ a built-in sync generator, the circuit of which is given in figure 5. Again a Schmitt trigger operates as an astable multivibrator, this time at a frequency of 250 kHz. The divide-by-two stages of four 7490's are used to divide this down to the line frequency of 15625 Hz. The 50 Hz field sync pulses are produced by taking the output of the third divide-by-two stage (31250 Hz) and feeding it back through the divide-by-five stages of the four 7490's. Since the field and line sync pulses must have pulse lengths of about 250  $\mu$ s and 4  $\mu$ s respectively the 50 Hz and 15625 Hz outputs are used to trigger the two halves of a 74123 dual multivibrator, with appropriate time constants.

The line sync pulses are used to trigger the video generator, and are also mixed with the field sync pulses and the video signal using the diode-resistor mixer network. Note that the output capacitor of the video generator is replaced by D4 in this circuit. The video output is taken from point B, and may be injected directly into the video stages of the TV set. Alternatively, the VHF/UHF modulator for the TV-tennis (described elsewhere in this issue) can be used.

### Construction

A printed circuit board and component layout for the video generator are shown in figure 6, and for the sync generator in figure 8. Photographs of the completed boards are shown in figures 7 and 9.

### Parts list for figures 5 and 7

#### Resistors:

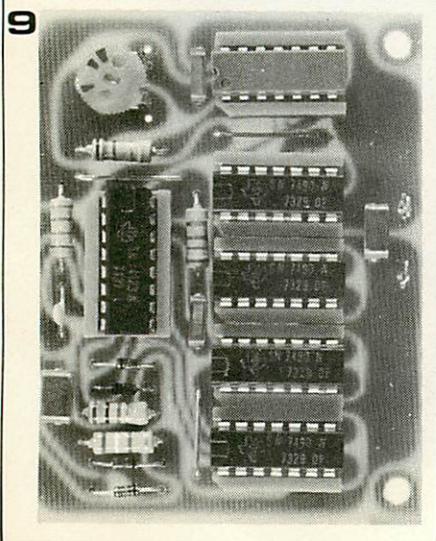
R1 = 270  $\Omega$   
 R2 = 27 k  
 R3 = 18 k  
 R4 = 39 k  
 R5 = 10 k  
 P1 = 1 k lin. (part of video generator)  
 P2 = 100  $\Omega$  preset

#### Capacitors:

C1 = 10 n  
 C2 = 820 p  
 C3 = 220 n  
 C4 = 33 n

#### Semiconductors:

IC1 = 7413  
 IC2 - IC5 = 7490  
 IC6 = 74123  
 D1 - D4 = DUS



the horizontal and vertical bars, the pattern must appear only when horizontal and vertical information are present. The  $\bar{H}$  and  $\bar{V}$  signals are thus ANDed together. These functions are performed by N4 and N5 respectively, and S1 selects the pattern. N6 and S2 provide the option of a positive or negative pattern i.e. white pattern on black background or black pattern on white ground. Note that peak white corresponds to logic '0'.

It is possible to use this circuit as it stands without any additional circuitry. This is accomplished by tuning the set to a station so that sync pulses are available from the transmission. The circuit may be triggered by picking up line flyback pulses from the line output transformer using a pickup coil. The dimensions of this coil are not at all

W. Schmidt

# with a pencil point

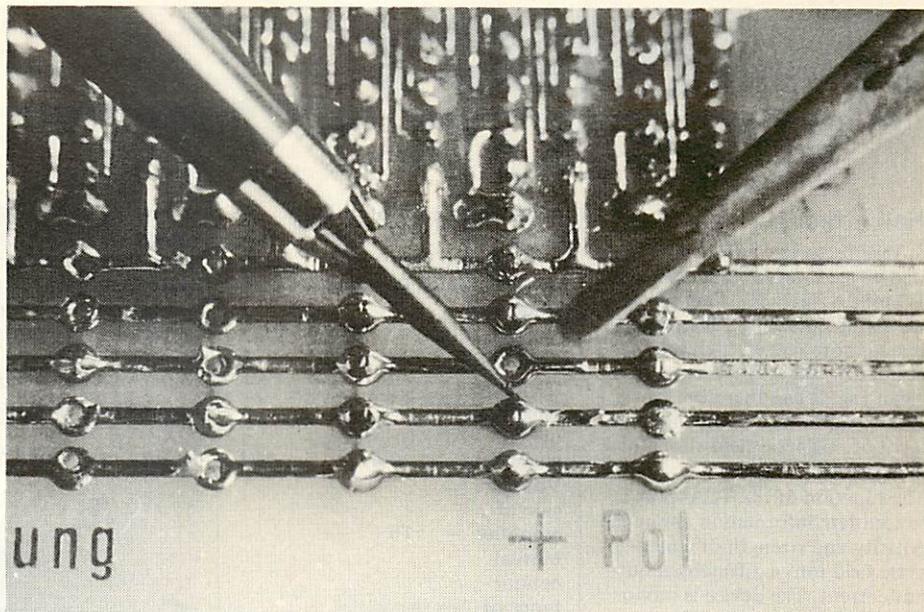
Many electronics enthusiasts look on solder removing as a loathsome job. This is especially true of printed circuit boards with narrowly-spaced conductors. Things which often happen when one is trying to desolder are:

The solder forms bridges between the conductors.

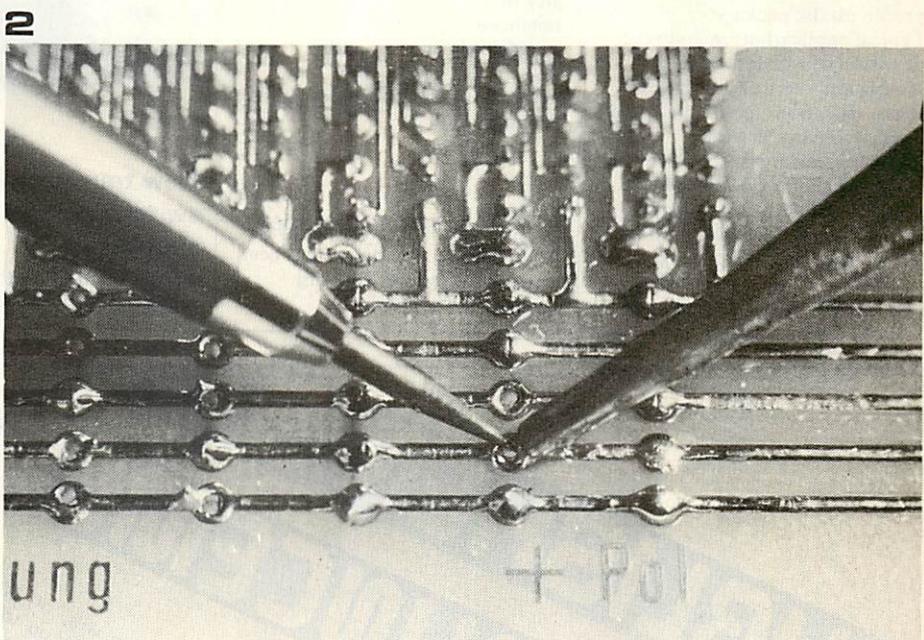
Blobs of solder drop off the board.

De-soldering tools or wicks are available commercially, but there is no need to pay out that kind of money. Any workshop toolbox should yield a really cheap device which will do the trick - a pencil. Propelling pencils with long leads of 2B or B hardness are particularly suitable (e.g. clutch pencils). To remove solder from a hole, the solder must be heated with a soldering iron until it melts (figure 1). The next step is to stick the pencil point in the hole, and take away the iron (figure 2). Where the pencil lead touches molten solder, the solder 'jumps' away, because of its surface tension, and the hole is cleared of solder (figure 3).

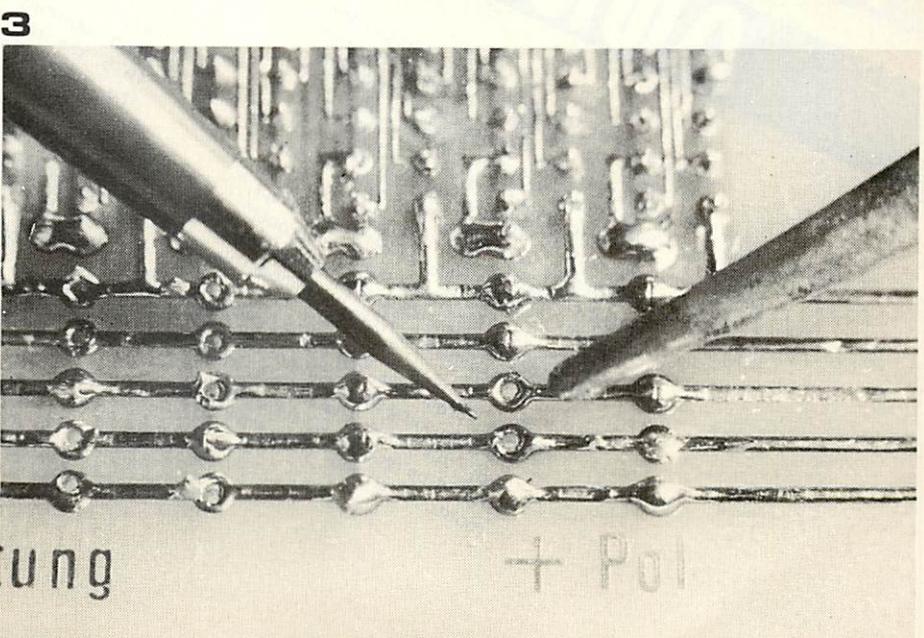
A similar method can be used for getting rid of bridges of solder between tracks. To do this, the pencil point is laid flat on the molten solder between the tracks.



1



2



3





In connection with the rapid growth of Elektor, we are now looking for an

# assistant editor

Applicants should have a sound knowledge of electronics and an ability to write lucidly on that subject. Previous journalistic experience is not essential but would be an advantage, as would a knowledge of the German language.

The successful applicant will have the opportunity to assist in the technical development of our magazine. Conditions of employment: attractive salary, 37½ hour week, 8.3% holiday bonus and 3.5% Christmas bonus, etc.

Applications with career details should be addressed to the Managing Director, Elektor Publishers Ltd, 6 Stour Street, Canterbury CT1 2XZ.

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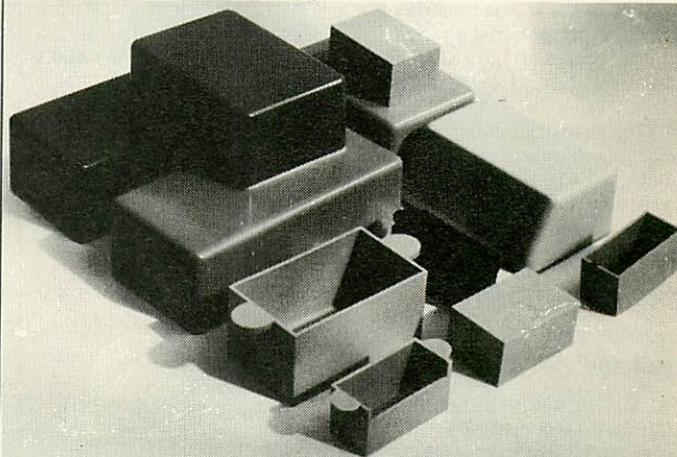
### Missing link

The most recent experiments with the TAP-power (this issue, page 1130) have shown that the most reliable circuit for the touch inputs is as follows:

- capacitors  $C_a$  and  $C_d$  are included across the touch contacts,  $C_b$  and  $C_c$  are omitted;
- the connections from the touch panels to the main pcb are made via  $1\text{ M}\Omega$  series resistors instead of wire links, e.g. a  $1\text{ M}\Omega$  resistor connects the junction of the 'ON' touch panel and  $C_a$  to the junction of R20 and pin 8 of N1.

## PLASTIC BOXES

Two new ranges of ABS plastic boxes are offered at competitive prices and with short deliveries. The first range, for electronic circuits and controls, gives volumes from 348 to 1,369 cc in four sizes.



The second, for potting, gives 41 to 187 cc in three sizes. ABS material is said to be antistatic, easily punched and drilled, and capable of withstanding  $100^\circ\text{C}$ . Standard colours offered are grey, blue, orange and red.

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3 Crown Buildings, Crown Street, London SE5.

# MARKET



## Mercury-wetted relays

From Astralux Dynamics Limited, the 270/280 series of miniature mercury-wetted reed relays are ideal for low-level switching applications. The mercury wetting of the relay contacts eliminates electrical contact 'bounce' and gives a stable contact resistance (initial contact rating 0.05  $\Omega$  maximum).

The avoidance of spurious operation means that the devices are suitable for interfacing with low-level logic equipment, while the relatively high power ratings enable the relays to be used for switching inductive loads. The life expectancy is also increased: up to  $50 \times 10^6$  operations.

The relays are available in 1 Form A, 2 Form A, 1 Form C and 2 Form C configurations.

Ratings for the Form A types are: breakdown 1.2 kV d.c. minimum; switching 200 V, 1 mA and 28 W, 1 A (1 kV d.c. and 2 A d.c. maximum); d.c. contact rating 50 W maximum. The corresponding figures for the Form C types are: breakdown 1 kV d.c. minimum; switching 200 V, 1 mA and 28 W, 1 A (200 V d.c. and 1 A d.c. maximum); d.c. contact rating 14 W maximum.

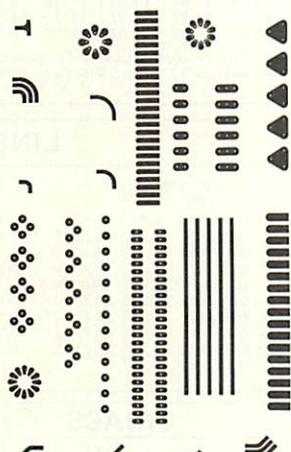
*Astralux Dynamics Limited, Brightlingsea, Colchester, Essex, CO7 0SW.*

## P.C.B. Transfer System

This system, from J.H. Equipment Ltd allows the production of high-quality one-off printed circuits without recourse to photography. The etch-resistant pads and tracks are laid out on the copper side of the board and the resulting circuit can then be etched. The manufacturers claim that their method of applying the adhesive to the symbols gives better definition than similar systems, as there is no ad-

hesive overlap which can produce ragged edges.

The system is available in kits of ten sheets of symbols as illustrated.



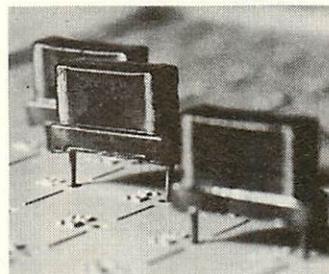
## Metallised plastic film capacitors

Designated Type MKM, these capacitors are the latest in a series developed by Siemens and feature exceptional compactness, stability, low loss and close tolerance. They have been introduced principally for use in completely automated production systems but, in a protected version, are also well suited to applications in both professional and semi-professional electronic equipment.

Individual capacitors are cut from a large 'mother' capacitor of known value, on which many of the processes necessary to the production of discrete units have already been carried out. In this way a uniformity of the electrical characteristics of the capacitors is achieved, which is not possible when produced individually. Currently, LST Electronic Components stock the B32551 version of the MKM capacitor. This is available at voltage ratings of

100 V d.c. and preferred values of 10 to 68 nF, and at 250 V d.c. and preferred values of 100, 150 and 220 nF. The pin spacing of the B32551 is 10 mm.

*LST Electronic Component Ltd, Victoria Road, Chelmsford, Essex.*



## Inexpensive Programmable Op-Amp

A single external resistor allows the characteristics of a new Motorola op-amp to be optimised to suit power supplies from  $\pm 6$  to  $\pm 15$  V. Parameters which are programmed by the external resistor include input current and voltage, power consumption and current noise. The new op-amp, designated type

MC3476, does not require frequency compensation, has offset null capability and is fully protected against damage from short circuits. A typical power consumption of only 4.8 mW makes the MC3476 a good choice for use in battery powered equipment. The data sheet gives the typical offset voltage, offset current and bias current as 2 mV, 2 nA and 15 nA respectively. Input resistance and capacitance are 5 M $\Omega$  and 2 pF, while input common-mode voltage range, and supply voltage rejection ratios are quoted as  $\pm 10$  V, 70 dB and 25  $\mu$ V/V respectively. The output resistance is 1 k $\Omega$  and the output current into a short circuit is typically 12 mA. From the performance point of view the MC3476 offers a minimum large signal voltage gain of 50 kV/V (min) with a 10 k $\Omega$  load and an output voltage swing of  $\pm 10$  V at 25°C. Slew rate with the same load is 0.8 V/ $\mu$ sec and the unity gain transient response is typically 0.35  $\mu$ sec.

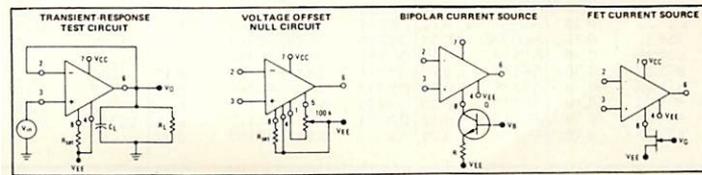
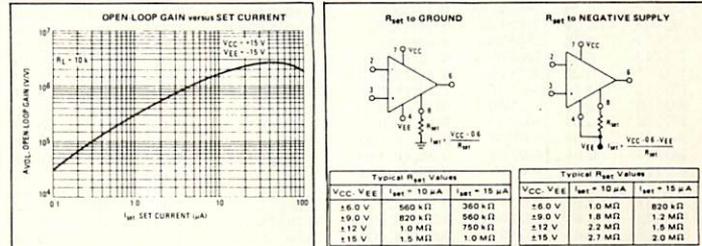
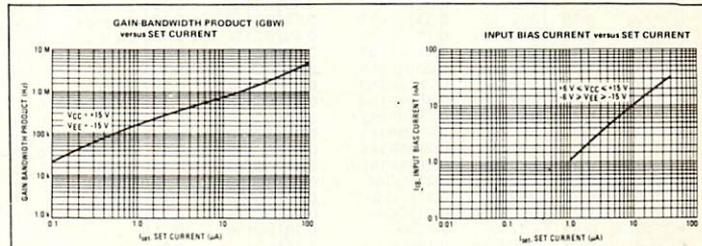
*Motorola Ltd, Semiconductor Products Division, York House Empire Way, Wembley, Middlesex.*

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Semiconductor Products Division

Technical Press Information

### MC3476

PROGRAMMABLE OPERATIONAL AMPLIFIER



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AC113	0.19	BSY41	0.29	AF126	0.29	P397	0.43	BF176	0.36
AC115	0.20	BSY95	0.13	AF127	0.29	ST140	0.13	BF177	0.36
AC117K	0.30	BSY95A	0.13	AF139	0.31	ST141	0.18	BF178	0.31
AC122	0.12	BU105	£2.04	AF178	0.51	TIP29	0.44	BF179	0.31
AC125	0.18	C111E	0.51	AF179	0.51	TIP30	0.52	BF180	0.31
AC126	0.18	C400	0.31	AF180	0.51	TIP31A	0.56	BF181	0.31
AC127	0.19	C407	0.26	AF181	0.51	TIP32A	0.68	BF182	0.41
AC128	0.19	C424	0.26	AF186	0.51	TIP41A	0.68	BF183	0.41
AC132	0.15	C425	0.51	AF239	0.38	TIP42A	0.81	BF184	0.26
AC134	0.15	C426	0.36	AL102	0.68	TIS43	0.31*	BF185	0.31
AC137	0.15	C428	0.20	AL103	0.68	UT46	0.28*	BF187	0.28
AC141	0.19	C441	0.31	ASV26	0.26	ZN414	1.11	BF188	0.41
AC141K	0.30	C442	0.31	ASV27	0.31	ZG301	0.19	BF194	0.12
AC142	0.19	C444	0.36	ASV28	0.26	ZG302	0.19	BF195	0.12
AC142K	0.26	C450	0.36	ASV29	0.26	ZG303	0.19	BF196	0.15
AC151	0.16	MAT100	0.19	ASV50	0.26	ZG304	0.25	BF197	0.15
AC154	0.20	MAT101	0.20	ASV51	0.26	ZG306	0.41	BF200	0.46
AC155	0.20	MAT120	0.19	ASV52	0.26	ZG308	0.36	BF222	0.98
AC156	0.20	MAT121	0.20	ASV54	0.26	2N2926 G	0.13	BF257	0.46
AC157	0.25	MJE521	0.56	ASV55	0.26	2N2926 Y	0.11	BF258	0.61
AC165	0.20	MJE2955	0.88	ASV56	0.26	2N2926 O	0.10	BF259	0.87
AC166	0.20	MJE3055	0.57	ASV57	0.26	2N2926 R	0.10	BF262	0.56
AC167	0.20	MJE3440	0.51	ASV58	0.26	2N2926 B	0.10	BF263	0.56
AC168	0.25	MPF102	0.43	ASV73	0.26	2N3010	0.71	BF270	0.36
AC169	0.15	MPF104	0.38	ASZ21	0.41	2N3011	0.15	BF271	0.31
AC176	0.20	MPF105	0.38	BC107	0.08	2N3053	0.18	BF272	0.81
AC177	0.25	OC19	0.36	BC108	0.08	2N3054	0.47	BF272	0.81
AC178	0.29	OC20	0.65	BC109	0.08	2N3055	0.42	BF273	0.36
AC179	0.29	OC22	0.47	BD136	0.41	2N3319	0.15	BF274	0.36
AC180	0.20	OC23	0.49	BD137	0.46	2N3391 A	0.17	BFW20	0.61
AC180K	0.30	OC24	0.57	BD138	0.51	2N3392	0.15	BFX29	0.28
AC181	0.20	OC25	0.39	BD139	0.56	2N3393	0.15	BFX84	0.22
AC181K	0.30	OC26	0.30	BD140	0.61	2N3394	0.15	BFX85	0.21
AC187	0.22	OC28	0.51	BD155	0.81	2N3395	0.18	BFX86	0.22
AC187K	0.23	OC29	0.51	BD175	0.61	2N3402	0.21	BFX87	0.25
AC188	0.22	OC35	0.43	BD176	0.61	2N3403	0.21	BFX88	0.22
AC188K	0.23	OC36	0.51	BD177	0.67	2N3404	0.29	BFY50	0.20
ACY17	0.26	OC41	0.20	BD178	0.67	2N3405	0.43	BFY51	0.20
ACY18	0.20	OC42	0.25	BD179	0.71	2N3414	0.16	BFY52	0.20
ACY19	0.20	2N918	0.31	BD180	0.71	2N3415	0.16	ZC309	0.37
ACY20	0.20	2N929	0.21	BD185	0.67	2N3416	0.29	ZC339	0.20
ACY21	0.20	2N930	0.21	BD186	0.67	2N3417	0.29	ZC339A	0.17
ACY22	0.17	2N1131	0.20	BD187	0.71	2N3525	0.77*	ZG344	0.19
ACY27	0.19	2N1132	0.22	BD188	0.71	2N3614	0.69	ZG345	0.17
ACY28	0.19	2N1302	0.15	BD189	0.77	2N3615	0.76	ZG371	0.17
ACY29	0.36	2N1303	0.15	BD190	0.77	2N3616	0.76	ZG371B	0.12
ACY30	0.29	2N1304	0.18	BD195	0.87	2N3646	0.09	ZG373	0.18
ACY31	0.29	2N1305	0.18	BD196	0.87	2N3702	0.12	ZG374	0.18
ACY34	0.21	2N1306	0.21	BD197	0.92	2N3703	0.12	ZG377	0.31
BC173	0.15	2N1307	0.21	BD198	0.92	2N3704	0.13	ZG378	0.17
BC174	0.15	2N1308	0.24	BD199	0.98	2N3705	0.12	ZG381	0.17
BC175	0.22	2N1309	0.24	BD200	0.98	2N3706	0.12	ZG382	0.17
BC177	0.19	2N1513	0.20	BD205	0.81	2N3707	0.13	ZG401	0.31
BC178	0.19	2N1711	0.20	BD206	0.81	2N3708	0.08	ZG414	0.31
BC179	0.19	2N1889	0.32	BD207	0.98	2N3709	0.09	ZG417	0.26
BC180	0.25	2N1890	0.46	BD208	0.98	2N3710	0.09	2N388	0.36
BC181	0.25	2N1893	0.33	BDY20	£1.02	2N3711	0.09	2N388A	0.56
BC182	0.15	2N2147	0.73	BF115	£1.02	2N3819	0.29	2N404	0.20
BC182L	0.15	2N2148	0.58	BF117	0.46	2N3820	0.51	2N404A	0.29
BC183	0.15	2N2192	0.36	BF118	0.71	2N3821	0.36	2N524	0.43
BC183L	0.15	2N2193	0.36	BF119	0.71	2N3823	0.29	2N527	0.50
BC184	0.20	2N2194	0.36	BF121	0.46	2N3823	0.29	2N598	0.43
BC184L	0.20	2N2217	0.22	BF123	0.51	2N3904	0.31	2N599	0.46
BC186	0.29	2N2218	0.20	BF125	0.46	2N3905	0.29	2N696	0.13
BC187	0.29	2N2219	0.20	BF127	0.51	2N3906	0.28	2N697	0.14
BC207	0.11	2N2220	0.20	BF152	0.56	2N4058	0.12	2N698	0.25
BC208	0.11	2N2221	0.20	BF153	0.46	2N4059	0.10	2N699	0.36
BC209	0.12	2N2222	0.20	BF154	0.46	2N4060	0.12	2N706	0.08
BC212L	0.18	2N2368	0.18	BF155	0.71	BC113	0.10	2N706A	0.09
BC213L	0.13	2N2369	0.15	BF156	0.49	BC114	0.16	2N708	0.12
BC214L	0.17	2N2369A	0.15	BF157	0.56	BC115	0.16	2N711	0.31
BC225	0.26	2N2411	0.25	BF158	0.56	BC116	0.16	2N717	0.36
BC226	0.36	2N2412	0.25	BF159	0.61	BC117	0.19	2N718	0.18
BC301	0.28	2N2646	0.48	BF160	0.41	BC118	0.10	2N718A	0.25
BC302	0.25	2N2711	0.21	BF162	0.41	BC119	0.81	2N726	0.29
BC303	0.31	2N2712	0.21	BF163	0.41	BC120	0.81	2N727	0.29
BC304	0.37	2N2714	0.21	BF164	0.41	BC125	0.12	2N743	0.20
BC440	0.31	2N2904	0.18	BF165	0.41	BC126	0.19	2N744	0.20
BC460	0.37	2N2904A	0.21	OC44	0.16	BC132	0.12	2N914	0.15
BCY30	0.25	2N2905	0.21	OC45	0.13	BC134	0.19	2N4061	0.12
BCY31	0.27	2N2905A	0.21	OC70	0.10	BC135	0.12	2N4062	0.12
BCY32	0.31	2N2906	0.16	OC71	0.10	BC136	0.16	2N4284	0.18
BCY33	0.22	2N2906A	0.19	OC72	0.15	BC137	0.16	2N4285	0.18
BCY34	0.26	2N2907	0.20	OC74	0.15	BC139	0.41	2N4286	0.18
BCY70	0.15	2N2907A	0.22	OC75	0.16	BC140	0.31	2N4287	0.18
BCY71	0.20	2N2923	0.15	OC76	0.16	BC141	0.31	2N4288	0.18
BCY72	0.15	2N2924	0.15	OC77	0.26	BC142	0.31	2N4289	0.18
BCZ10	0.20	2N2925	0.15	OC81	0.16	BC143	0.31	2N4290	0.18
BCZ11	0.26	ACY35	0.21	OC81D	0.16	BC145	0.46	2N4291	0.18
BCZ12	0.26	ACY36	0.29	OC82	0.16	BC147	0.10	2N4292	0.18
BD115	0.63	ACY40	0.18	OC82D	0.16	BC148	0.10	2N4293	0.18
BD116	0.63	ACY41	0.19	OC83	0.20	BC149	0.12	2N5172	0.12
BD121	0.61	ACY44	0.36	OC139	0.20	BC150	0.19	2N5194	0.56
BD123	0.67	AD130	0.39	OC140	0.20	BC151	0.20	2N5294	0.56
BD124	0.70	AD140	0.49	OC169	0.26	BC152	0.18	2N5296	0.56
BD131	0.51	AD142	0.49	OC170	0.26	BC153	0.29	2N5457	0.32
BD132	0.61	AD143	0.39	OC171	0.26	BC154	0.31	2N5458	0.32
BD133	0.67	AD149	0.51	OC299	0.26	BC157	0.19	2N5459	0.41
BD135	0.41	AD161	0.36	OC201	0.29	BC158	0.12	2N6122	0.69
BFY53	0.18	AD162	0.36	OC202	0.29	BC159	0.12	2S301	0.51
BSX19	0.16	AD161 &	OC203	0.26	BC160	0.46	2S302A	0.43	
BSX20	0.16	AD162(MP)	0.69	OC204	0.26	BC161	0.51	2S302	0.43
BSY25	0.16	ADT140	0.51	OC205	0.36	BC167	0.12	2S303	0.56
BSY26	0.16	AF114	0.25	OC309	0.41	BC168	0.12	2S304	0.71
BSY27	0.16	AF115	0.25	OC7P1	0.44*	BC169	0.12	2S305	0.80
BSY28	0.16	AF116	0.25	ORP12	0.44*	BC170	0.12	2S306	0.80
BSY29	0.16	AF117	0.25	ORP60	0.41*	BC171	0.15	2S307	0.80
BSY38	0.19	AF118	0.36	ORP61	0.41*	BC172	0.15	2S321	0.75
BSY39	0.19	AF124	0.31	P20	0.51*	BF167	0.22		

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Type	Quantities			Type	Quantities			Type	Quantities		
	1	25	100+		1	25	100+		1	25	100+
7400	0.14	0.18	0.12	7448	£1.02	0.99	0.97	74122	0.65	0.63	0.60
7401	0.14	0.13	0.12	7450	0.14	0.13	0.12	74123	0.69	0.68	0.65
7402	0.14	0.13	0.12	7451	0.14	0.13	0.12	74141	0.79	0.76	0.73
7403	0.14	0.13	0.12	7453	0.14	0.13	0.12	74145	£1.20	£1.16	£1.11
7404	0.14	0.13	0.12	7454	0.14	0.13	0.12	74150	£1.39	£1.30	£1.20
7405	0.14	0.13	0.12	7460	0.14	0.13	0.12	74151	£1.02	0.97	0.93
7406	0.36	0.31	0.29	7470	0.30	0.27	0.25	74153	0.93	0.88	0.83
7407	0.36	0.31	0.29	7472	0.30	0.27	0.25	74154	£1.57	£1.48	£1.48
7408	0.28	0.22	0.21	7473	0.						

# PO BOX 6 WARE HERTS

## SUPER UNTESTED PAKS

Pak No.	Description	Price
		£p
U 1	120 Glass Sub-min. General purpose Germ. diodes	0.60
U 2	50 Mixed Germanium transistors AF/RF	0.60
U 3	75 Germanium gold bonded sub-min. like OA5, PA47	0.60
U 4	30 Germanium Transistors like OC81, AC128	0.60
U 5	60 200mA sub-min. silicon diodes	0.60
U 6	30 Sil. Planar trans. NPN like BSY95A, 2N706	0.60
U 7	16 Sil. rect. TOP-HAT 750mA, VLTG. RANGE up to 100	0.60
U 8	50 Sil. planar diodes DO-7 glass 250mA like OA200/202	0.60
U 9	20 Mixed voltages, 1 Watt Zener Diodes	0.60
U10	20 BAY50 charge storage diodes DO-7 glass	0.60
U11	20 PNP Sil. planar trans. TO-5 like 2N1132, 2N2904	0.60
U13	30 PNP-NPN Sil. transistors OC200 & 2S104	0.60
U14	150 Mixed silicon and germanium diodes	0.60
U15	20 NPN Sil. planar trans. TO-5 like 2N696, 2N697	0.60
U16	10 3 Amp sil. rectifiers stud type up to 1000 PIV	0.60
U17	30 Germanium PNP AF transistors TO-5 like ACY 17-22	0.60
U18	8 6Amp sil. rectifiers BYZ13 type up to 600 PIV	0.60
U19	20 Silicon NPN transistors like BC 108	0.60
U20	12 1-5 Amp sil. rectifiers top hat up to 1000 PIV	0.60
U21	30 AF. Germ. alloy transistors 2G300 series & OC71	0.60
U23	25 MADT's like MHz series PNP transistors	0.60
U24	20 Germ. 1 Amp rectifiers GJM series up to 300 PIV	0.60
U25	25 300 MHz NPN silicon transistors 2N708, BSY27	0.60
U26	30 Fast switching silicon diodes like 1N914 Micro-Min.	0.60
U29	10 1 Amp SCR's TO-5 can. up to 600 PIV CRS1/25-600	£1.20*
U32	25 Zener diodes 400 mW DO-7 case 3-33 volts mixed	0.60
U33	15 Plastic case 1 Amp sil. rectifiers 1N4000 series	0.60
U34	30 Silicon PNP alloy trans. TO-5 BCY26 2S302/4	0.60
U35	25 Silicon planar transistors PNP TO-18 2N2906	0.60
U36	20 Silicon planar NPN transistors TO-5 BFY50/51/52	0.60
U37	30 Silicon alloy transistors SO-2 PNP OC200, S2322	0.60
U38	20 Fast switching silicon trans. NPN 400 MHz 2N3011	0.60
U39	30 RF. Ger. PNP transistors 2N1303/5 TO-5	0.60
U40	10 Dual transistors 6 lead TO-5 2N2060	0.60
U43	25 Silicon trans. plastic TO-18 A.F. BC113/114	0.60
U44	20 Silicon trans. plastic TO-5 BC115	0.60
U45	7 3A SCR. TO-66 up to 600 PIV	£1.20*
U46	20 Unijunction transistors similar to TIS43	0.60*
U47	10 TO220 AB plastic triacs 50 V 6 A	£1.20*
U48	9 NPN Sil. power transistors like 2N3055	£1.20
U49	12 NPN Sil. plastic power trans. 60 W like 2N5294/5296	£1.20

Code No's mentioned above are given as a guide, to the type of device in the pak. The devices themselves are normally unmarked.

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TO.3 Plastic Encapsulation	
µA.7805/L129 5V	(Equip. to MVR5V) £1.25p
µA.7812/L130 12V	(Equip. to MVR12V) £1.25p
µA.7815/L131 15V	(Equip. to MVR15V) £1.25p
µA.7818 18V	(Equip. to MVR18V) £1.25p

## THYRISTORS

PIV	0.6A TO18	0.8A TO92	1A TO5	3A TO66	5A TO66	5A TO64	7A TO48	10A TO48	16A TO48	30A TO48
10	0.13	0.15	-	-	-	-	-	-	-	-
20	0.15	0.18	-	-	-	-	-	-	-	-
30	0.19	0.22	-	-	-	-	-	-	-	-
50	0.22	0.28	0.20	0.25	0.36	0.36	0.48	0.51	0.54	£1.18
100	0.25	0.30	0.25	0.25	0.48	0.48	0.51	0.57	0.58	£1.43
150	0.31	0.38	-	-	-	-	-	-	-	-
200	0.38	0.44	0.25	0.30	0.50	0.50	0.57	0.62	0.62	£1.63
400	-	-	0.30	0.39	0.55	0.57	0.62	0.71	0.77	£1.79
600	-	-	0.39	0.48	0.69	0.69	0.78	0.99	0.90	-
800	-	-	0.58	0.65	0.81	0.81	0.92	£1.22	£1.39	£4.07

## DIODES

Type	Price	Type	Price	Type	Price	Type	Price
AA119	0.08	BY101	0.12	BY216	0.41	OA85	0.09
AA120	0.08	BY105	0.18	BY217	0.36	OA90	0.07
AA129	0.08	BY114	0.12	BY218	0.36	OA91	0.07
AA30	0.09	BY124	0.12	BY219	0.28	OA95	0.07
AA213	0.10	BY126	0.15	CG62	-	OA200	0.07
BA100	0.10	BY127	0.16	(OA91 Eq)	0.06	OA202	0.07
BA116	0.21	BY128	0.16	CG651 (OA70)	0.07	SD10	0.06
BA126	0.22	BY130	0.17	OA79	0.07	SD19	0.06
BA148	0.15	BY133	0.21	OAS Short	-	IN34	0.07
BA154	0.12	BY164	0.51	Leads	0.21	IN34A	0.07
BA155	0.15	BX38/30	0.43	OA10	0.14	IN914	0.06
BA156	0.14	BY210	0.36	OA47	0.07	IN916	0.06
BA173	0.15	BY211	0.31	OA70	0.07	IN4148	0.06
BB104	0.15	BY212	0.31	OA79	0.07	IS021	0.10
BY100	0.16	BY213	0.26	OA81	0.07	IS951	0.70

## QUALITY TESTED PAKS

Pak No.	Quality Tested Paks	Price
Q 1	20 Red spot transistors PNP	0.60
Q 2	16 White spot R.F. transistors PNP	0.60
Q 3	4 OC 77 type transistors	0.60
Q 4	6 Matched transistors OC44/45/81/81 D	0.60
Q 5	4 OC 75 transistors	0.60
Q 6	5 OC 72 transistors	0.60
Q 7	4 AC 128 transistors PNP high gain	0.60
Q 8	4 AC 126 transistors PNP	0.60
Q 9	7 OC 81 type transistors	0.60
Q10	7 OC 71 type transistors	0.60
Q11	2 AC 127/128 Complementary pairs PNP/NPN	0.60
Q12	3 AF 116 type transistors	0.60
Q13	3 AF 117 type transistors	0.60
Q14	3 OC 171 H.F. type transistors	0.60
Q15	7 2N2926 Sil. Epoxy transistors mixed colours	0.60
Q17	5 NPN 2 x ST.141. & 3 x ST.140	0.60
Q18	4 MADT'S 2 x MAT 100 & 2 x MAT 120	0.60
Q19	3 MADT'S 2 x MAT 101 & 1 x MAT 121	0.60
Q20	4 OC 44 Germanium transistors A.F.	0.60
Q21	4 AC 127 NPN Germanium transistors	0.60
Q22	20 NKT transistors A.F. R.F. coded	0.60
Q23	10 OA 202 Silicon diodes sub-min	0.60
Q24	8 OA 81 diodes	0.60
Q25	15 1N914 Silicon diodes 75 PIV 75 mA	0.60
Q26	8 OA 95 Germanium diodes sub-min-1N69	0.60
Q27	2 10A 600 PIV Silicon rectifiers 1S425B	0.60*
Q28	2 Silicon power rectifiers BYZ 13	0.60*
Q29	4 Sil. transistors 2 x 2N696, 1 x 2N697, 1 x 2N698	0.60
Q30	7 Silicon switch transistors 2N706 NPN	0.60
Q31	6 Silicon switch transistors 2N708 NPN	0.60
Q32	3 PNP Sil. trans. 2 x 2N1131, 1 x 2N1132	0.60
Q33	3 Silicon. NPN transistors 2N1711	0.60
Q34	7 Sil. NPN trans. 2N2369, 500 MHz (code P397)	0.60
Q35	3 Silicon. PNP TO-5 2 x 2N2904 & 1 x 2N2095	0.60
Q36	7 2N3646 TO-18 plastic 300 MHz NPN	0.60
Q37	3 2N3053 NPN Silicon transistors	0.60
Q38	5 PNP transistors 3 x 2N3703, 2 x 2N3702	0.60
Q39	5 NPN transistors 3 x 2N3704, 2 x 2N3705	0.60
Q40	5 NPN transistors 3 x 2N3707, 2 x 2N3708	0.60
Q41	3 Plastic NPN TO18 2N3904	0.60
Q43	5 BC 107 NPN transistors	0.60
Q44	5 NPN transistors 3 x BC 108, 2 x BC 109	0.60
Q45	3 BC 113 NPN TO-18 transistors	0.60
Q46	3 BC 115 NPN TO-5 transistors	0.60
Q47	4 NPN high gain transistors 2 x BC 157, 2 x BC 168	0.60
Q48	3 BCY 70 NPN transistors TO-18	0.60
Q49	3 NPN transistors 2 x BFY 51, 1 x BFY 52	0.60
Q50	7 BSY 28 NPN switch transistors TO-18	0.60
Q51	7 BSY 95A NPN transistors 300 MHz	0.60
Q52	8 BY 100 type silicon rectifiers	£1.20
Q53	25 Sil. & Germ. trans. mixed all marked new	£1.50
Q54	6 TIL 209 Red LED	£1.20*

## UNTESTED T.T.L. PAKS

Manufacturers "Fall Outs" which include Functional and part Functional Units. These are classed as 'out-of-spec' from the makers' very rigid specifications, but are ideal for learning about I.C.'s and experimental work.

Pak No.	Contents	Price	Pak No.	Contents	Price
UIC00	= 12 x 7400	0.60	UIC72	= 8 x 7472	0.60
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UIC03	= 12 x 7403	0.60	UIC75	= 8 x 7475	0.60
UIC04	= 12 x 7404	0.60	UIC76	= 8 x 7476	0.60
UIC05	= 12 x 7405	0.60	UIC80	= 5 x 7480	0.60
UIC06	= 8 x 7406	0.60	UIC81	= 5 x 7481	0.60
UIC07	= 8 x 7407	0.60	UIC82	= 5 x 7482	0.60
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UIC43	= 5 x 7443	0.60	UIC95	= 5 x 7495	0.60
UIC44	= 5 x 7444	0.60	UIC96	= 5 x 7496	0.60
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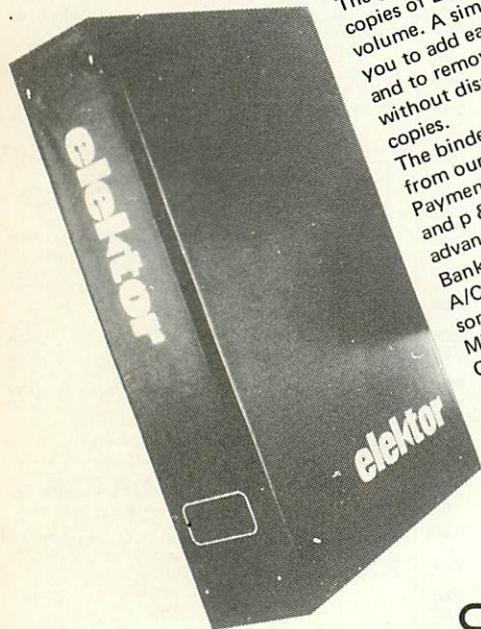
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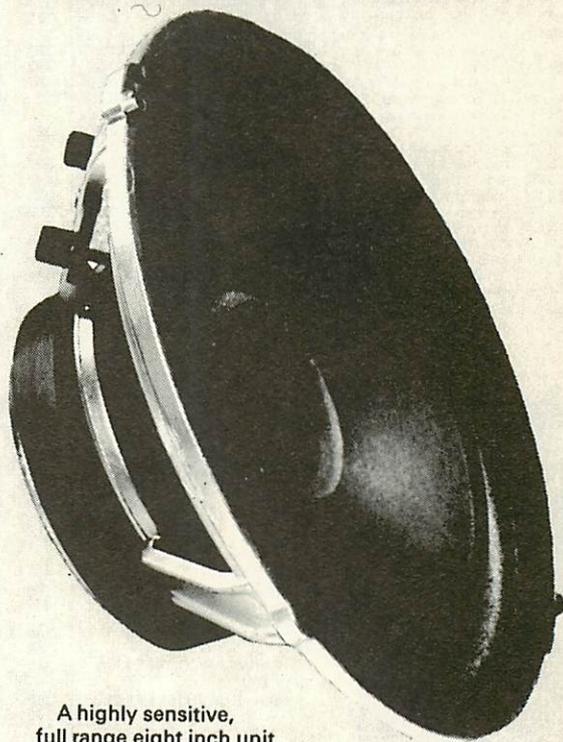
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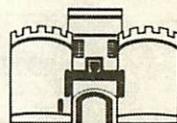
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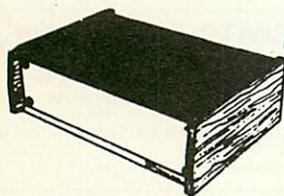


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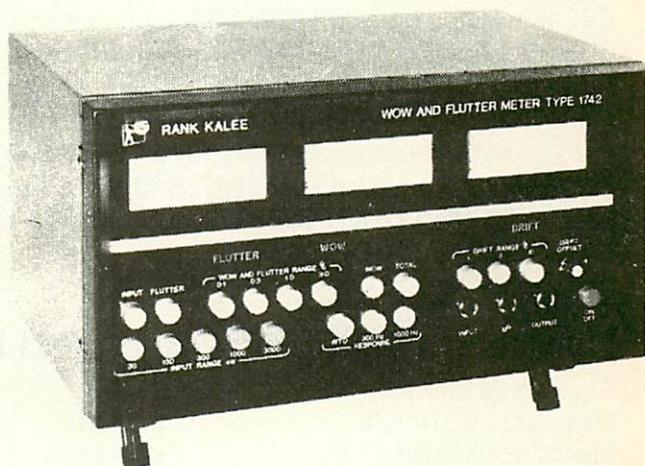
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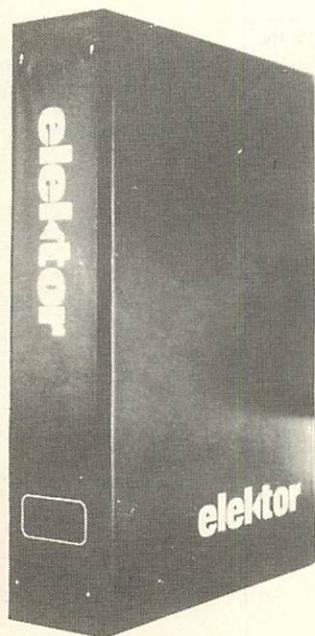
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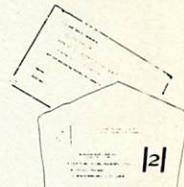
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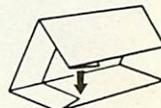
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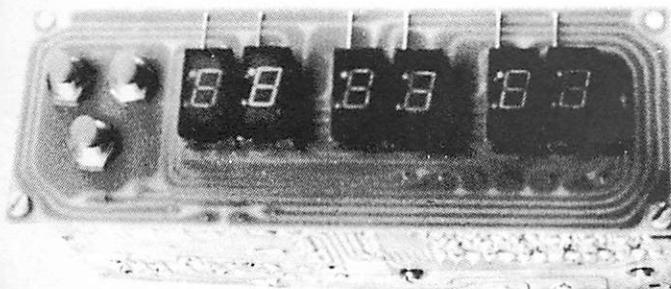
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